SLAS490-OCTOBER 2005



16-BIT, 2-MSPS, LVDS SERIAL INTERFACE, SAR ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 2-MHz Sample Rate
- 16-Bit Resolution
- SNR 92 dB at 10 kHz I/P
- THD –107 dB at 10 kHz I/P
- ±1 LSB Typ, ±2 LSB INL Max
- +0.7/-0.5 LSB Typ, +1.5/-1 LSB DNL Max
- Unipolar Differential Input Range: –4 V to 4 V
- Internal Reference
- Internal Reference Buffer
- 200-Mbps LVDS Serial Interface
- Optional 200-MHz Internal Interface Clock
- 16-/8-Bit Data Frame
- Zero Latency at Full Speed
- Power Dissipation: 290 mW at 2 MSPS
- Nap Mode (125 mW Power Dissipation)
- Power Down (5 μW)
- 48-Pin QFN Package

APPLICATIONS

- Medical Instrumentation
- High-Speed Data Acquisiton Systems
- High-Speed Close-Loop Systems
- Communication

DESCRIPTION

The ADS8413 is a 16-bit, 2-MSPS, analog-to-digital (A/D) converter with 4-V internal reference. The device includes a capacitor based SAR A/D converter with inherent sample and hold.

The ADS8413 also includes a 200-Mbps, LVDS, serial interface. This interface is designed to support daisy chaining or cascading of multiple devices. A selectable 16-/8-bit data frame mode enables the use of a single shift register chip (SN65LVDS152) for converting the data to parallel format.

The ADS8413 unipolar differential input range supports a differential input swing of $-V_{ref}$ to $+V_{ref}$ with a common-mode voltage of $+V_{ref}/2$.

The nap feature provides substantial power saving when used at lower conversion rates.

The ADS8413 is available in a 48-pin QFN package.

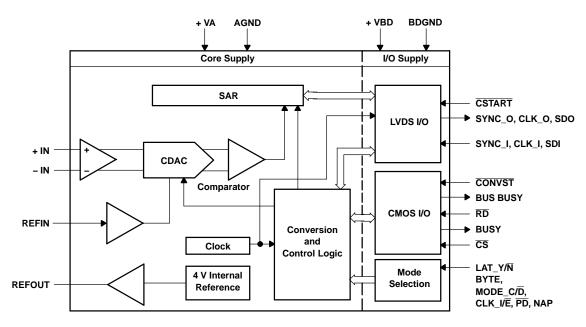
High-Speed SAR Converter Family

Type/Speed	500 kHz	~ 600 kHz	750 kHZ	1 MHz	1.25 MHz	2 MHz	3 MHz	4 MHz
40 Dit Doordo Diff	ADS8383	ADS8381						
18-Bit Pseudo-Diff		ADS8380 (S)						
18-Bit Pseudo-Bipolar, Fully Diff		ADS8382 (S)						
						ADS8411		
16-Bit Pseudo-Diff		ADS8370 (S)	ADS8371		ADS8401/05	ADS8410 (S-LVDS)		
						ADS8412		
16-Bit Pseudo-Bipolar, Fully Diff		ADS8372 (S)				ADS8413 (S-LVDS)		
14-Bit Pseudo-Diff					ADS7890 (S)		ADS7891	
12-Bit Pseudo-Diff								ADS7881



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





ORDERING INFORMATION(1)

MODEL	MAXIMUM INTEGRAL LINEARITY (LSB)	MAXIMUM DIFFERENTIAL LINEARITY (LSB)	NO MISSING CODES AT RESOLUTION (BIT)	PACKAGE TYPE	PACKAGE DESIGNATOR	TEMPERATURE RANGE	ORDERING INFORMATION	TRANSPORT MEDIA QUANTITY
ADS8413IB	±2	1.5/–1	16	48 pin	RGZ	-40°C	ADS8413IBRGZT	250
AD36413IB	±2	1.5/-1	16	QFN	RGZ	to 85°C	ADS8413IBRGZR	2000
ADS8413I	±4	3/–1	16	48 pin	RGZ	-40°C	ADS8413IRGZT	2000 250 2000
AD58413I	± 4	3/-1	16	QFN	RGZ	to 85°C	ADS8413IRGZR	

⁽¹⁾ For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		UNIT
+IN to AGND		-0.3 V to +VA + 0.3 V
-IN to AGND		-0.3 V to +VA + 0.3 V
+VA to AGND		−0.3 to 7 V
+VBD to BDGND		−0.3 to 7 V
Digital input voltage to GND		-0.3 V to (+VBD + 0.3 V)
Digital output to GND		-0.3 V to (+VBD + 0.3 V)
Operating temperature range		-40°C to 85°C
Storage temperature range		–65°C to 150°C
Junction temperature (T _J max)		150°C
	Power dissipation	$(T_J Max - T_A)/\theta_{JA}$
QFN package	θ _{JA} Thermal impedance	86°C/W
	Vapor phase (60 sec)	215°C
Lead temperature, soldering	Infrared (15 sec)	220°C

⁽¹⁾ Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



SPECIFICATIONS

 $T_A = -40$ °C to 85 °C, +VA = 5 V,+VBD = 5 V or 3.3 V, $V_{ref} = 4.096$ V, $f_{sample} = 2$ MHz (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT		
ANALOG I	INPUT								
	Full-scale input voltage span	(1)	+IN - (-IN)	-V _{ref}		V_{ref}	V		
	Absolute input voltage renge		+IN	-0.2		V _{ref} + 0.2	V		
	Absolute input voltage range		-IN	-0.2		V_{ref} + 0.2	V		
	Input common-mode voltage	range		V _{ref} /2-0.2	V _{ref} /2	V _{ref} /2+0.2	V		
Ci	Input capacitance				25		pF		
	Input leakage current				500		pA		
SYSTEM P	PERFORMANCE					<u> </u>			
	Resolution				16		Bits		
	No mission and a	ADS8413IB		16			D:4-		
	No missing codes	ADS8413I		16			Bits		
		ADS8413IB		-2	±1	2	1.05(3)		
INL	Integral linearity (2)	ADS8413I		-4.0	±2	4.0	LSB ⁽³⁾		
		ADS8413IB		-1	0.7/–0.5	1.5	(0)		
DNL	Differential linearity	ADS8413I	1	-1.0	1.5/-0.8	V _{ref} + 0.2 V _{ref} /2+0.2 S 0 6 1	LSB ⁽³⁾		
		ADS8413IB		-1	±0.2	±1 3.0 0.03 0.1			
Eo	Offset error	ADS8413I	External reference	-3.0	±1	3.0	mV		
		ADS8413IB		-0.1	±0.03	0.1			
E _G	Gain error ⁽⁴⁾	ADS8413I	External reference	-0.15	±0.1	0.15	% of FS		
CMMR	Common-mode rejection ratio)	With common mode input signal = 200 mV _{p-p} at 1 MHz				dB		
PSRR	Power supply rejection ratio		At FFF0 _H output code		80		dB		
SAMPLING	G DYNAMICS								
			+VBD = 5 V		360	391			
	Conversion time		+VBD = 3 V			391	ns		
	A 1.101 of		+VBD = 5 V	100					
	Acquisition time		+VBD = 3 V	100			ns		
	Maximum throughput rate with	h or without latency				2.0	MHz		
	Aperture delay				20		ns		
	Aperture jitter				10		psec		
	Step response				50		ns		
	Overvoltage recovery				50		ns		
DYNAMIC	CHARACTERISTICS								
			V _{IN} 0.5 dB below FS at 10 kHz		-107				
THD	Total harmonic distortion (5)		V _{IN} 0.5 dB below FS at 100 kHz		-95		dB		
			V _{IN} 0.5 dB below FS at 0.5 MHz		-90				
			V _{IN} 0.5 dB below FS at 10 kHz		92				
SNR	Signal-to-noise ratio		V _{IN} 0.5 dB below FS at 100 kHz		90		dB		
	·		V _{IN} 0.5 dB below FS at 0.5 MHz		89		ű -		
			V _{IN} 0.5 dB below FS at 10 kHz		92				
SINAD	Signal-to-noise and distortion		V _{IN} 0.5 dB below FS at 100 kHz		86		dB		
=	- 5		V _{IN} 0.5 dB below FS at 0.5 MHz		84				
			V _{IN} 0.5 dB below FS at 10 kHz		-113				
			- IIV 5.5 GD 551511 1 5 dt 10 lt 12						
SEDR	Spurious free dynamic range		V _{IN} 0.5 dB below FS at 100 kHz		_98		dВ		
SFDR	Spurious free dynamic range		V _{IN} 0.5 dB below FS at 100 kHz V _{IN} 0.5 dB below FS at 0.5 MHz		-98 -93		dB		

- Ideal input span; does not include gain or offset error.
 This is endpoint INL, not best fit.
 Least significant bit

- Measured relative to actual measured reference.
- (5) Calculated on the first nine harmonics of the input frequency.



SPECIFICATIONS (continued)

 $T_A = -40$ °C to 85 °C, +VA = 5 V,+VBD = 5 V or 3.3 V, $V_{ref} = 4.096$ V, $f_{sample} = 2$ MHz (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
EXTERNAL	REFERENCE INPUT							
	Input voltage range, V _{REF}			3.9	4.096	4.2	V	
	Resistance ⁽⁶⁾		To internal reference voltage		500		kΩ	
INTERNAL	REFERENCE OUTPUT							
	Start-up time		From 95% (+VA), with 1-μF storage capacitor on REFOUT to AGND			25	ms	
	Reference voltage range, V _{ref}		At room temperature	4.080	4.096	4.112	V	
	Source current		Static load			10	μΑ	
	Line regulation		+VA = 4.75 V to 5.25 V		0.6		mV	
	Drift		IOUT = 0 V		36		PPM/°C	
POWER SU	PPLY REQUIREMENTS							
	Dawar ayaab yaltaga	+VBD		2.7	3.3	5.25		
	Power supply voltage	+VA		4.75	5	5.25	V	
	Supply current, 2-MHz sample rate	+VA			58	64	mA	
	Power dissipation, 2-MHz sample ra	ite	+VA = 5 V		290	320	mW	
NAP MODE				•				
	Supply current	+VA			25		mA	
POWER DO	WN							
	Supply current	+VA			1	2.5	μΑ	
	Powerdown time				10		μs	
	Powerup time		With 1-μF storage capacitor on REFOUT to AGND		25		ms	
	Invalid conversions after power up of	or reset			3		Numbers	
TEMPERAT	URE RANGE							
	Operating free air			-40		85	°C	
LOGIC FAN	IILY CMOS							
V _{IH}	High-level input voltage		I _{IH} = 5 μA	+VBD -1		+VBD +0.3	V	
V _{IL}	Low-level input voltage		I _{IL} = 5 μA	-0.3		0.8	V	
V _{OH}	High-level output voltage		I _{OH} = 2 TTL loads	+VBD - 0.6		+VBD	V	
V _{OL}	Low-level output voltage		I _{OL} = 2 TTL loads	0		0.4	V	
LOGIC FAN	IILY LVDS ⁽⁷⁾			1				
DRIVER								
V _{OD(SS)}	Steady-state differential output volta magnitude	ge		247	340	454		
$\Delta V_{OD(SS)} $	Change in steady-state differential of magnitude between logic states	output voltage	R_L = 100 Ω, See Figure 52, Figure 53	-50		50	mV	
V _{OC(SS)}	Steady-state common-mode output	voltage		1.125	1.2	1.375	V	
$\Delta V_{OC(SS)} $	Change in steady-state common-movoltage between logic states	ode output	See Figure 54	-50		50		
V _{OC(pp)}	Peak to peak change in common-m voltage	ode output			50	150	mV	
	Object singuit suits in		V _{OY} or V _{OZ} = 0 V		3	10	^	
Ios	Short circuit output current		V _{OD} = 0 V		3	10	mA	
l _{oz}	High impedance output current		VO = 0 V or +VBD	-5		5	μΑ	

⁽⁶⁾ Can vary ±20%(7) All min max values ensured by design.



SPECIFICATIONS (continued)

 $T_A = -40$ °C to 85°C, +VA = 5 V,+VBD = 5 V or 3.3 V, $V_{ref} = 4.096$ V, $f_{sample} = 2$ MHz (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
RECEIVE	ER .					
$V_{\text{ITH+}}$	Positive going differential voltage threshold				50	mV
V _{ITH-}	Negative going differential voltage threshold		-50			mv
V _{IC}	Common mode input voltage		0.2	1.2	2.2	V
Cı	Input capacitance			5		pF

TIMING REQUIREMENTS

 $T_A = -40^{\circ}\text{C}$ to 85°C , +VA = 5 V, +VBD = 5 V or 3.3 V (unless otherwise noted)

	PARAMETER		MIN	TYP MAX	UNIT	REF
SAM	PLING AND CONVERSION RELATED					
acq	Acquisition time		100		ns	Figure 1, Figure 2
cnv	Conversion time			391	ns	Figure 1, Figure 2
w1	Pulse duration, CONVST high		100		ns	Figure 1
w2	Pulse duration, CONVST low	40		ns	Figure 1, Figure 2	
11	Delay time, CONVST rising edge to sample start			5	ns	Figure 1
d2	Delay time, CONVST falling edge to conversion start			5	ns	Figure 1, Figure 2
	Delegation OONIVOT felling advantable	+VBD = 3.3 V		14		Figure 1,
13	Delay time, CONVST falling edge to busy high	+VBD = 5 V		13	ns	Figure 2
	Delegations are assessed to be seen beautiful and the beautiful an	+VBD = 3.3 V		8		Figure 1,
14	Delay time, conversion end to busy low	+VBD = 5 V		7	ns	Figure 2
v3	Pulse duration, CSTART high	l.	100		ns	Figure 1, Table 2
<i>i</i> 4	Pulse duration, CSTART low	45		ns	Figure 1, Figure 2, Table 2	
15	Delay time, CSTART rising edge to sample start		7.5	ns	Figure 1, Table 2	
d6	Delay time, CSTART falling edge to conversion start		7.5	ns	Figure 1, Figure 2, Table 2	
	Delevatives OCTADT fellings along to be seen black	+VBD = 3.3 V		16.5		Figure 1,
17	Delay time, CSTART falling edge to busy high	+VBD = 5 V		15.5	ns	Figure 2, Table 2
O F	ELATED				I	
8	Delay time, RD falling edge while CS low to BUS_BUSY high			16	ns	Figure 5
	Delay time, RD falling edge while CS low to SYNC_O and SDO out of	+VBD = 3.3 V		29		
9	3-state condition (for device with LAT_Y/N pulled low)	+VBD = 5 V		28	ns	Figure 5
10	Delay time, pre_conversion end (point A) to SYNC_O and SDO out of condition	3-state		22	ns	Figure 6
	Delay time, pre_conversion end (point A) to BUS_BUSY high	VBD = 3.3 V		8	ns	Figure 6
111	belay time, pre_conversion end (point A) to 605_6051 high	+VBD = 5 V		7	115	rigure o
12	Delay time, conversion phase end to SYNC_O high		6	9 + t _{CLK}	ns	Figure 6
13	Delay time, RD falling edge while CS low to SYNC_O high	+VBD = 3.3 V +VBD = 5 V	5.5 + 4*t _{CLK} 5 + 4*t _{CLK}	8.5 + 5*t _{CLK} 8 + 5*t _{CLK}	ns	Figure 5
<i>ı</i> 5	Pulse duration, RD low for device in no latency mode		5	GLK	ns	Figure 11
•0		+VBD = 3.3 V		1.4	113	
114	Delay time, CLK_O rising edge to data valid	+VBD = 5 V		1.3	ns	Figure 5, Figure 6
115	Delay time, BUS_BUSY low to SYNC_O high in daisy chain mode	+VBD = 3.3 V	4*t _{CLK} 6.5	4*t _{CLK} -3	ns	Figure 7,
110	indicating receiving device to output the data	+VBD = 5 V	4*t _{CLK} 6	4*t _{CLK} - 2.5		Figure 12



TIMING REQUIREMENTS (continued)

 $T_A = -40$ °C to 85°C, +VA = 5 V, +VBD = 5 V or 3.3 V (unless otherwise noted)

	PARAMETER		MIN	TYP	MAX	UNIT	REF
t _{d16}	Delay time, CLK_O to SDO and SYNC_O 3-state				4	ns	Figure 7, Figure 8, Figure 12, Figure 15
t _{pd1}	Propagation delay time, SYNC_I to SYNC_O in daisy chain mode			1	1 + 0.5*t _{CLK}	ns	Figure 12
t _{d17}	Delay time, SYNC_O and SDO 3-state to BUS_BUSY low in cascade	0		2	ns	Figure 8	
	Delay time, RD rising edge to BUS_BUSY high for device with	+VBD = 3.3 V			8	20	Figure 11,
t _{d18}	$LAT_Y/\overline{N} = 1$	+VBD = 5 V			7	ns	Figure 14
	Delay time, point A indicating clear for bus 3-state release to BUSY	+VBD = 3.3 V			40.5		Figure 6
t _{d19}	falling edge	+VBD = 5 V			40	ns	Figure 6
t _r	Rise time, differential LVDS output signal				950	ps	Figure 53
t _f	Fall time, differential LVDS output signal				950	ps	Figure 53
	CLK frequency (serial data rate)		190		210	MHz	
t _{d20}	Delay time, from PD falling edge to SDO 3-state				10	ns	Figure 22, Figure 23
t _{d21}	Delay time, from PD falling edge to device powerdown				10	μs	Figure 22, Figure 23
t _{d22}	Delay time, from PD rising edge to device powerup			25	ms	Figure 22, Figure 23	
t _{s1}	Settling time, internal reference after first three conversions			4	ms	Figure 22	
t _{d23}	Delay time, CONVST falling edge to start of restricted zone for start of	f data read cycle			335	ns	Figure 9
t _{d24}	Delay time, CONVST falling edge to end of restricted zone for start of	data read cycle			406	ns	Figure 9



DEVICE INFORMATION

RGZ PACKAGE (TOPVIEW) AGND 11 10 48 □ BUS_BUSY REFIN [47 RD REFOUT [46 BUSY NC +VA 🗆 45 BDGND 16 AGND 17 44 +VBD 43 SYNC_O + +IN □ 42 SYNC_O -−IN 🗆 41 SDO + AGND 20 40 SDO -+VA 🛚 39 CLK_O + +VA ☐ 22 38 CLK_O -AGND²³ 37 - +VA AGND²⁴ (M2+) SDI + [(M2-) SDI - [AGND□ ¥, AGND[+) SYNC_I + CSTART+ CSTART--) SYNC_I

NC - No internal connection

TERMINAL FUNCTIONS

ξ

TE	TERMINAL		DESCRIPTION						
NO.	NAME	I/O	DESCRIPTION						
			ANALOG PINS						
11, 12	REFM	I	Reference ground. Connect to analog ground plane.						
13	REFIN	1	Reference (positive) input. Decouple with REFM pin using $0.1-\mu F$ bypass capacitor and $1-\mu F$ storage capacitor.						
14	REFOUT	0	Internal reference output. Short to REFIN pin when internal reference is used. Do not connect to REFIN pin when external reference is used. Always decouple with AGND using 0.1-μF bypass capacitor.						
18	+IN	I	Noninverting analog input channel						
19	-IN	I	Inverting analog input channel						
	LVDS I/O PINS(1)								
28, 29	CSTART+ CSTART-	I	Device sample and convert control input. Device enters sample phase with rising edge of CSTART and conversion phase starts with falling edge of CSTART (provided other conditions are satisfied). Set CSTART = 0 when CONVST input is used.						

⁽¹⁾ All LVDS inputs and outputs are differential with signal+ and signal- lines. Whenever only the 'signal' is mentioned it refers to the signal+ line and signal- line is the compliment. For example CLK_O refers to CLK_O+.



DEVICE INFORMATION (continued)

TERMINAL FUNCTIONS (continued)

 -	TERMINAL FONCTIONS (COntinued)										
	1	1/0	DESCRIPTION								
NO.	NAME										
30,	SYNC_I + SYNC_I-	I Dasiy Chain	Connect to previous device SYNC_O with same polarity, while device is selected to operate in daisy chain mode.								
31	M1+ M1-	I Cascade	Mode 1 (valid in cascade mode only). CLK_O available while M1=1 (LVDS) or M1+ is pulled up to +VBD and M1- is grounded (AGND). CLK_O o/p goes to 3-state when M1 = 0 (LVDS) or M1+ is grounded (AGND) and M1- is pulled up to +VBD. Do not allow these pins to float.								
32,	SDI+ SDI-	I Daisy Chain	Serial data input. Connect to previous device SDO with same polarity, while device is selected to operate in daisy chain mode.								
33	M2+ M2-	I Cascade	Mode 2 (valid in cascade mode only). Doubles LVDS o/p current while M2 = 1 (LVDS) or M2+ is pulled up to +VBD and M2- is grounded (AGND). LVDS o/p current is normal (3.4 mA typ) when M2 = 0 (LVDS) or M2+ is grounded (AGND) and M2 - is pulled up to +VBD. Do not allow these pins to float.								
34, 35	CLK_I+ CLK_I-	I.	Serial external clock input. Set CLK_I/E (pin 7) = 0 to select external clock source.								
38, 39	CLK_O- CLK_O+	0	Serial clock out. Data is latched out on the rising edge of CLK_O and can be captured on the next falling edge.								
40, 41	SDO- SDO+	0	Serial data out. Data is latched out on the rising edge of CLK_O with MSB first format.								
42, 43	SYNC_O - SYNC_O +	0	Synchronizes the data frame. (2)								
			CMOS I/O PINS								
1	CS	1	Chip select, active low signal. All of the LVDS o/p except CLK_O are 3-state if this pin is high.								
2	CONVST	I	CMOS equivalent of CSTART input. So functionality is the same as the CSTART input. Set CONVST = 0 when the CSTART input is used.								
3	BYTE	I.	Controls the data frame (2) duration. The frame duration is 16 CLKs if BYTE = 0 or 8 CLKs if BYTE = 1.								
4	PD	1	Active low input, acts as device power down.								
5	NAP	I	Selects nap mode while high. Device enters nap state at conversion end and remains so until next acquisition phase begins.								
6	$MODE_C/\overline{D}$	I	Selects cascade (MODE_C/ \overline{D} = 1) or daisy chain mode (MODE_C/ \overline{D} = 0).								
7	CLK_I/E	I	Selects the source of the I/O clock. CLK_I/E = 1 selects internally generated clock with 200-MHz typ frequency. CLK_I/E = 0 selects CLK_I as the I/O clock.								
8	LAT_Y/N	I	Controls the data read with latency (LAT_Y/ \overline{N} = 1) or without latency ((LAT_Y/ \overline{N} = 0). It is essential to set LAT_Y/ \overline{N} = 0 for the first device in daisy chain or cascade.								
46	BUSY	0	Active high signal, indicates a conversion is in progress.								
47	RD	ı	Data read request to the device, also acts as a hand shake signal for daisy chain and cascade operation.								
48	BUS_BUSY	0	Status output. Indicates that the bus is being used by the device. Connect to \overline{RD} of the next device for daisy chain or cascade operation.								
	1		POWER SUPPLY PINS								
10, 16, 21, 22, 26, 37	+VA	_	Analog power supply and LVDS input buffer power supply.								
9, 17, 20, 23, 24, 25, 27, 36	AGND	_	Analog ground pins. Short to the analog ground plane below the device.								
44	+VBD	_	Digital power supply for all CMOS digital inputs and CMOS, LVDS outputs.								
45	BDGND	-	Digital ground for all digital inputs and outputs. Short to the analog ground plane below the device.								

⁽²⁾ The duration from the first rising edge of SYNC_O to the second rising edge of SYNC_O is one data frame. The data frame duration is 16 CLKs if BYTE = 0 or 8 CLKs if BYTE = 1.



DEVICE INFORMATION (continued)

TERMINAL FUNCTIONS (continued)

TE	TERMINAL		TERMINAL I/O		DESCRIPTION					
NO.	NAME	1/0	DESCRIPTION							
	NOT CONNECTED PINS									
15	NC	_	No connection pins							

Table 1. Device Configuration for Various Modes of Operation

			DEVICE DING	AND DECOM	MENDED	001015	/ELO		COMMENTO	DEFEDENC	E FIGURES	
			DEVICE PINS	AND RECON	IMENDED I	LOGIC LEV	/ELS	ı	COMMENTS	KEFERENC	E FIGURES	
OPERA	TION MODE	MODE_C/D	CLK_I/E	LAT_Y/N	M1+	M1-	M2+	M2-		FOR SAMPLING AND CONVERSION	FOR DATA READ	
					+VBD	AGND	AGND	+VBD			See Figures 3,4	
Cin ala da	da.	1	1 or 0	0	or M1 = 1	LVDS	or M2 = 0	LVDS	Recommended configuration	1 or 2	and 5,6,8 for more details	
Single de	vice	0	1 or 0	0	See comm	nents	See comments		Set SYNC_I and SDI to logic 0 or + terminal to AGND and -ve terminal to +VBD	1 or 2	See Figures 3,4 and 5,6,7 for more details	
Multiple devices in daisy	1st Device	0	1 or 0	0	See comm	nents	See comr	nents	Set SYNC_I and SDI to logic 0 or + terminal to AGND and -ve terminal to +VBD	1 or 2	See Figures 3,4,11 and 6,12	
chain	2nd To last device	0	0	1	See comm	nents	See comr	nents	Maximum 4 devices supported at 2 MSPS with 200-MHz CLK	1 or 2	for more details	
	1at Davisa	4	0	0	+VBD	AGND	AGND	+VBD				
Multiple devices	1st Device	1 0	U	0	or M1 = 1 LVDS		or M2 = 0	LVDS(1)	Maximum 3 devices supported	1 or 2	See Figures 3,4,14 and 6,15	
in cascade	2nd To last	2nd To last		0	0 4	+VBD	AGND	AGND	+VBD	at 2 MSPS	1012	for more details
oasoade	device	1	U	1	or M1 = 0	LVDS	or M2 = 0	LVDS(1)				

⁽¹⁾ Specified polarity is suitable for a $100-\Omega$ differential load across the LVDS outputs. However, polarity can be reversed to double the output current in order to support two $100-\Omega$ loads on both ends of the transmission lines, resulting in $50-\Omega$ net load.

DETAILED DESCRIPTION

SAMPLE AND CONVERT

The sampling and conversion process is controlled by the CSTART (LVDS) or CONVST (CMOS) signal. Both signals are functionally identical. The following diagrams show control with CONVST. The rising edge of CONVST (or CSTART) starts the sample phase, if the conversion has completed and the device is in the wait state. Figure 2 shows the case when the device is in the conversion phase at the rising edge of CONVST. In this case, the sample phase starts immediately at the end of the conversion phase and there is no wait state.

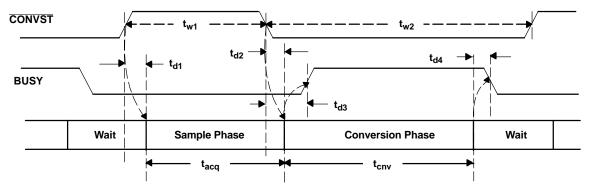


Figure 1. Sample and Convert With Wait (Less Than 2 MSPS Throughput)



DETAILED DESCRIPTION (continued)

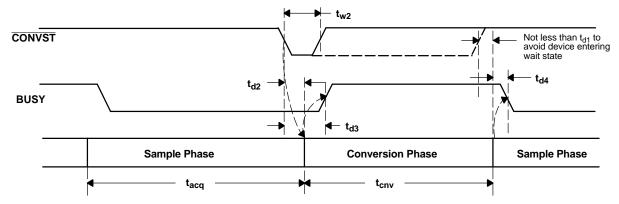


Figure 2. Sample and Convert With No Wait or Back to Back (2 MSPS Throughput)

The device ends the sample phase and enters the conversion phase on the falling edge of $\overline{\text{CONVST}}$ ($\overline{\text{CSTART}}$). A high level on the BUSY output indicates an ongoing conversion. The device conversion time is fixed. The falling edge of $\overline{\text{CONVST}}$ ($\overline{\text{CSTART}}$) during the conversion phase aborts the ongoing conversion. A data read after a conversion abort fetches invalid data. Valid data is only available after a sample phase and a conversion phase has completed. The timing diagram for control with $\overline{\text{CSTART}}$ is similar to Figure 1 and Figure 2. Table 2 shows the equivalent timing for control with $\overline{\text{CONVST}}$ and $\overline{\text{CSTART}}$.

Table 2. CONVST and CSTART Timing Control

DATA READ OPERATION

The ADS8413 supports a 200-MHz serial LVDS interface for data read operation. The three signal LVDS interface (SDO, CLK_O, and SYNC_O) is well suited for high-speed data transfers. An application with a single device or multiple devices can be implemented with a daisy chain or cascade configuration. The following sections discuss data read timing when a single device is used.

DATA READ FOR A SINGLE DEVICE (See Table 1 for Device Configuration)

For a single device, there are two possible read cycle starts: a data read cycle start during a wait or sample phase or a data read cycle start at the end of a conversion phase. Read cycle end conditions can change depending on MODE C/\overline{D} selection. Figure 3 explains the data read cycle. The details of a read frame start with the two previous listed conditions and a read cycle end with MODE C/\overline{D} selection are explained in Figure 5 and Figure 6 and Figure 7 and Figure 8, respectively.



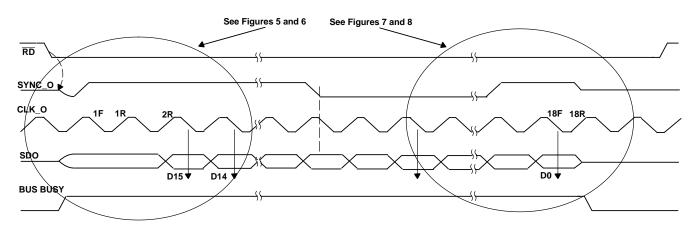


Figure 3. Data Read With \overline{CS} Low and BYTE = 0

As shown in Figure 3, a new data read cycle is initiated with the falling edge of \overline{RD} , if \overline{CS} is low and the device is in a wait or sample phase. The device releases the LVDS o/p (SYNC_O, SDO) from 3-state and sets BUS_BUSY high at the start of the read cycle. The SYNC_O cycle is 16 clocks wide (rising edge to rising edge) if BYTE i/p is held low and can be used to synchronize a data frame. The clock count begins with the first CLK_O falling edge after a SYNC_O rising edge. The MSB is latched out on the second rising edge (2R) and each subsequent data bit is latched out on the rising edge of the clock. The receiver can shift data bits on the falling edges of the clock. The next rising edge of SYNC_O coincides with the 16th rising edge of the clock. D0 is latched out on the 17th rising edge of the clock. The receiver can latch the de-serialized 16-bit word on the 18th rising edge (18R, or the second rising edge after a SYNC_O rising edge).

CS high during a data read 3-states SYNC_O and SDO. These signals remain in 3-state until the start of the next data read cycle.

DATA READ IN BYTE MODE

Byte mode is selected by setting BYTE = 1, this mode is allowed for any condition listed in Table 1. Figure 4 shows a data read operation in byte mode.

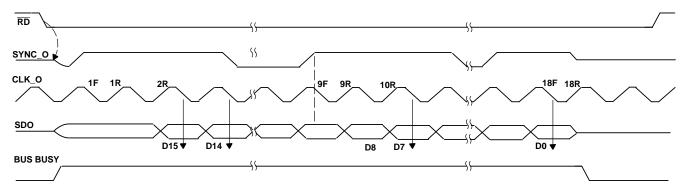


Figure 4. Data Read Timing Diagram with \overline{CS} Low and BYTE = 1

Similar to Figure 3, a new data read cycle is initiated with the falling edge of \overline{RD} , if \overline{CS} is low and device is in a wait or sample phase. The device releases the LVDS o/p (SYNC_O, SDO) from 3-state and sets BUS_BUSY high at the start of the read cycle. The SYNC_O cycle is 8 clocks wide (rising edge to rising edge) if BYTE i/p is held high and can be used to synchronize a data frame. The clock count begins with the first CLK_O falling edge after a SYNC_O rising edge. The MSB is latched out on the second rising edge (2R) and each subsequent data bit is latched out on the rising edge of the clock. The receiver can shift data bits on the falling edges of clock. The next rising edge of SYNC_O coincides with the 8th rising edge of the clock. D8 is latched out on the 9th rising edge of the clock. The receiver can latch the de-serialized higher byte on the 10th rising edge (10R, or second rising edge after a SYNC_O rising edge). The de-serialized lower byte can be latched on the 18th rising edge (18R).



CS high during a data read 3-states SYNC_O and SDO. These signals remain in 3-state until the start of the next data read cycle.

DATA READ CYCLE START DURING WAIT OR SAMPLE PHASE

As shown in Figure 5, the falling edge of \overline{RD} , with \overline{CS} low and the device is in a wait or sample phase, triggers the start of a read cycle. The cycle starts when BUS_BUSY goes high and SYNC_O, SDO are released from 3-state. SYNC_O is low at the start and rises to a high level t_{d13} ns after the falling edge of \overline{RD} . As shown in Figure 5, the MSB is shifted on the 2nd rising edge of the clock (2R). Other details about the data read cycle are discussed in the previous section (see Figure 3).

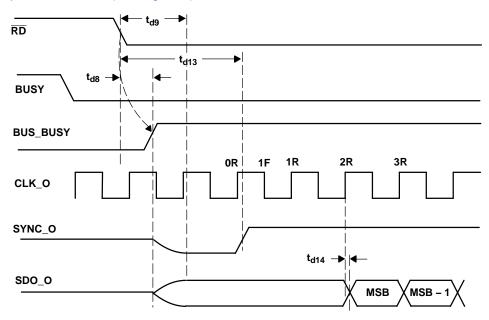


Figure 5. Start of Data Read Cycle with RD with CS Low and Device in Wait or Sample Phase

DATA READ CYCLE START AT END OF CONVERSION PHASE (Read Without Latency, Back-to-Back)

This mode is optimized for a data read immediately after the end of a conversion phase and ensures the data read is complete before the sample end while running at 2 MSPS. Point A in Figure 6 indicates 'pre_conversion_end'; it occurs t_{d19} ns before the falling edge of BUSY or $[(t_{d2} + t_{cnv} + t_{d4}) - t_{d19}]$ ns after the falling edge of \overline{CONVST} . A read cycle is initiated at point A if \overline{RD} is issued before point A while \overline{CS} is low. Alternately, \overline{RD} and \overline{CS} can be held low. At the start of the read cycle, BUS_BUSY rises to a high level and the LVDS outputs are released from 3-state. The rising edge of SYNC_O occurs t_{d12} ns after the conversion end. As shown in Figure 6, the MSB is shifted on the 2nd rising edge of the clock (2R). Other details about the data read cycle are discussed in the previous section (see Figure 3).



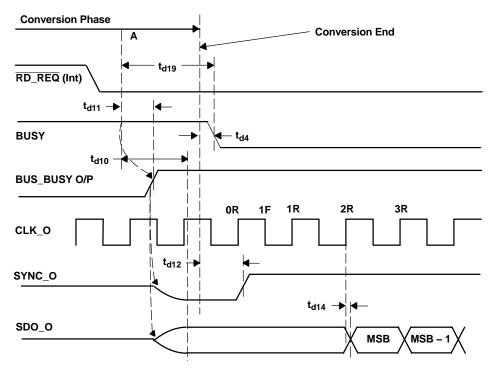


Figure 6. Start of Data Read Cycle with End of Conversion

DATA READ CYCLE END (With MODE $C/\overline{D} = 0$)

A data read cycle ends after all 16 bits have been serially latched out. Figure 7 shows the timing of the falling edge of BUS_BUSY and the rising edge of SYNC_O with respect to SDO. SYNC_O rises on the 16th rising edge of CLK_O. As shown in Figure 5 and Figure 6, the MSB is shifted out on the 2nd rising edge of CLK_O. Therefore, the LSB-1 is shifted out on the 16th rising edge of CLK_O.

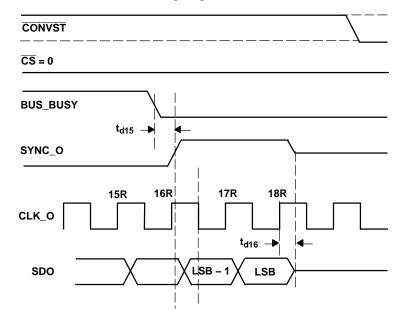


Figure 7. Data Read Cycle End with MODE $C/\overline{D} = 0$



The next two rising edges of CLK_O are shown as 17R and 18R in Figure 7. On 17R the LSB is latched out, and on 18R SDO and SYNC-O go to 3-state. Note that BUS_BUSY falls t_{d15} ns before the rising edge of SYNC_O when MODE $C/\overline{D} = 0$. Care must be taken not to allow LVDS bus usage by any other device until the end of the read cycle or $(t_{d15} + 2/t_{clk} + t_{d16})$ ns after the falling edge of BUS_BUSY.

DATA READ CYCLE END (With MODE $C/\overline{D} = 1$)

A data read cycle ends after all 16 bits have been serially latched out. Figure 8 shows the timing of the falling edge of BUS_BUSY and the rising edge of SYNCO with respect to SDO. SYNC_O rises on the 16th rising edge of CLK_O. As shown in Figure 5 and Figure 6, the MSB is shifted out on the 2nd rising edge of CLK_O. Therefore, the LSB-1 is shifted out on the 16th rising edge of CLK_O.

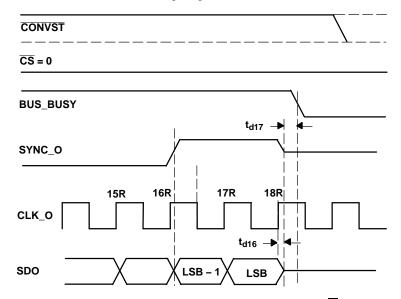


Figure 8. Data Read Cycle End with MODE $C/\overline{D} = 1$

The next two rising edges of CLK_O are shown as 17R and 18R in Figure 8. On 17R the LSB is latched out and on 18R the SDO and SYNC_O go in 3-state. In cascade mode (with MODE $C/\overline{D} = 1$) unlike daisy chain mode BUS_BUSY falling edge occurs after LVDS outputs are 3-state. One can use BUS_BUSY falling edge to allow the LVDS bus usage by any other device.

RESTRICTIONS ON READ CYCLE START

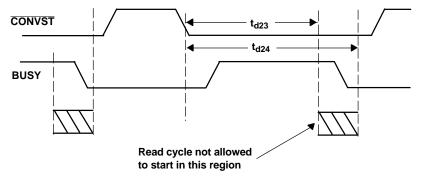


Figure 9. Read Cycle Restriction Region

The start of a data read cycle is not allowed in the region bound by t_{d23} and t_{d24} . Previous conversion results are available for a data read cycle start before this region, and current conversion results are available for a read cycle start after this region.



MULTIPLE DEVICES IN DAISY CHAIN OR CASCADE

Multiple devices can be connected in either a daisy chain or cascade configuration. The following sections describes detailed timing diagrams and electrical connections. The ADS8413 provides all of the hand-shake signals required for both of these modes. CONVST or CSTART is the only external signal needed for operation.

DAISY CHAIN

Figure 10 shows the first two devices in daisy chain. The signals shown by double lines are LVDS and the others are CMOS. Daisy chain mode is selected by setting MODE_C/ \overline{D} = 0. The first device in the chain is identified by selecting LAT_Y/ \overline{N} = 0.

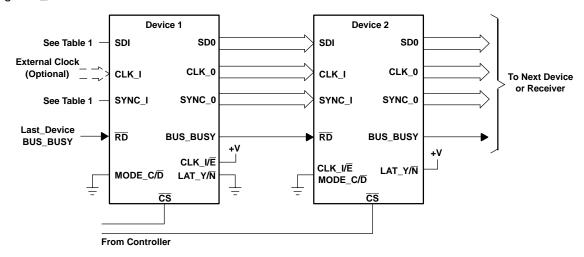


Figure 10. Connecting Multiple Devices in Daisy Chain

For all of the other devices in the chain LAT_Y/ \overline{N} = 1. See Table 1 for more details on device configurations. SDO, CLK_O, and SYNC_O of device n are to be connected to SDI, CLK_I, and SYNC_I of the n+1 device. SDO, CLK_O, and SYNC_O of the last device in the chain go to the receiver. BUS_BUSY of device n is connected to \overline{RD} of device n+1 and so on. Finally, BUS_BUSY of the last device in the chain is connected to \overline{RD} of device 1. This ensures the necessary handshake to seamlessly propagate the data of all devices through the chain (it is also allowed to tie \overline{RD} = 0 for device 1).

TIMING DIAGRAMS FOR DAISY CHAIN OPERATION

The conversion speed for n devices in the chain must be selected such that:

1/conversion speed > read startup delay + n*(data frame duration) + t_{d16}

Read startup delay = 10 ns + $(t_{d19} - t_{d4}) + t_{d12} + 2/f_{CLK}$

Data frame duration = 16/f_{CLK}

Note that it is not necessary for all devices in the chain to sample the data simultaneously. But all of the devices must operate with the same exact conversion speed.



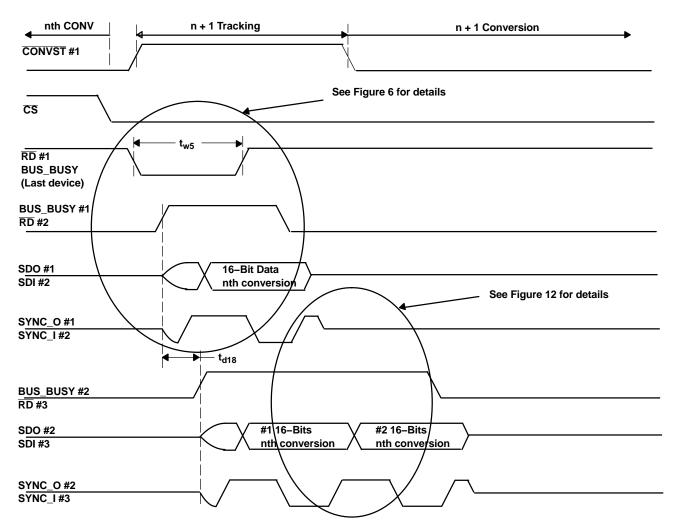


Figure 11. Data Read Operation for Devices in Daisy Chain

DATA READ OPERATION

On power up, BUS_BUSY of all of the devices is low. The devices receive $\overline{\text{CONVST}}$ or $\overline{\text{CSTART}}$ to sample and start the conversion. The first device in the chain starts the data read cycle at the end of its conversion. BUS_BUSY of device 1 (connected to $\overline{\text{RD}}$ of device 2) goes high on the read cycle start. Device 2 BUS_BUSY goes high on the rising edge of $\overline{\text{RD}}$. This propagates until the last device in the chain. Device 2 receives CLK_I, SDI, and SYNC_I from device 1 and it passes all of these signals to the next device. Device 2 (and every subsequent device in the chain) passes the received signals to its output until it sees the falling edge of RD (same as BUS_BUSY of the previous device). In daisy chain mode, BUS_BUSY for any device falls when it has passed all of the previous device data followed by its own data. The falling edge of BUS_BUSY occurs before the rising edge of SYNC_O. This indicates to the receiving device that the previous data chain is over and it is its own turn to output the data. The device outputs the data from the last completed conversion. BUS_BUSY of the last device in the chain is fed back to $\overline{\text{RD}}$ of the first device as shown in Figure 10 (or device 1 $\overline{\text{RD}}$ tied to 0). This makes sure that $\overline{\text{RD}}$ of device 1 is low before its conversion is over. The chain continues with only one external signal ($\overline{\text{CONVST}}$ or $\overline{\text{CSTART}}$) when $\overline{\text{CS}}$ is held low. Every device LVDS output goes to 3-state once all data transfer through the device has been completed.

 $\overline{\text{CS}}$ going high during the data read cycle of any device 3-states its SYNC_O and SDO. This halts the propagation of data through the chain. To reset this condition it is necessary to assert $\overline{\text{CS}}$ high for all devices. The new read sequence starts only after $\overline{\text{CS}}$ for all devices is low before point A as shown in Figure 6. The high pulse on $\overline{\text{CS}}$ must be at least 20 ns wide. It is better to connect $\overline{\text{CS}}$ of all of the devices together to avoid undesired halting of the daisy chain.



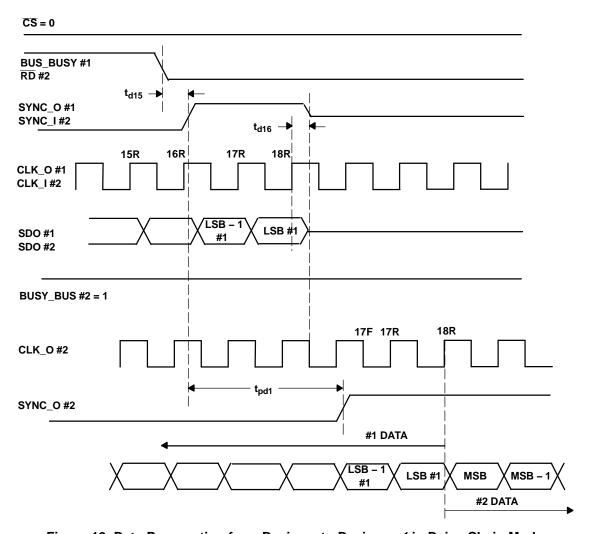


Figure 12. Data Propagation from Device n to Device n+1 in Daisy Chain Mode

As shown in Figure 12 there is a propagation delay of t_{pd1} from SYNC_I to SYNC_O or SDI to SDO. Note that the data frames of all devices in the chain appear seamless at the last device output. The rising edge of SYNC_O occurs at an interval of 16 clocks (or 8 clocks in BYTE mode); this can be used as a data frame sync. The deserializer at the output of the last device can shift the data on every falling edge of the clock and it can latch the parallel 16-bit word on the second rising edge of CLK_O (shown as 18R) after every rising edge of SYNC_O.

CASCADE

Figure 13 shows the cascade connection. The signals shown with double lines are LVDS and the others are CMOS. Cascade mode is selected by setting MODE_ $C/\overline{D}=1$. Similar to daisy chain, the first device in the chain is identified by selecting LAT_ $Y/\overline{N}=0$. For all other devices in the chain LAT_ $Y/\overline{N}=1$. See Table 1 for more details on device configuration. SDO, CLK_O, and SYNC_O are connected to the common bus. This means only one device occupies the bus at a time, while LVDS drivers for all other devices 3-state. Unlike SDO and SYNC_O, the clock cannot be switched out from device to device as the receiver requires a continuous clock. So only device 1 outputs the clock and CLK_O of all other devices is 3-stated by appropriately setting M1+ and M1-as listed in Table 1.



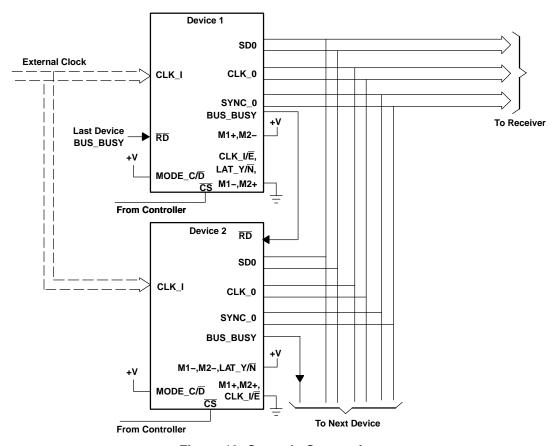


Figure 13. Cascade Connection

CLOCK SOURCE

In this mode it is very critical to control the skew between the three LVDS o/p signals. It is recommended to use external clock mode only for all of the devices in cascade. BUS_BUSY of device n is connected to \overline{RD} of device n + 1 and so on. Finally BUS_BUSY of the last device in the chain is to be connected to \overline{RD} of device 1. This ensures the necessary handshake to control the sequence of data reads for all of the devices in cascade. (It is also allowed to tie \overline{RD} to 0 for device 1.)

TIMING DIAGRAMS FOR CASCADE OPERATION

The conversion rate for n devices in cascade must be selected such that:

1/conversion speed > first device read cycle duration + (n - 1) next device read cycle duration

First device read cycle duration = read startup delay_1 + data frame duration + $(t_{d16} + t_{d17})$

Next device read cycle duration = read startup delay_n + data frame duration + $(t_{d16} + t_{d17})$

Read startup delay_1 = 10 ns + $(t_{d19} - t_{d4} + t_{d12}) + 2/f_{clk}$

Read startup delay_n = $(t_{d13} + 2/f_{clk})$

Data frame duration = 16/f_{clk}

Note that it is not necessary that all devices in the chain to sample the data simultaneously. But all of the devices must operate with the same exact conversion speed.



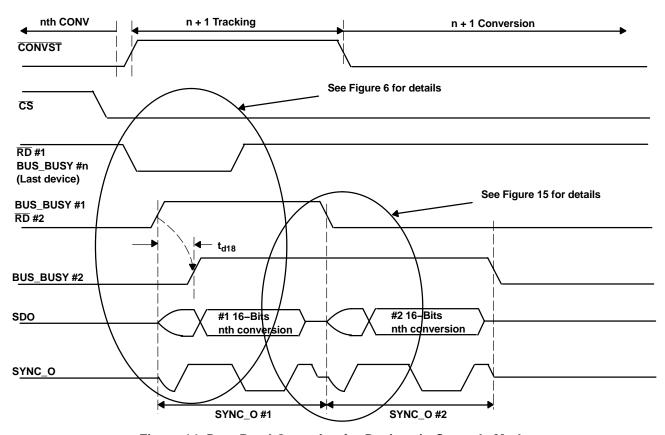


Figure 14. Data Read Operation for Devices in Cascade Mode

DATA READ OPERATION

On power up, BUS_BUSY for all of the devices is low. The devices receive CONVST or CSTART to sample and start the conversion. The first device starts the data read cycle at the end of its conversion. BUS_BUSY of device 1 (connected to RD of device 2) goes high on the read cycle start, indicating that it wants to occupy the bus. Device 2 BUS_BUSY goes high on the rising edge of RD. This propagates until the last device.

Device 1 BUS_BUSY goes low after it outputs its data, at this time SDO and SYNC_O for device 1 go to 3-state. The falling edge of BUS_BUSY (\overline{RD} of the next device) indicates to the next device that it is its turn to output the data. The next device outputs the data from the last completed conversion. BUS_BUSY of the last device goes low and its SYNC_O and SDO go to 3-state after it outputs its data. BUS_BUSY of the last device is fed back to \overline{RD} of the first device as shown in Figure 13 (\overline{RD} can also be tied to 0 for device 1). This ensures that \overline{RD} of device 1 is low before its conversion is over. The data read sequence continues with only one external signal, \overline{CONVST} or \overline{CSTART} , when $\overline{CS} = 0$. For any device, \overline{CS} high during the data read cycle 3-states SYNC_O and SDO of the device and halts the data read sequence. To reset this condition it is necessary to assert \overline{CS} high for all of the devices. The new read sequence starts only after \overline{CS} for all of the devices is low before point A as shown in Figure 6. The high pulse on \overline{CS} must be at least 20 ns wide. It is better to connect \overline{CS} for all of the devices together to avoid undesired halting of the data read sequence.



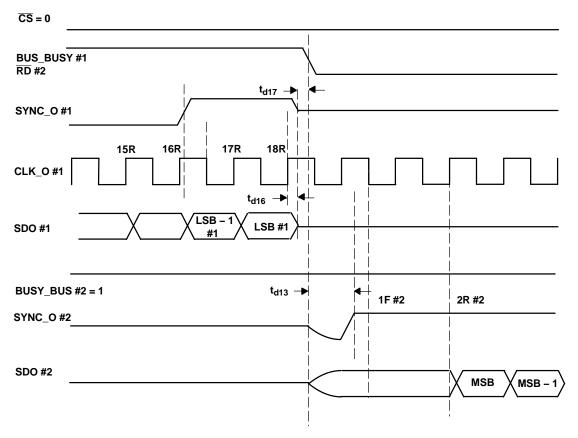


Figure 15. Device n Read Cycle End and Device n+1 Read Cycle Start

Unlike daisy chain, the data frames of all the devices in cascade are not seamless and there is a loss of time between one device 3-state to other device data valid due to wakeup time from 3-state and a two clock phase shift between SYNC and data (see Figure 15 for details). As a result, the number of data frames per second in this mode is less than in daisy chain mode. Also, a maximum of 4 devices can be cascaded on the same bus. But, I/O power per device is considerably lower in cascade as compared to daisy chain as each device LVDS o/p goes to 3-state after its data transfer. The deserializer at the output of the last device can shift the data on every clock falling edge, and it can latch the parallel 16-bit word on the second CLK_O rising edge (shown as 18R) after every SYNC_O rising edge.

THEORY OF OPERATION

The ADS8413 is a member of the high-speed successive approximation register (SAR) analog-to-digital converters family. The architecture is based on charge redistribution, which inherently includes a sample/hold function. The device includes a built-in conversion clock, internal reference, and 200-MHz LVDS serial interface. The device can be operated at maximum throughput of 2 MSPS.

ANALOG INPUT

An analog input is provided to two input pins: +IN and -IN. When a conversion is initiated, the voltage difference between these pins is sampled on the internal capacitor array. While a conversion is in progress, both inputs are disconnected from any internal function.



THEORY OF OPERATION (continued)

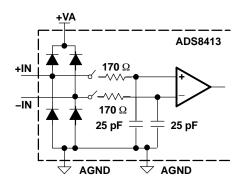


Figure 16. Simplified Input Circuit

When the converter enters hold mode, the voltage difference between the +IN and -IN inputs is captured on the internal capacitor array. The input current on the analog inputs depends upon a number of factors: sample rate, input voltage, signal frequency, and source impedance. Essentially, the current into the ADS8413 charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current (this may not happen when the signal is moving continuously). The source of the analog input voltage must be able to charge the input capacitance (25 pF) to better than a 16-bit settling level with a step input within the acquisition time of the device. For calculation, the step size can be selected equal to the maximum voltage difference between two consecutive samples at the maximum signal frequency (see the TYPICAL ANALOG INPUT CIRCUIT section). When the converter goes into hold mode, the input impedance is greater than $1G\Omega$.

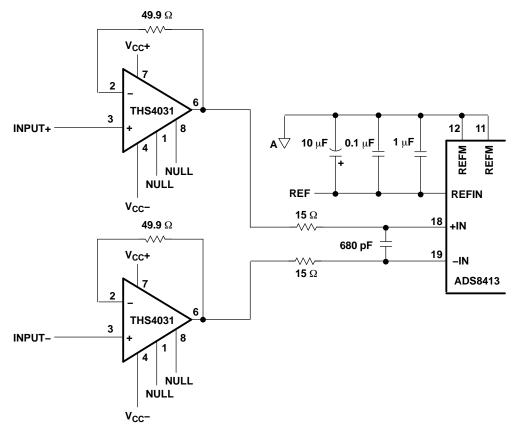


Figure 17. Typical Analog Input Schematic



THEORY OF OPERATION (continued)

Care must be taken regarding the absolute analog input voltage. To maintain the linearity of the converter, both -IN and +IN inputs should be within the limits specified. Outside of these ranges, the converter linearity may not meet specifications. Care should be taken to ensure that +IN and -IN see the same impedance to the respective sources. If this is not observed, the two inputs could have different setting times. This may result in offset error, gain error, and linearity error which changes with temperature and input voltage.

REFERENCE

The ADS8413 has a built-in 4.096-V (nominal value) reference. The ADS8413 can also operate with an external reference. When the internal reference is used, pin 14 (REFOUT) should be connected to pin 13 (REFIN), and a 0.1- μ F decoupling capacitor and 1- μ F storage capacitor must be connected between pin 14 (REFOUT) and pins 11 and 12 (REFM) (see Figure 18). The internal reference of the converter is buffered.

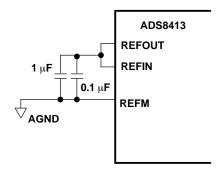


Figure 18. Using Internal Reference

The REFIN pin is also internally buffered. This eliminates the need to put a high bandwidth buffer onboard to drive the ADC reference and saves system area and power. When an external reference is used, the reference must be low noise, which can be achieved by the additional bypass capacitor from the REFIN pin to the REFM pin (see Figure 19). REFM must be connected to the analog ground plane.

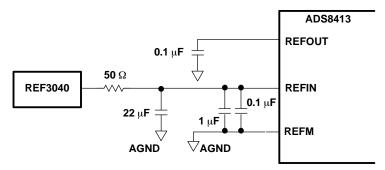


Figure 19. Using External Reference

DIGITAL INTERFACE

TIMING AND CONTROL

Refer to the timing diagrams and TIMING REQUIREMENTS table for detailed information.

SAMPLING AND CONVERSION

Sampling and conversion is controlled by the $\overline{\text{CONVST}}$ pin. For higher noise performance it is essential to have low jitter on the falling edge of $\overline{\text{CONVST}}$. The device uses the internally generated clock for conversion, hence it has a fixed conversion time.



THEORY OF OPERATION (continued)

READING DATA

The ADS8413 includes a high-speed LVDS serial interface. As discussed prior, an external clock (CLK_I, less than 200 MHz) or an internal 200-MHz clock can be used for a data read. The device outputs data in two's compliment format. Table 3 lists the ideal output codes.

Table 3. Ideal Input Voltages and Output Codes

DESCRIPTION	ANALOG VALUE (+IN – (-IN))	HEX CODE	
Full-scale range	2(+V _{ref})	_	
Least significant bit (LSB)	2(+V _{ref})/2 ¹⁶	_	
Full scale	V _{ref} – 1 LSB	7FFF	
Midscale	0 V	0000	
Midscale – 1LSB	0 V – 1 LSB	FFFF	
-Full scale	-V _{ref}	8000	



The restrictions on read cycle start are described in the section RESTRICTIONS ON READ CYCLE START (see Figure 9).

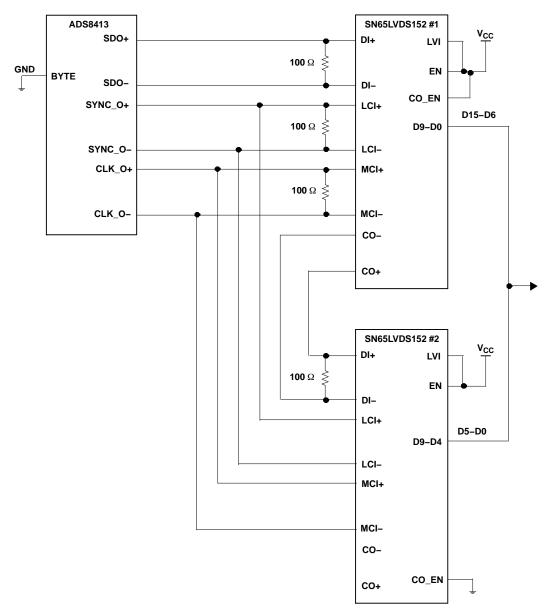


Figure 20. 16-Bit Data De-Serialization While BYTE = 0



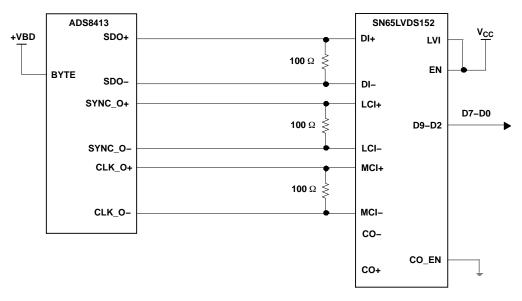


Figure 21. 8-Bit Data De-Serialization While BYTE = 1, Data

POWER SAVING

The converter provides two power saving modes, full powerdown and nap. Table 4 lists information on the activation/deactivation and resumption times for both modes.

POWERDOWN MODE	SDO	POWER CONSUMPTION	ACTIVATED BY	ACTIVATION TIME	RESUME POWER BY
Normal operation	Refer to DATA READ OPERATION section	58 mA	NA	NA	NA
Full powerdown (internal reference)	3 Stated	1 μΑ	$\overline{PD} = 0$	t _{d21}	PD = 1
Full powerdown (external reference)	3 Stated	1 μΑ	$\overline{PD} = 0$	t _{d21}	PD = 1
Nap powerdown	Not 3 stated	25 mA	Nap = 1	150 ns	Sample start

Table 4. Powerdown Modes

FULL POWERDOWN MODE

Full powerdown mode is activated by deasserting \overline{PD} = 0; the device takes t_{d21} ns to reach the full powerdown state. The device can return to normal mode from full powerdown by asserting \overline{PD} = 1. The powerup sequence is different for device operation with an internal reference or external reference as shown in Figure 22 and Figure 23.



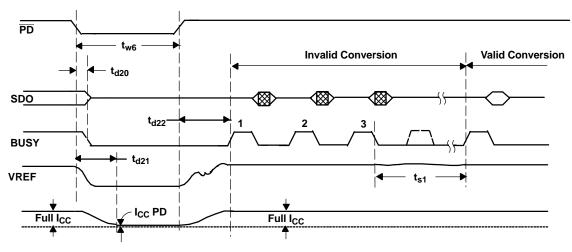


Figure 22. Device Full Powerdown and Powerup Sequence with Device Operation in Internal Reference Mode

When an internal reference is used, a conversion can be started t_{d22} ns after asserting $\overline{PD} = 1$. After the first three conversions, t_{s1} ns are required for reference voltage settling to the trimmed value. Any conversions after this provide data at the specified accuracy.

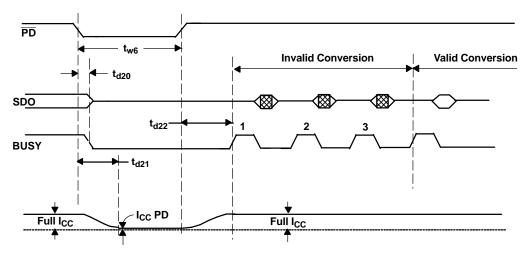


Figure 23. Device Full Powerdown and Powerup Sequence with Device Operation in External Reference Mode

When an external reference is used, a conversion can be started t_{d22} n after asserting \overline{PD} = 1. The first three conversions are required for internal circuit stabilization. Any conversions after this provide data at the specified accuracy.

NAP MODE

The device automatically enters the nap state if nap = 1 at end of a conversion, and it remains in the nap state until the start of the sampling phase. A minimum of 150 ns is required after a sample start for the device to come out of the nap state and to perform normal sampling. So the minimum sampling time needed for nap mode is $t_{acq(min)} + 150$ ns, or the maximum conversion speed in nap mode is 1.5 MHz.



LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS8413 circuitry. The device offers single-supply operation, and it is often used in close proximity with digital logic, FPGA, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it is to achieve good performance from the converter.

The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to the end of sampling and just prior to latching the output of the analog comparator during the conversion phase. Such glitches might originate from switching power supplies, nearby digital logic, or high power devices. Noise during the end of sampling and the later half of a conversion must be kept to a minimum (the former half of a conversion is not very sensitive since the device uses a proprietary error correction algorithm to correct for transient errors during this period).

The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. On average, the device draws very little current from an external reference as the reference voltage is internally buffered. If the reference voltage is external and originates from an op amp, make sure that it can drive the bypass capacitor or capacitors without oscillation. A 0.1- μF bypass capacitor and 1- μF storage capacitor are recommended from REFIN directly to REFM.

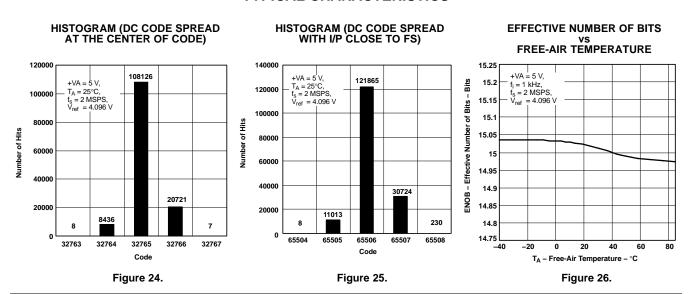
The AGND and BDGND pins should be connected to a clean ground point. In all cases, this should be the analog ground. Avoid connections that are too close to the grounding point of a microcontroller or digital signal processor. If required, run a ground trace directly from the converter to the power supply entry point. The ideal layout consists of an analog ground plane dedicated to the converter and associated analog circuitry.

As with the AGND connections, +VA should be connected to a +5-V power supply plane that is separate from the connection for +VBD and digital logic until they are connected at the power entry point onto the PCB. Power to the ADC should be clean and well bypassed. A 0.1- μ F ceramic bypass capacitor should be placed as close to the device as possible. See Table 5 for the placement of the capacitor. In addition to the 0.1- μ F capacitor, a 1- μ F capacitor is recommended. In some situations, additional bypassing may be required, such as a 100- μ F electrolytic capacitor or even a Pi filter made up of inductors and capacitors; all designed to essentially low-pass filter the +5-V supply, thus removing the high frequency noise.

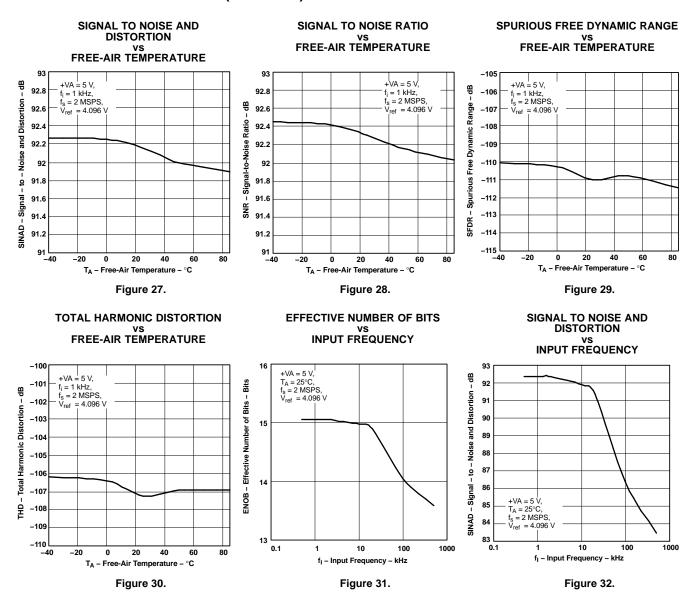
Table 5. Power Supply Decoupling Capacitor Placement

POWER SUPPLY PLANE	CONVERTER ANALOG SIDE	CONVERTER DIGITAL SIDE	
SUPPLY PINS			
Pair of pins require a shortest path to decoupling capacitors	(9,10) (16,17) (20,21) (22,23) (26,27 or 25,26) (36,37)	(44,45)	

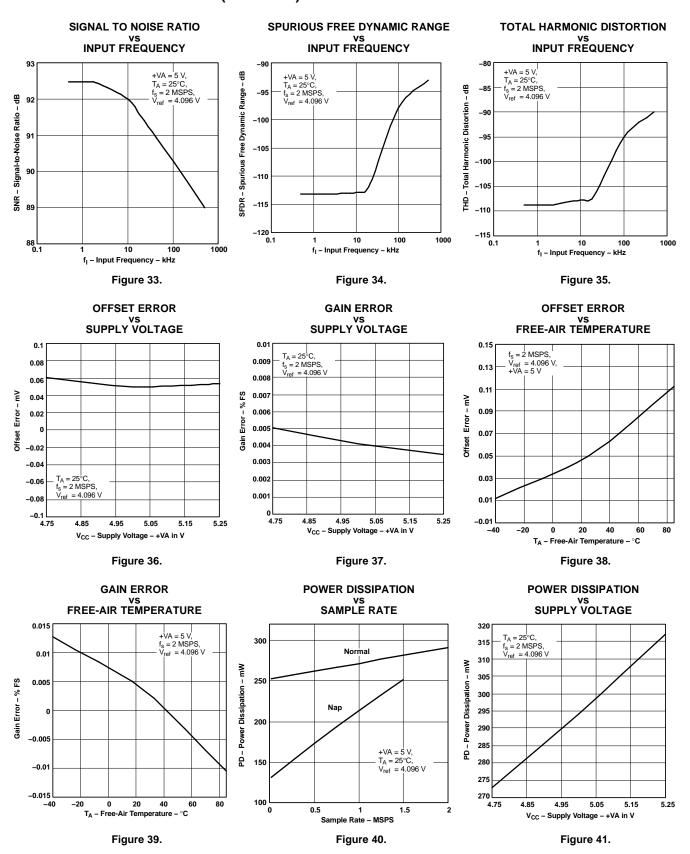
TYPICAL CHARACTERISTICS



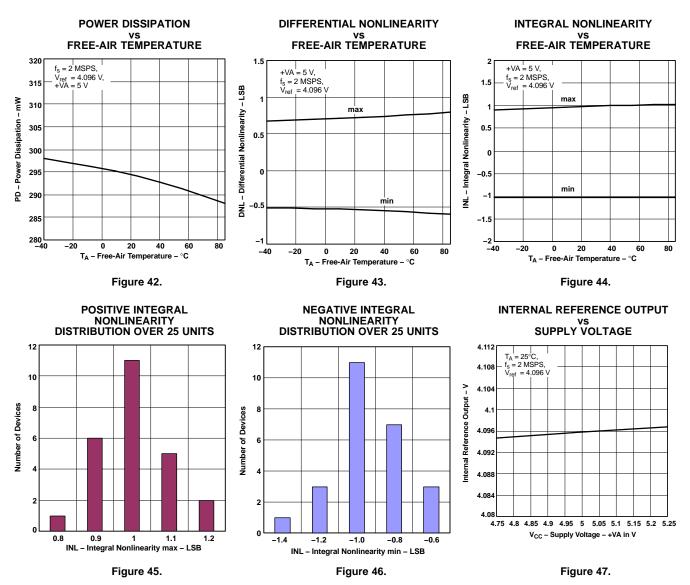








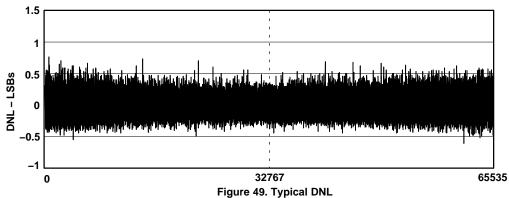






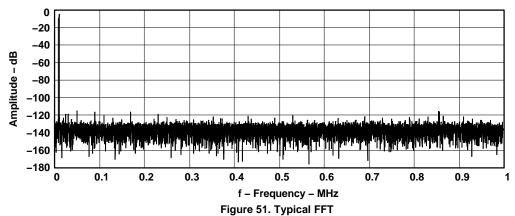
INTERNAL REFERENCE OUTPUT

 T_A – Free-Air Temperature – °C Figure 48.



2 1.5 1 0.5 0 -0.5 -1 -1.5 -2 0 32767 65535 Figure 50. Typical INL





PARAMETER MEASUREMENT INFORMATION

DRIVER

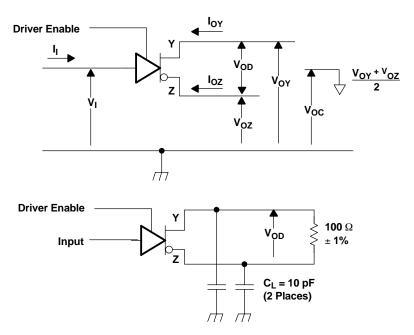


Figure 52. Driver Voltage and Current Definitions



PARAMETER MEASUREMENT INFORMATION (continued)

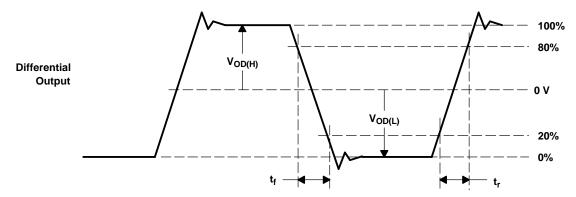


Figure 53. Timing and Voltage Definitions of the Differential Output Signal

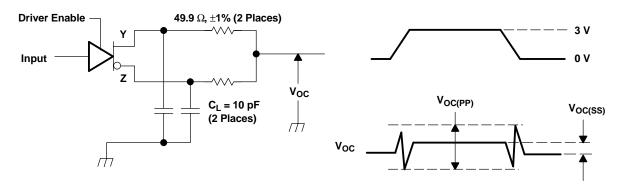


Figure 54. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

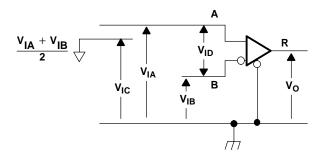


Figure 55. Receiver Voltage Definitions

www.ti.com 11-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
ADS8413IBRGZT	Active	Production	VQFN (RGZ) 48	250 SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	ADS8413I B
ADS8413IBRGZT.B	Active	Production	VQFN (RGZ) 48	250 SMALL T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	ADS8413I B

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4224671/A



PLASTIC QUADFLAT PACK- NO LEAD



NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



PLASTIC QUADFLAT PACK- NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUADFLAT PACK- NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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