

# ADS8284 18-BIT, 1-MSPS, Pseudo-Bipolar Differential SAR ADC with On-Chip ADC Driver (OPA) and 4-Channel Differential Multiplexer

#### **Features**

- 1.0-MHz Sample Rate, Zero Latency at Full Speed
- 18-Bit Resolution
- Supports Pseudo-Bipolar Differential Input Range: -4 V to +4 V with 2-V Common-Mode
- Built-In Four Channel, Differential Ended Multiplexer; with Channel Count Selection and Auto/Manual Mode
- On-Board Differential ADC Driver (OPA)
- Buffered Reference Output to Level Shift Bipolar ±4-V Input with External Resistance Divider
- Reference/2 Output to Set Common-Mode for External Signal Conditioner
- 18-/16-/8-Bit Parallel Interface
- SNR: 98.4dB Typ at 2-kHz I/P
- THD: -119dB Typ at 2-kHz I/P
- Power Dissipation: 331.25 mW at 1 MSPS Including ADC Driver
- Internal Reference
- Internal Reference Buffer
- 64-Pin QFN Package

### **Applications**

- Medical Imaging/CT Scanners
- **Automated Test Equipment**
- **High-Speed Data Acquisition Systems**
- High-Speed Closed-Loop Systems

#### 3 Description

The ADS8284 is a high-performance analog systemon-chip (SoC) device with an 18-bit, 1-MSPS A/D converter, 4-V internal reference, an on-chip ADC driver (OPA), and a 4-channel differential multiplexer. The channel count of the multiplexer and auto/manual scan modes of the device are user selectable.

The ADC driver is designed to leverage the very high noise performance of the differential ADC at optimum power usage levels.

The ADS8284 outputs a buffered reference signal for level shifting of a ±4-V bipolar signal with an external resistance divider. A V<sub>ref</sub>/2 output signal is available to set the common-mode of a signal conditioning circuit. The device also includes an 18-/16-/8-bit parallel interface.

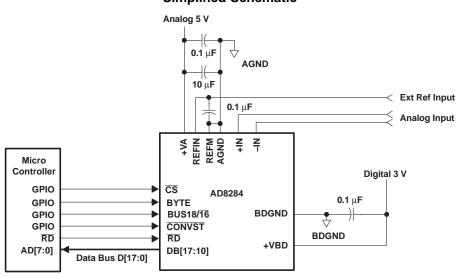
The ADS8284 is available in a 9 mm x 9 mm, 64-pin QFN package and is characterized from -40°C to 85°C.

#### **Device Information (1)**

DEVICE NAME	PACKAGE	BODY SIZE
ADS8284	QFN (64)	9mm x 9mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Simplified Schematic







## **Table of Contents**

1	Features 1		6.10 Typical Characteristics	19
2	Applications 1	7	Device Description	30
3	Description 1		7.1 Overview	30
4	Revision History2		7.2 Functional Block Diagram	30
5	Pin Configuration and Function3		7.3 Feature Description	31
6	Specifications6		7.4 Device Functional Modes	32
•	6.1 Absolute Maximum Ratings6	8	Application and Implementation	33
	6.2 Handling Ratings		8.1 Application Information	
	6.3 Recommended Operating Conditions		8.2 Typical Applications	33
	6.4 Thermal Information	9	Power Supply Recommendations	36
	6.5 Electrical Characteristics	10	Device and Documentation Support	37
	6.6 Timing Requirements, 5 V		10.1 Trademarks	37
	6.7 Timing Requirements, 3 V		10.2 Electrostatic Discharge Caution	37
	6.8 Multiplexer Timing Requirements		10.3 Glossary	37
	6.9 Timing Diagrams	11	Mechanical, Packaging, and Orderable Information	37

## 4 Revision History

CI	hanges from Original (March 2009) to Revision A	Page
•	Changed the data sheet to the new TI standard	
•	Added the Device Information table	·
•	Added the Handling Ratings table	(
•	Added Reference/2 Voltage Range to the Electrical Characteristics table	
•	Added the Power Supply Recommendations section	36



SLAS628A - MARCH 2009 - REVISED APRIL 2014

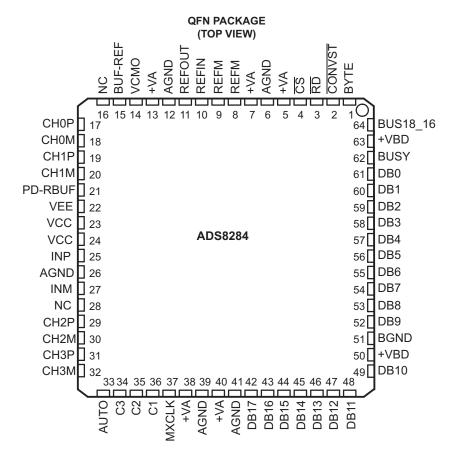
#### **Device Comparison Table**

TYPE/SPEED	500 kHz	~600 kHz	750 kHz	1 MHz	1.25 MHz	2 MHz	3 MHz	4MHz
18-Bit Pseudo-Diff	ADS8383	ADS8381		ADS8481				
16-Bit Fseudo-Dill		ADS8380 (s)						
10.57.5		ADS8382 (s)		ADS8284	ADS8484			
18-Bit Pseudo-Bipolar, Fully Diff				ADS8482				
	ADS8327	ADS8370 (s)	ADS8371	ADS8471	ADS8401	ADS8411		
16-Bit Pseudo-Diff	ADS8328				ADS8405	ADS8410 (s)		
	ADS8319							
16 Pit Dooudo Pipolor Fully Diff	ADS8318	ADS8372 (s)		ADS8472	ADS8402	ADS8412		ADS8422
16-Bit Pseudo-Bipolar, Fully Diff				ADS8254	ADS8406	ADS8413 (s)		
14-Bit Pseudo-Diff					ADS7890 (s)		ADS7891	
12-Bit Pseudo-Diff				ADS7886		ADS7883		ADS7881

#### **Device Linearity**

MODEL	MAXIMUM INTEGRAL LINEARITY (LSB)	MAXIMUM DIFFERENTIAL LINEARITY (LSB)	NO MISSING CODES AT RESOLUTION (BIT)
ADS8284IB	±2.5	+1.5/–1	18
ADS8284I	±4.5	+1.5/–1	18

## 5 Pin Configuration and Function





### **Pin Functions**

	PIN FUNCTIONS								
NO	PIN	I/O		DESCRIPTION					
NO MULTIP	NAME LEXER INPUT	DIME							
WIOLTIP	LEXEK INPUT	PINS	Non inverting analog in	anut for differential mu	ultiplayer shapped pu	umbor O. Dovido porfo	ermanas is antimiza	d for EO O course	
17	CH0P	I	Non-inverting analog ir impedance at this inpu	t.	•				
18	СНОМ	I	Inverting analog input f impedance at this inpu		exer channel numbe	er 0. Device performa	nce is optimized for	50-Ω source	
19	CH1P	I	Non-inverting analog ir impedance at this inpu		ultiplexer channel nu	umber 1. Device perfo	ormance is optimize	d for 50-Ω source	
20	CH1M	I	Inverting analog input fi		exer channel numbe	r 1. Device performa	nce is optimized for	50-Ω source	
29	CH2P	I	Non-inverting analog ir impedance at this inpu		ultiplexer channel nu	umber 2. Device perfo	ormance is optimize	d for 50-Ω source	
30	CH2M	I	Inverting analog input f		exer channel numbe	r 2. Device performa	nce is optimized for	50-Ω source	
31	CH3P	ı	Non-inverting analog ir impedance at this inpu	nput for differential mu	ultiplexer channel nu	umber 3. Device perfo	ormance is optimize	d for 50 ohm source	
32	СНЗМ	I	Inverting analog input fi	or differential multiple	exer channel numbe	r 3. Device performa	nce is optimized for	50-Ω source	
ADC INF	PUT PINS		impedance at this inpu						
25	INP	J	ADC Non inverting input	ut connect 1-nF can	acitor across INP ar	nd INM			
27	INM	i	ADC Inverting input, co						
	ENCE INPUT/	OUTPUT	0 .	Supuoitoi	and in				
8, 9	REFM	1	Reference ground.						
10	REFIN	i	Reference Input. Add (	).1-uF decoupling car	pacitor between REI	FIN and REFM.			
11	REFOUT	0	Reference Output. Add				en internal reference	e is used	
14	VCMO	0	This pin outputs REFIN	· · ·				, 10 40041	
15	BUF-REF	0	Buffered reference out						
	CONTROL PI		24.10.04.10.010.100.04.	Patr 0001a. to 10101 of	s.po.a. o.ga.o a.	sing external recipiers	-		
21	PD-RBUF	1	High on this pin powers	s down the reference	huffer (BLIF-RFF)				
	LEXER CONT	ROI PIN		o down the releighed	banor (Bor IVE).				
33	AUTO	1	High level on this pin s	elects auto mode for	multiplexer scannin	a. Low level selects n	nanual mode of mu	Itinlexer scanning	
34	C3	ı	In auto mode (AUTO =	1) multiplexer chann					
35	C2	ı	Acts as multiplexer add multiplexer channel (ch	dress bit when AUTO			O = 1) C2 and C1 s	elect the last	
36	C1	I	Acts as multiplexer add	dress LSB when AUT	O = 0 (manual mod	e). In auto mode (AU	TO = 1) C2 and C1	select the last	
			multiplexer channel (ch Multiplexer channel is				auto or manual mo	de. Device BUSY	
37	MXCLK	I	output can be connected						
ADC DA	TA BUS			8-BIT BUS		16-BIT	BUS	18-BIT BUS	
42-49,	Data Bus		BYTE = 0	BYTE = 1	BYTE = 1	BYTE = 0	BYTE = 0	BYTE = 0	
52-61			BUS18/16 = 0	BUS18/16 = 0	BUS18/16 = 1	BUS18/16 = 0	BUS18/16 = 1	BUS18/16 = 0	
42	DB17	0	D17 (MSB)	D9	All ones	D17 (MSB)	All ones	D17 (MSB)	
43	DB16	0	D16	D8	All ones	D16	All ones	D16	
44	DB15	0	D15	D7	All ones	D15	All ones	D15	
45	DB14	0	D14	D6	All ones	D14	All ones	D14	
46	DB13	0	D13	D5	All ones	D13	All ones	D13	
47	DB12	0	D12	D4	All ones	D12	All ones	D12	
48	DB11	0	D11	D3	D1	D11	All ones	D11	
49	DB10	0	D10	D2	D0 (LSB)	D10	All ones	D10	
52	DB9	0	D9	All ones	All ones	D9	All ones	D9	
53	DB8	0	D8	All ones	All ones	D8	All ones	D8	
54	DB7	0	D7	All ones	All ones	D7	All ones	D7	
55	DB6	0	D6	All ones	All ones	D6	All ones	D6	
56	DB5	0	D5	All ones	All ones	D5	All ones	D5	
50	טטט	J	20	7 til OHE3	7 dl 01163	20	7 dl 01163	23	

Product Folder Links: ADS8284

Submit Documentation Feedback

Copyright © 2009–2014, Texas Instruments Incorporated



SLAS628A -MARCH 2009-REVISED APRIL 2014

## Pin Functions (continued)

PIN					DECC	NIDTION			
NO	NAME	1/0		DESCRIPTION					
57	DB4	0	D4	All ones	All ones	D4	All ones	D4	
58	DB3	0	D3	All ones	All ones	D3	D1	D3	
59	DB2	0	D2	All ones	All ones	D2	D0 (LSB)	D2	
60	DB1	0	D1	All ones	All ones	D1	All ones	D1	
61	DB0	0	D0 (LSB)	All ones	All ones	D0 (LSB)	All ones	D0 (LSB)	
ADC CO	NTROL PINS								
62	BUSY	0	Status output. This pin	is held high when de	vice is converting.				
64	BUS18_16	1	Bus size select input. U	Ised for selecting 18-	bit or 16-bit wide bu	us transfer. Refer to A	ADC DATA BUS de:	scription above.	
1	BYTE	_	Byte Select Input. Used	I for 8-bit bus reading	g. Refer to ADC DA	TA BUS description a	above.		
2	CONVST	1	Convert start. This input	t is active low and ca	an act independent	of the $\overline{CS}$ input.			
3	RD	_	Synchronization pulse t	or the parallel output					
4	CS	- 1	Chip select.						
DEVICE	POWER SUPI	PLIES							
22	VEE		Negative supply for OP	A (OP1, OP2)					
23, 24	VCC		Positive supply for OPA	(OP1, OP2, BUF-RI	EF)				
5, 7, 13, 38, 40	+VA		Analog power supply.						
6, 12, 26, 39, 41	AGND		Analog ground.						
50, 63	+VBD		Digital power supply for	Digital power supply for ADC bus.					
51	BGND		Digital ground for ADC	bus interface digital s	supply.				
NOT CO	NNECTED PIN	IS							
16, 28	NC		No connection.						



### 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
CH(i) to AGND (both P and M inputs)	VEE-0.3	VCC + 0.3	V
VCC to VEE	-0.3	18	V
+VA to AGND	-0.3	7	V
+VBD to BDGND	-0.3	7	V
ADC control digital input voltage to GND	-0.3	(+VBD + 0.3)	V
ADC control digital output to GND	-0.3	(+VBD + 0.3)	V
Multiplexer control digital input voltage to GND	-0.3	(+VA + 0.3)	V
Power control digital input voltage to GND	-0.3	(+VCC + 0.3)	V
Operating temperature range	-40	85	°C
Junction temperature (T <sub>J</sub> max)		150	°C

<sup>(1)</sup> Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### 6.2 Handling Ratings

			MIN	MAX	UNIT
T <sub>stg</sub>	Storage temperature rang	orage temperature range			
V <sub>(ESD)</sub> Electrostatic disc	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)		2	kV
	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	-500	500	V

<sup>(1)</sup> JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

#### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Analog Input at Multiplexer Inputs	CHxP, CHxM	0		$V_{REF}$	V
Digital Supply Voltage	+VBD	2.7	3.3	5.25	V
Analog Supply Voltage	+VA	4.75	5	5.25	V
Positive Supply Voltage for OPA	VCC	4.75	5	7.5	V
Negative Supply Voltage for OPA	VEE	-7.5	-5	-3	V

#### 6.4 Thermal Information

	THERMAL METRIC <sup>(1)</sup>	RCG	LINUT
	THERMAL METRIC	64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	24.0	
R <sub>0JC(top)</sub>	Junction-to-case(top) thermal resistance	7.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	3.2	°C // //
ΨЈТ	Junction-to-top characterization parameter	0.1	°C/W
ΨЈВ	Junction-to-board characterization parameter	3.2	
R <sub>0JC(bottom)</sub>	Junction-to-case(bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

<sup>(2)</sup> JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

www.ti.com

### 6.5 Electrical Characteristics

 $T_A = -40$ °C to 85°C, VCC = 5 V, VEE = -5 V, +VA = 5 V, +VBD = 5 V or 3.3 V,  $V_{ref} = 4$  V,  $f_{SAMPLE} = 1$  MSPS (unless otherwise noted)

PARA	METER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT		'				
Full-scale input voltage at m	nultiplexer input <sup>(1)</sup>	CH(i)P-CH(i)M	-V <sub>ref</sub>		$V_{ref}$	V
Absolute input range at mul	tiplexer input	CH (i)	-0.2		V <sub>ref</sub> + 0.2	V
Input common-mode voltage	e	[CH(i)P + CH(i)M] /2	(V <sub>ref</sub> )/2 - 0.2	(V <sub>ref</sub> )/2	(V <sub>ref</sub> )/2 + 0.2	٧
SYSTEM PERFORMANCE		<u> </u>	+			
Resolution				18		Bits
	ADS8284IB		18			
No missing codes	ADS8284I		18			Bits
(0)	ADS8284IB		-2.5	±1.25	2.5	(0)
Integral linearity (2)	ADS8284I		-4.5	±1.5	4.5	LSB (3)
	ADS8284IB		-1	±0.6	1.5	(2)
Differential linearity	ADS8284I	At 18-bit level	-1	±0.6	1.5	LSB <sup>(3)</sup>
	ADS8284IB		-0.5	±0.05	0.5	
Offset error	ADS8284I		-0.5	±0.05	0.5	mV
	ADS8284IB		-0.1	±0.025	0.1	
Gain error <sup>(4)</sup>	ADS8284I	External reference	-0.1	±0.025	0.1	%FS
DC power supply rejection ratio		At 3FFF0 <sub>H</sub> output code. For +VA or VCC, VEE variation of 0.5 V individually	011	80	<u> </u>	dB
SAMPLING DYNAMICS		,				
		+VBD = 5 V		625	650	ns
Conversion time		+VDB = 3 V		625	650	ns
		+VBD = 5 V	320	350		ns
Acquisition time		+VDB = 3 V	320	350		
Maximum throughput rate					1.0	MHz
Aperture delay				4		ns
Aperture jitter				5		ps
r		For ADC only		150		ns
Settling time to 0.5 LSB		For OPA (OP1, OP2) + mux		700		
Over voltage recovery		For ADC only		150		ns
DYNAMIC CHARACTERIS	TICS	,,				
	ADS8284I			-119		
	ADS8284IB	$V_{IN} = 4 V_{pp}$ at 2 kHz		-119		dB
Total harmonic distortion	ADS8284I			-105		
(THD) <sup>(5)</sup>	ADS8284IB	$V_{IN} = 4 V_{pp}$ at 10 kHz		-105		dB
	ADS8284I	V 4V =+400 HI=		-100		
	ADS8284IB	$V_{IN} = 4 V_{pp}$ at 100 kHz, LoPWR = 0		-100		dB
	ADS8284I			98.4		
	ADS8284IB	$V_{IN} = 4 V_{pp}$ at 2 kHz	97.5	98.4		dB
	ADS8284I		31.3	98		
Signal-to-noise ratio (SNR)	ADS8284IB	$V_{IN} = 4 V_{pp}$ at 10 kHz		98		dB
	ADS8284I			95		
		$V_{IN} = 4 V_{pp}$ at 100 kHz, LoPWR = 0				dB
	ADS8284IB	LUFWK = U		97		

<sup>(1)</sup> Ideal input span, does not include gain or offset error.

<sup>(2)</sup> This is endpoint INL, not best fit.

<sup>(3)</sup> LSB means least significant bit.

<sup>(4)</sup> Calculated on the first nine harmonics of the input frequency.

<sup>(5)</sup> Measured relative to acutal measured reference.



## **Electrical Characteristics (continued)**

 $T_A = -40$ °C to 85°C, VCC = 5 V, VEE = -5 V, +VA = 5 V, +VBD = 5 V or 3.3 V,  $V_{ref} = 4$  V,  $f_{SAMPLE} = 1$  MSPS (unless otherwise noted)

PARA	METER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	ADS8284I	V 4V (2)		98.3		ı.
	ADS8284IB	$V_{IN} = 4 V_{pp}$ at 2 kHz		98.3		dB
Signal-to-noise + distortion	ADS8284I	V 4V 440111		97.2		in.
(SINAD)	ADS8284IB	$V_{IN} = 4 V_{pp}$ at 10 kHz		97.2		dB
	ADS8284I	$V_{IN} = 4 V_{pp}$ at 100 kHz,		93.8		ın
	ADS8284IB	LoPWR = 0		95.23		dB
	ADS8284I	V 4V (2111		121		ın
	ADS8284IB	$V_{IN} = 4 V_{pp}$ at 2 kHz		121		dB
Spurious free dynamic	ADS8284I	V 4V 4044		106		
range (SFDR)	ADS8284IB	$V_{IN} = 4 V_{pp}$ at 10 kHz		106		dB
	ADS8284I	$V_{IN} = 4 V_{pp}$ at 100 kHz,		101		
	ADS8284IB	LoPWR = 0		101		dB
-3dB small signal bandwidtl	h			8		MHz
VOLTAGE REFERENCE IN	IPUT (REFIN)					
Reference voltage at REFIN			3.0	4.096	+VA - 0.8	V
Reference input current (6)				1	1	μA
INTERNAL REFERENCE C	OUTPUT (REFOUT)		I.			
Internal reference start-up ti	me	From 95% (+VA), with 1-µF storage capacitor			120	ms
Reference voltage range, V	ref		4.081	4.096	4.111	V
Source current	···	Static load			10	μA
Line regulation		+VA = 4.75 V to 5.25 V	60			<u>.</u> μV
Drift		I <sub>O</sub> = 0		±6		PPM/°C
BUFFERED REFERENCE	OUTPUT (BUF-REF)					
Output current		REFIN = 4 V, at 85°C		70		mA
REFERENCE/2 OUTPUT (\	/CMO)	·				
Reference/2 Voltage Range		At No Load on VCMO	1.938	2.048	2.158	V
Output current		REFIN = 4 V, at +85°C	50			μA
ANALOG MULTIPLEXER		· · · · · · · · · · · · · · · · · · ·				
Number of channels					4	
Channel to channel crosstal	lk	100 kHz i/p		-95		dB
Channel selection		Auto sequencer with selection of channel count or manual selection through control lines				
DIGITAL INPUT-OUTPUT		-				
ADC CONTROL PINS						
Logic Family-CMOS						
<u> </u>	V <sub>IH</sub>	Ι <sub>ΙΗ</sub> = 5 μΑ	+V <sub>BD</sub> -1		+V <sub>BD</sub> + 0.3	V
	V <sub>IL</sub>	I <sub>IL</sub> = 5 μA	0.3		0.8	V
Logic level	V <sub>OH</sub>	I <sub>OH</sub> = 2 TTL loads	+V <sub>BD</sub> -0.6		+V <sub>BD</sub>	V
	V <sub>OL</sub>	I <sub>OL</sub> = 2 TTL loads	0		0.4	V
MULTIPLEXER CONTROL		<del></del>	-			
Logic Family - CMOS						
	I <sub>IH</sub>	Ι <sub>ΙΗ</sub> = 5 μΑ	2.3		+VA +0.3	V
Logic level I <sub>IL</sub>		I <sub>IL</sub> = 5 μA			0.8	V
POWER CONTROL PINS	IL.	in the same	1 0.0		5.0	•
Logic Family - CMOS						
Logic I allilly - CiviO3	V	I <sub>IH</sub> = 5 μA	2.3		+VA +0.3	V
Logic level	V <sub>IH</sub>		-0.3		0.8	V
	V <sub>IL</sub>	$I_{IL} = 5 \mu A$	-0.3		0.8	V

(6) Can vary ±20%

Submit Documentation Feedback

Copyright © 2009–2014, Texas Instruments Incorporated

www.ti.com

## **Electrical Characteristics (continued)**

 $T_A = -40$ °C to 85°C, VCC = 5 V, VEE = -5 V, +VA = 5 V, +VBD = 5 V or 3.3 V,  $V_{ref} = 4$  V,  $f_{SAMPLE} = 1$  MSPS (unless otherwise noted)

PAR	AMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER	SUPPLY REQUIREMENTS					
	+VBD		2.7	3.3	5.25	V
Dawer augustus seltaga	+VA		4.75	5	5.25	V
Power supply voltage	VCC		4.75	5	7.5	V
	VEE		-7.5	-5	-3	V
ADC driver positive supply (VCC) current (for OP1 and OP2 together)		VCC = +5, VEE = -5V, CH0 - CH3 p and m inputs shorted to each other and connected to 2V		11.65		mA
ADC driver negative supply ( VEE) current (for OP1 and OP1 together)		VCC= +5V, CH0 - CH3 p and m inputs shorted to each other and connected to 2V		9.6		mA
+VA supply current, 1-MF	Iz sample rate			45	50	mA
Reference buffer (BUF-REF) supply current (VCC to GND)		VCC= +5, PD-RBUF = 0, Quiescent current		8		mA
		VCC = 5, PD-RBUF = 1 <sup>(7)</sup>		10		μA
TEMPERATURE RANGE					'	
Operating free-air			-40		85	°C

<sup>(7)</sup> PD-RBUF = 1 powers down the reference buffer (BUF-REF), note that it does not 3-state the BUF-REF output.



## 6.6 Timing Requirements, 5 V

All specifications typical at  $-40^{\circ}$ C to  $85^{\circ}$ C,  $+VA = +VBD = 5 V^{(1)} (2) (3)$ 

	PARAMETER	MIN	TYP	MAX	UNIT
t <sub>(CONV)</sub>	Conversion time			650	ns
t <sub>(ACQ)</sub>	Acquisition time	320			ns
t <sub>(HOLD)</sub>	Sample capacitor hold time			25	ns
t <sub>pd1</sub>	CONVST low to BUSY high			40	ns
t <sub>pd2</sub>	Propagation delay time, end of conversion to BUSY low			15	ns
t <sub>pd3</sub>	Propagation delay time, start of convert state to rising edge of BUSY			15	ns
t <sub>w1</sub>	Pulse duration, CONVST low	40			ns
t <sub>su1</sub>	Setup time, $\overline{\text{CS}}$ low to $\overline{\text{CONVST}}$ low	20			ns
t <sub>w2</sub>	Pulse duration, CONVST high	20			ns
	CONVST falling edge jitter			10	ps
t <sub>w3</sub>	Pulse duration, BUSY signal low	t <sub>(ACQ)</sub> min			ns
t <sub>w4</sub>	Pulse duration, BUSY signal high	, ,		650	ns
t <sub>h1</sub>	Hold time, first data bus transition (RD low, or CS low for read cycle, or BYTE or BUS18/16 input changes) after CONVST low	40			ns
t <sub>d1</sub>	Delay time, $\overline{\text{CS}}$ low to $\overline{\text{RD}}$ low	0			ns
t <sub>su2</sub>	Setup time, $\overline{\text{RD}}$ high to $\overline{\text{CS}}$ high	0			ns
t <sub>w5</sub>	Pulse duration, RD low	50			ns
t <sub>en</sub>	Enable time, $\overline{RD}$ low (or $\overline{CS}$ low for read cycle) to data valid			20	ns
t <sub>d2</sub>	Delay time, data hold from RD high	5			ns
t <sub>d3</sub>	Delay time, BUS18/16 or BYTE rising edge or falling edge to data valid	10		20	ns
t <sub>w6</sub>	Pulse duration, RD high	20			ns
t <sub>w7</sub>	Pulse duration, $\overline{\text{CS}}$ high	20			ns
t <sub>h2</sub>	Hold time, last $\overline{\text{RD}}$ (or $\overline{\text{CS}}$ for read cycle ) rising edge to $\overline{\text{CONVST}}$ falling edge	50			ns
t <sub>pd4</sub>	Propagation delay time, BUSY falling edge to next $\overline{\text{RD}}$ (or $\overline{\text{CS}}$ for read cycle) falling edge	0			ns
t <sub>d4</sub>	Delay time, BYTE edge to BUS18/16 edge skew	0			ns
t <sub>su3</sub>	Setup time, BYTE or BUS18/16 transition to RD falling edge	10			ns
t <sub>h3</sub>	Hold time, BYTE or BUS18/16 transition to RD falling edge	10			ns
t <sub>dis</sub>	Disable time, RD high (CS high for read cycle) to 3-stated data bus			20	ns
t <sub>d5</sub>	Delay time, BUSY low to MSB data valid delay			0	ns
t <sub>d6</sub>	Delay time, $\overline{\text{CS}}$ rising edge to BUSY falling edge	50			ns
t <sub>d7</sub>	Delay time, BUSY falling edge to CS rising edge	50			ns
t <sub>su5</sub>	BYTE transition setup time, from BYTE transition to next BYTE transition, or BUS18/16 transition setup time, from BUS18/16 to next BUS18/16.	50			ns
t <sub>su(ABORT)</sub>	Setup time from the <u>falling edge</u> of $\overline{CONVST}$ (used to start the valid conversion) to the next falling edge of $\overline{CONVST}$ (when $\overline{CS} = 0$ and $\overline{CONVST}$ are used to abort) or to the next falling edge of $\overline{CS}$ (when $\overline{CS}$ is used to abort).	60		550	ns

All input signals are specified with  $t_r$  =  $t_f$  = 5 ns (10% to 90% of +VBD) and timed from a voltage level of  $(V_{IL} + V_{IH})/2$ . See timing diagrams.

10

All timing are measured with 20 pF equivalent loads on all data bits and BUSY pins.



### 6.7 Timing Requirements, 3 V

All specifications typical at  $-40^{\circ}$ C to  $85^{\circ}$ C, +VA = 5 V + VBD = 3 V (1) (2) (3)

	PARAMETER	MIN	TYP	MAX	UNIT
t <sub>(CONV)</sub>	Conversion time			650	ns
t <sub>(ACQ)</sub>	Acquisition time	320			ns
t <sub>(HOLD)</sub>	Sample capacitor hold time			25	ns
t <sub>pd1</sub>	CONVST low to BUSY high			40	ns
t <sub>pd2</sub>	Propagation delay time, end of conversion to BUSY low			25	ns
t <sub>pd3</sub>	Propagation delay time, start of convert state to rising edge of BUSY			25	ns
t <sub>w1</sub>	Pulse duration, CONVST low	40			ns
t <sub>su1</sub>	Setup time, $\overline{\text{CS}}$ low to $\overline{\text{CONVST}}$ low	20			ns
t <sub>w2</sub>	Pulse duration, CONVST high	20			ns
	CONVST falling edge jitter			10	ps
t <sub>w3</sub>	Pulse duration, BUSY signal low	t <sub>(ACQ)</sub> min			ns
t <sub>w4</sub>	Pulse duration, BUSY signal high	, ,		650	ns
t <sub>h1</sub>	Hold time, first data bus transition (RD low, or CS low for read cycle, or BYTE or BUS18/16 input changes) after CONVST low	40			ns
t <sub>d1</sub>	Delay time, $\overline{\text{CS}}$ low to $\overline{\text{RD}}$ low	0			ns
t <sub>su2</sub>	Setup time, RD high to CS high	0			ns
t <sub>w5</sub>	Pulse duration, RD low	50			ns
t <sub>en</sub>	Enable time, $\overline{\text{RD}}$ low (or $\overline{\text{CS}}$ low for read cycle) to data valid			30	ns
t <sub>d2</sub>	Delay time, data hold from RD high	5			ns
t <sub>d3</sub>	Delay time, BUS18/16 or BYTE rising edge or falling edge to data valid	10		30	ns
t <sub>w6</sub>	Pulse duration, RD high	20			ns
t <sub>w7</sub>	Pulse duration, CS high	20			ns
t <sub>h2</sub>	Hold time, last RD (or CS for read cycle ) rising edge to CONVST falling edge	50			ns
t <sub>pd4</sub>	Propagation delay time, BUSY falling edge to next $\overline{RD}$ (or $\overline{CS}$ for read cycle) falling edge	0			ns
t <sub>d4</sub>	Delay time, BYTE edge to BUS18/16 edge skew	0			ns
t <sub>su3</sub>	Setup time, BYTE or BUS18/16 transition to RD falling edge	10			ns
t <sub>h3</sub>	Hold time, BYTE or BUS18/16 transition to RD falling edge	10			ns
t <sub>dis</sub>	Disable time, RD high (CS high for read cycle) to 3-stated data bus			30	ns
t <sub>d5</sub>	Delay time, BUSY low to MSB data valid delay			0	ns
t <sub>d6</sub>	Delay time, CS rising edge to BUSY falling edge	50			ns
t <sub>d7</sub>	Delay time, BUSY falling edge to CS rising edge	50			ns
t <sub>su5</sub>	BYTE transition setup time, from BYTE transition to next BYTE transition, or BUS18/16 transition setup time, from BUS18/16 to next BUS18/16.	50			ns
t <sub>su(ABORT)</sub>	Setup time from the falling edge of $\overline{CONVST}$ (used to start the valid conversion) to the next falling edge of $\overline{CONVST}$ (when $CS = 0$ and $\overline{CONVST}$ are used to abort) or to the next falling edge of $\overline{CS}$ (when $\overline{CS}$ is used to abort).	70		550	ns

<sup>1)</sup> All input signals are specified with  $t_r = t_f = 5$  ns (10% to 90% of +VBD) and timed from a voltage level of  $(V_{IL} + V_{IH})/2$ .

#### 6.8 Multiplexer Timing Requirements

VCC = 4.75 V to 7.5 V, VEE = -3 V to -7.5 V

		MIN	TYP	MAX	UNIT
t <sub>su6</sub>	Setup time C1, C2 or C3 to MXCLK rising edge			600	ns
t <sub>d8</sub>	Multiplexer and driver settle time ( from MXCLK rising edge to CONVST falling edge)	600			ns

<sup>(2)</sup> See timing diagrams.

<sup>(3)</sup> All timing are measured with 20-pF equivalent loads on all data bits and BUSY pins.



#### 6.9 Timing Diagrams

The ADS8284 is analog system-on-chip (SoC) device. The device includes a multiplexer, a differential input/differential output ADC driver and differential input high-performance ADC, an additional internal reference, a buffered reference output, and a REF/2 output.

Figure 1 shows the basic operation of the device (including all elements). Subsequent sections describe the detailed timings of the individual blocks of the device (primarily the multiplexer and ADC).

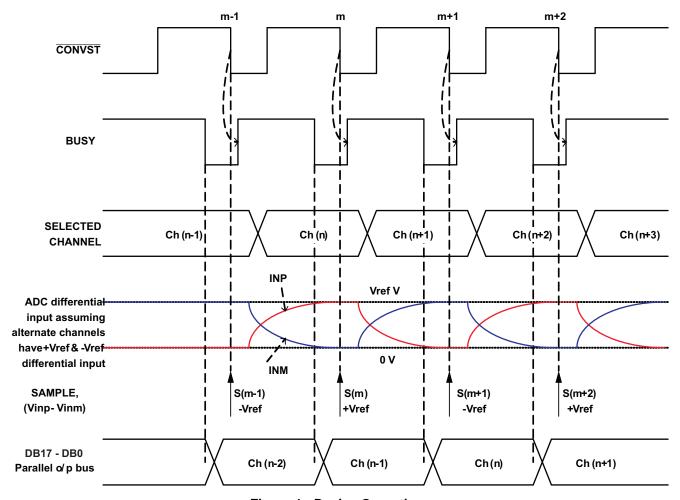


Figure 1. Device Operation

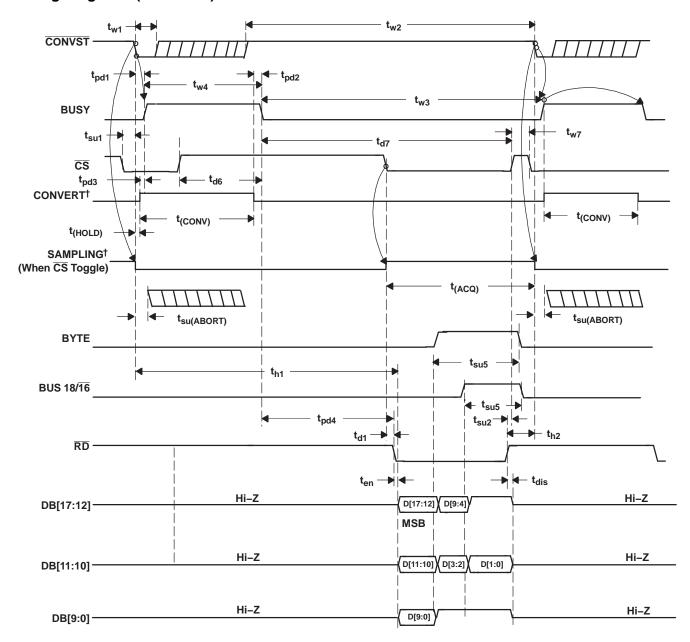
As shown in the diagram, the device can be controlled with only one (CONVST) digital input. On the falling edge of CONVST, the BUSY output of the device goes high. A high level on BUSY indicates the device has sampled the signal and it is converting the sample into its digital equivalent. After the conversion is complete, the BUSY output falls to a logic low level and the device output data corresponding to the recently converted sample is available for reading.

It is recommended (not mandatory) to short the BUSY output of the device to the MXCLK input. The device selects a new channel at every rising edge of MXCLK. The multiplexer is differential. The multiplexer and ADC driver are designed to settle to the 18-bit level before sampling; even at the maximum conversion speed.

**ADC control and timing:** The timing diagrams in this section describe ADC operation; multiplexer operation is described in a later section.

www.ti.com

## **Timing Diagrams (continued)**



<sup>†</sup>Signal internal to device

Figure 2. Timing for Conversion and Acquisition Cycles with  $\overline{\text{CS}}$  and  $\overline{\text{RD}}$  Toggling

### **Timing Diagrams (continued)**

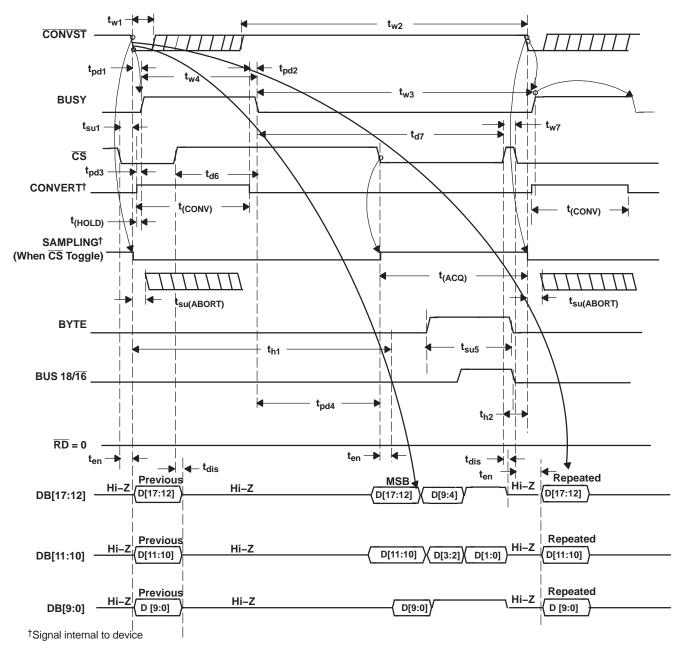


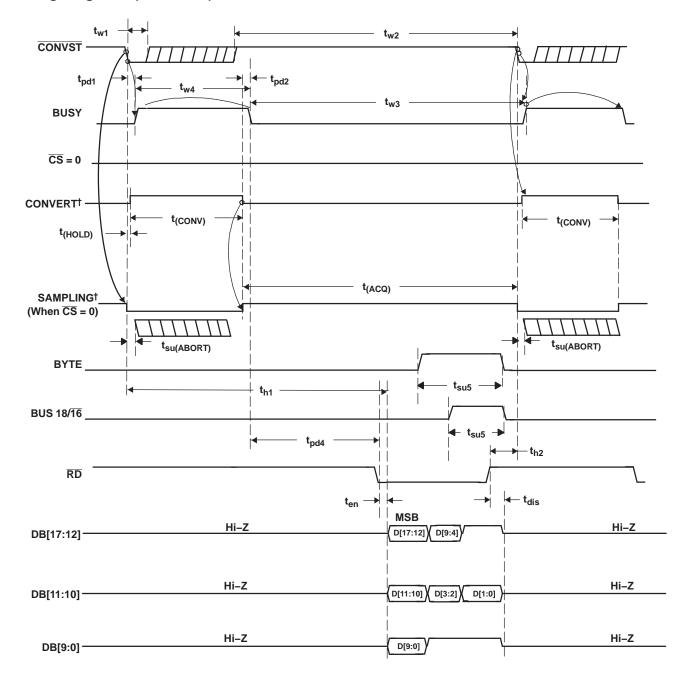
Figure 3. Timing for Conversion and Acquisition Cycles with  $\overline{\text{CS}}$  Toggling,  $\overline{\text{RD}}$  Tied to BDGND

Submit Documentation Feedback

Copyright © 2009–2014, Texas Instruments Incorporated

www.ti.com

## **Timing Diagrams (continued)**



<sup>†</sup>Signal internal to device

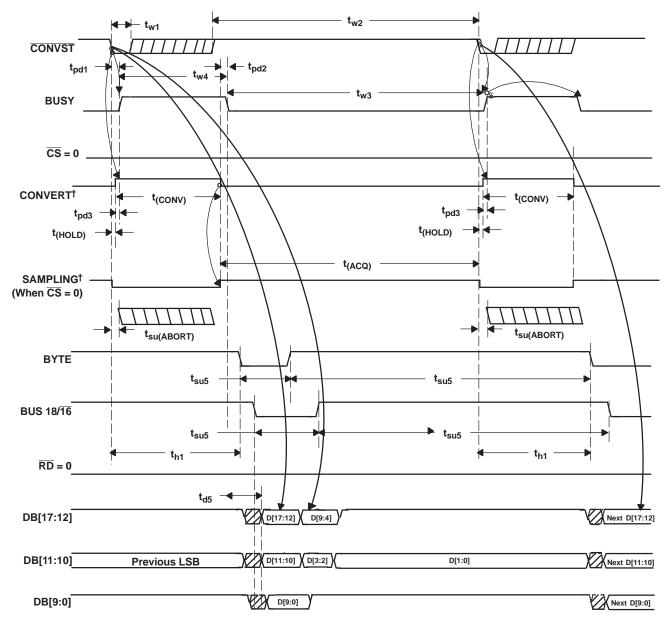
Figure 4. Timing for Conversion and Acquisition Cycles With  $\overline{\text{CS}}$  Tied to BDGND,  $\overline{\text{RD}}$  Toggling

Copyright © 2009–2014, Texas Instruments Incorporated

Submit Documentation Feedback



## **Timing Diagrams (continued)**



<sup>†</sup>Signal internal to device

Figure 5. Timing for Conversion and Acquisition Cycles With  $\overline{\text{CS}}$  and  $\overline{\text{RD}}$  Tied to BDGND - Auto Read

Submit Documentation Feedback

SLAS628A - MARCH 2009 - REVISED APRIL 2014

### **Timing Diagrams (continued)**

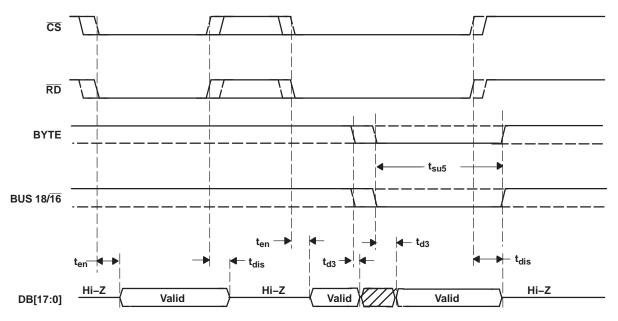


Figure 6. Detailed Timing for Read Cycles

**Multiplexer:** The multiplexer has two modes of sequencing namely auto sequencing and manual sequencing. Multiplexer mode selection and operation is controlled with the AUTO, C1, C2, C3, and MXCLK pin.

**Auto sequencing:** A logic one level on the AUTO pin selects auto sequencing mode. It is possible to select the number of channels to be scanned (always starting from channel zero) in auto sequencing mode. Pins C1 and C2 select the channel count (last channel in the auto sequence).

On every rising edge of MXCLK while C3 is at the logic zero level, the next higher channel (in ascending order) is selected. Channel selection rolls over to channel zero on the rising edge of MXCLK after channel selection reaches the *channel count* (last channel in the auto sequence selected by pins C1and C2).

Any time during the sequence the channel sequence can be reset to channel zero. A rising edge on MXCLK while C3 is at the logic one level resets channel selection to channel zero.

**Table 1. Channel Selection in Auto Mode** 

CHAN	CHANNEL COUNT PINS CLOCK PIN C3 C2 C1 MXCLK		CLOCK PIN	LAST CHANNEL IN SEQUENCE	CHANNEL SEQUENCE			
C3			MXCLK	LAST CHANNEL IN SEQUENCE	CHANNEL SEQUENCE			
0	0	0	1	0	0,0,0,0			
0	0	1	1	1	0,1,0,1,			
0	1	0	1	2	0,1,2,0,1,2,0			
0	1	1	1	3	0,1,2,3,0,1,2,3,0			
1	X	Χ	<b>↑</b>	X	$n \rightarrow 0$ (channel reset to zero)			



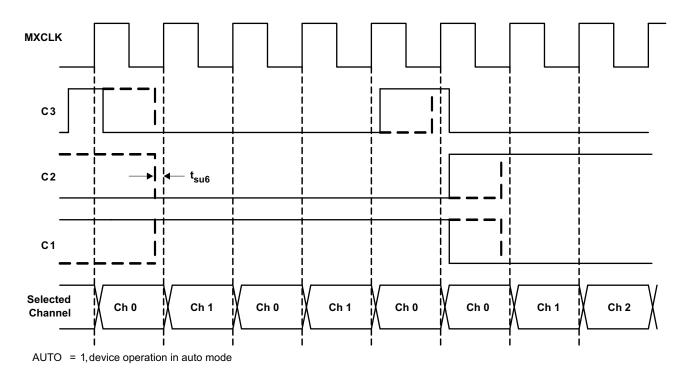


Figure 7. Multiplexer Auto Mode Timing Diagram

**Manual sequencing:** A logic zero level on the AUTO pin selects manual sequencing mode. Pins C1and C2 set the channel address. On the rising edge of MXCLK, the addressed channel is connected to the ADC driver input.

**Table 2. Channel Selection in Manual Mode** 

MODE	СНА	NNEL ADDRESS	CLOCK PIN	CHANNEL		
AUTO	C3	C2	C1	MXCLK	CHANNEL	
0	X	0	0	1	0	
0	X	0	1	1	1	
0	Х	1	0	1	2	
0	Х	1	1	1	3	

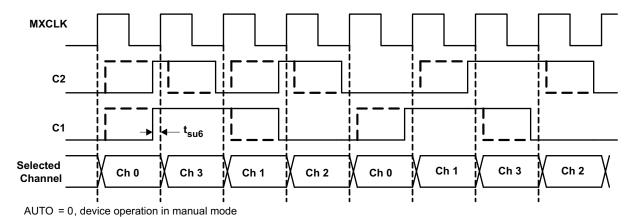


Figure 8. Multiplexer Manual Mode Timing Diagram

Product Folder Links: ADS8284

18

ADS8284



#### 6.10 Typical Characteristics

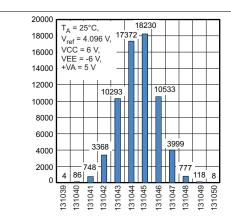


Figure 9. DC Histogram (CH0 without mux switching)

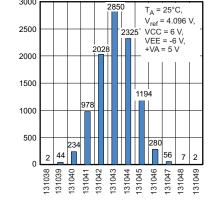


Figure 10. DC Histogram (CH0 with mux switching, CH 0-1-0)

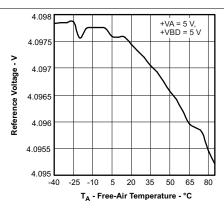


Figure 11. Internal Reference Voltage vs Free-air Temperature

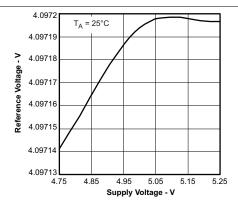


Figure 12. Internal Reference Voltage vs SI Voltage

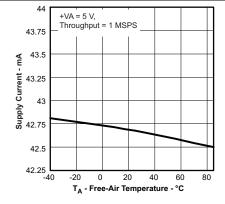


Figure 13. Analog Voltage (+VA) Supply Current (IA) vs Free-air Temperature

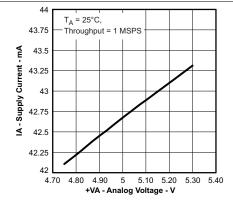


Figure 14. Supply Current (IA) vs Analog Voltage (+VA)

Copyright © 2009–2014, Texas Instruments Incorporated

Submit Documentation Feedback



#### **Typical Characteristics (continued)**

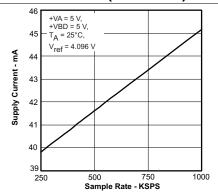


Figure 15. Analog Supply Current vs Sample Rate

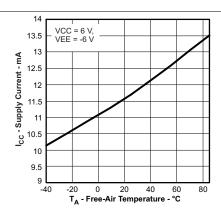


Figure 16. OPA Positive Supply Current (I<sub>CC</sub>) vs Free-air Temperature

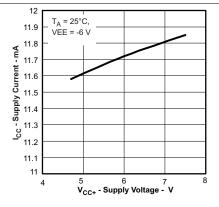


Figure 17. OPA Positive Supply Current (I<sub>CC</sub>) vs OPA Positive Supply Voltage (+VCC)

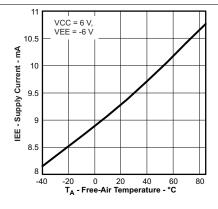


Figure 18. OPA -VE Supply Current (IEE) vs Free-air Temperature

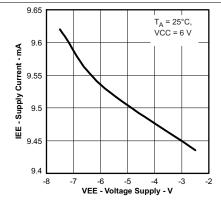


Figure 19. OPA Negative Supply Current (IEE) vs OPA Negative Supply Voltage (-VEE)

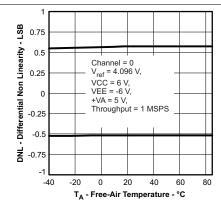


Figure 20. Differential Nonlinearity vs Free-air Temperature

Submit Documentation Feedback

ADS8284

www.ti.com

### **Typical Characteristics (continued)**

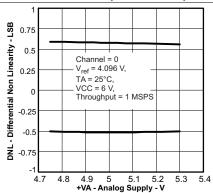


Figure 21. Differential Nonlinearity vs Analog Supply Voltage (+VA)

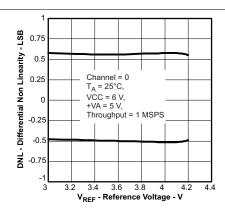


Figure 22. Differential Nonlinearity vs Reference Voltage

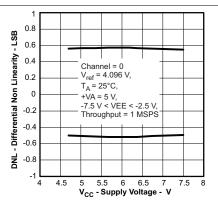


Figure 23. Differential Nonlinearity vs OPA Supply Voltage (VCC)

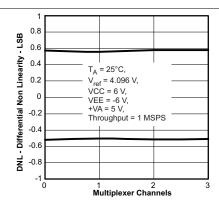


Figure 24. Differential Nonlinearity vs Multiplexer Channels

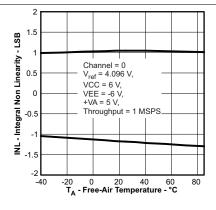


Figure 25. Integral Nonlinearity vs Free-air Temperature

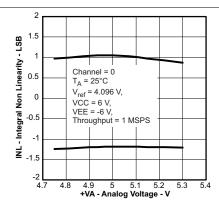


Figure 26. Integral Nonlinearity vs Analog Supply Voltage (+VA)



#### **Typical Characteristics (continued)**

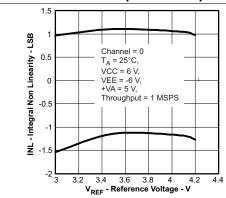


Figure 27. Integral Nonlinearity vs Reference Voltage

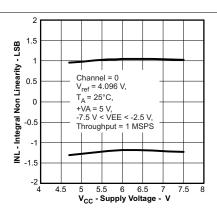


Figure 28. Integral Nonlinearity vs OPA Supply Voltage (+VCC)

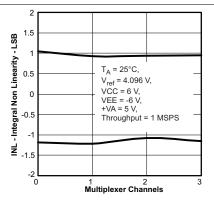


Figure 29. Integral Nonlinearity vs Multiplexer Channels

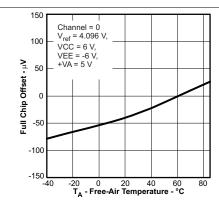


Figure 30. Full Chip Offset Error vs Free-air Temperature

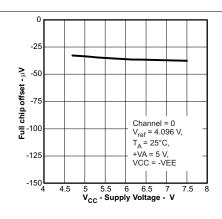


Figure 31. Full Chip Offset Error vs OPA Supply Voltage (VCC)

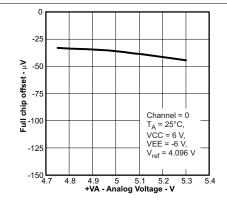


Figure 32. Full Chip Offset Error vs Analog Supply Voltage (+VA)

ADS8284

www.ti.com

#### **Typical Characteristics (continued)**

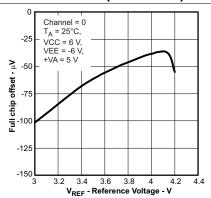


Figure 33. Full Chip Offset Error vs Reference Voltage

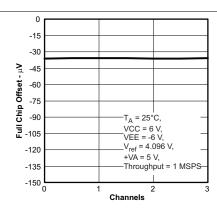


Figure 34. Full Chip Offset Error vs Channel

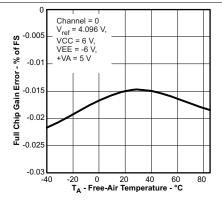


Figure 35. Full Chip Gain Error vs Free-air Temperature

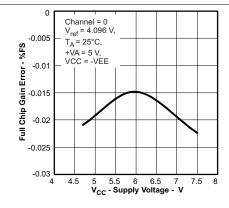


Figure 36. Full Chip Gain Error vs OPA Supply Voltage (VCC)

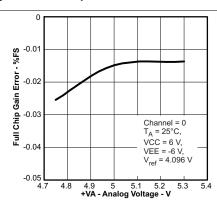


Figure 37. Full Chip Gain Error vs Analog Supply Voltage (+VA)

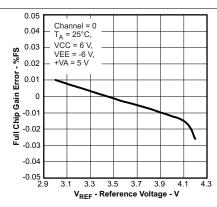


Figure 38. Full Chip Gain Error vs Reference Voltage

Copyright © 2009–2014, Texas Instruments Incorporated

Submit Documentation Feedback



#### **Typical Characteristics (continued)**

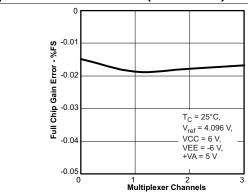


Figure 39. Full Chip Gain Error vs Multiplexer Channels

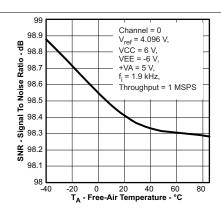


Figure 40. Signal-To-Noise Ratio vs Free-air Temperature

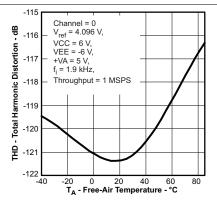


Figure 41. Total Harmonic Distortion vs Free-air Temperature

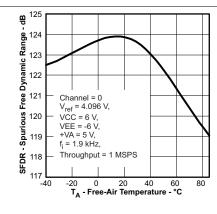


Figure 42. Spurious Free Dynamic Range vs Free-air Temperature

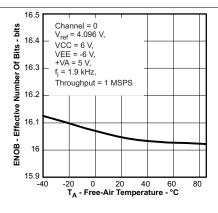


Figure 43. Effective Number Of Bits vs Free-air Temperature

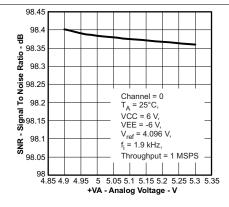


Figure 44. Signal-To-Noise Ratio vs Analog Supply Voltage (+VA)

Submit Documentation Feedback

Copyright © 2009–2014, Texas Instruments Incorporated

ADS8284



**Typical Characteristics (continued)** 

4.8

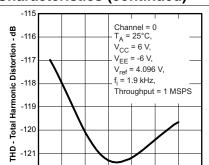


Figure 45. Total Harmonic Distortion vs Analog Supply Voltage (+VA)

4.9 5 5.1 5.2 +VA - Analog Voltage - V 5.3 5.4

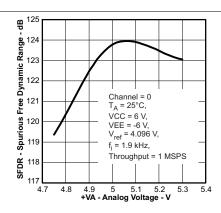


Figure 46. Spurious Free Dynamic Range vs Analog Supply Voltage (+VA)

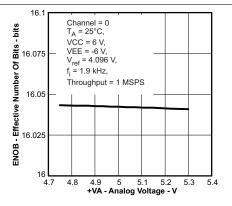


Figure 47. Effective Number Of Bits vs Analog Supply Voltage (+VA)

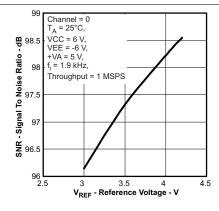


Figure 48. Signal-To-Noise Ratio vs Reference Voltage

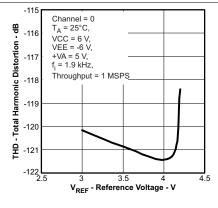


Figure 49. Total Harmonic Distortion vs Reference Voltage

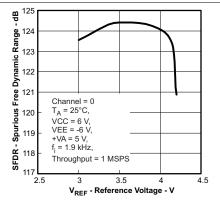


Figure 50. Spurious Free Dynamic Range vs Reference Voltage

Submit Documentation Feedback



#### **Typical Characteristics (continued)**

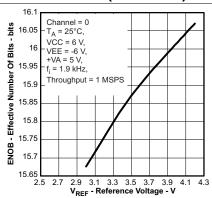


Figure 51. Effective Number Of Bits vs Reference Voltage

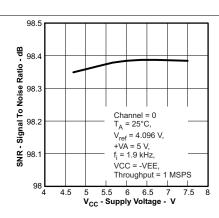


Figure 52. Signal-To-Noise Ratio vs OPA Supply Voltage (VCC)

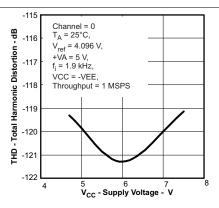


Figure 53. Total Harmonic Distortion vs OPA Supply Voltage (VCC)

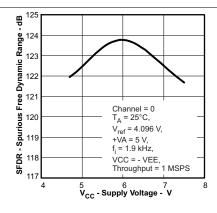


Figure 54. Spurious Free Dynamic Range vs OPA Supply Voltage (VCC)

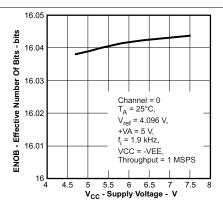


Figure 55. Effective Number Of Bits vs OPA Supply Voltage (VCC)

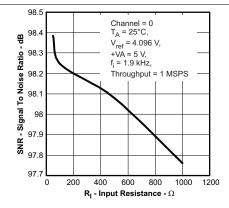


Figure 56. Signal-To-Noise Ratio vs Source Resistance (RIN)

Submit Documentation Feedback

Copyright © 2009–2014, Texas Instruments Incorporated

ADS8284



#### **Typical Characteristics (continued)**

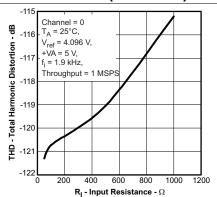


Figure 57. Total Harmonic Distortion vs Source Resistance (RIN)

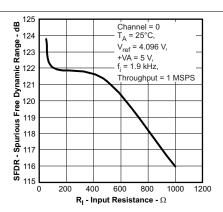


Figure 58. Spurious Free Dynamic Range vs Source Resistance (RIN)

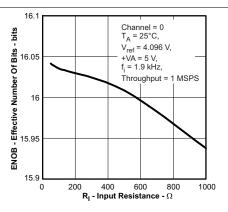


Figure 59. Effective Number OF Bits vs Source Resistance (RIN)

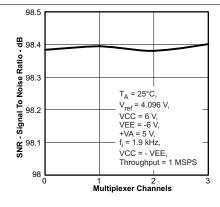


Figure 60. Signal-To-Noise Ratio vs Multiplexer Channels

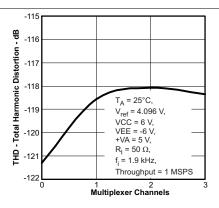


Figure 61. Total Harmonic Distortion vs Multiplexer Channels

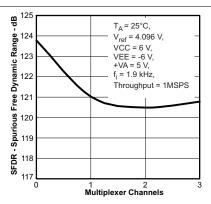


Figure 62. Spurious Free Dynamic Range vs Multiplexer Channels



#### **Typical Characteristics (continued)**

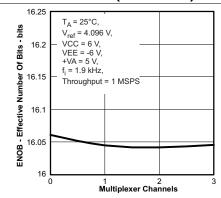


Figure 63. Effective Number Of Bits vs Multiplexer Channels

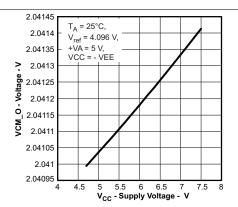


Figure 64. VCM\_O Voltage vs OPA Supply Voltage (VCC)

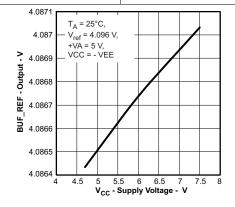


Figure 65. BUF\_REF Output Voltage vs OPA Supply Voltage (VCC)

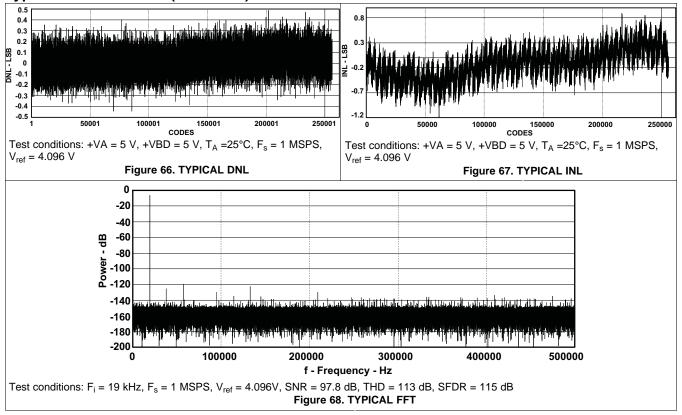
Submit Documentation Feedback

Copyright © 2009–2014, Texas Instruments Incorporated

www.ti.com

SLAS628A - MARCH 2009 - REVISED APRIL 2014

#### **Typical Characteristics (continued)**





### 7 Device Description

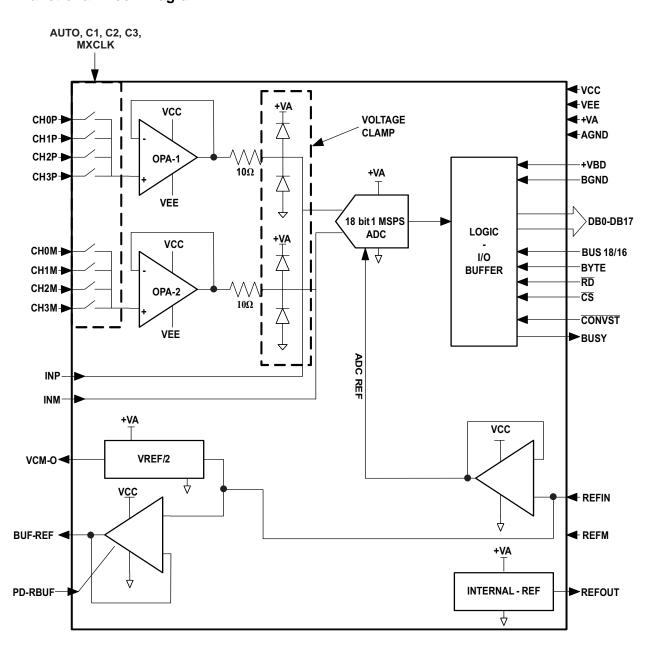
#### 7.1 Overview

The ADS8284 features a high-speed successive approximation register (SAR) analog-to-digital converter (ADC). The architecture is based on charge redistribution which inherently includes a sample/hold function. See Figure 73 for the application circuit for the ADS8284.

The conversion clock is generated internally. The conversion time of 650 ns is capable of sustaining a 1 MHz throughput.

The analog input voltage to ADC is provided to two input pins AINP and AINM. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both inputs are disconnected from any internal function.

#### 7.2 Functional Block Diagram



Product Folder Links: ADS8284

Submit Documentation Feedback



#### 7.3 Feature Description

#### 7.3.1 Analog Input

The device features an analog multiplexer, a differential, high input impedance, unity gain ADC driver, and a high performance ADC. Typically alot of care is required for driving circuit component selection and board layout for high resolution ADC driving. However an on-board ADC driver simplifies the job for the user. All that is required is to decouple AINP and AINM with a 1-nF decoupling capacitor across these two pins as close to the device as possible. The multiplexer inputs tolerate source impedance of up to 50  $\Omega$  for specified device performance at an operating speed of 1-MSPS. This relaxes constraints on the signal conditioning circuit. In the case of true bipolar input signals, it is possible to condition them with a resister divider as shown in Figure 72. The device permits use of 1.2-k $\Omega$  resistors for the divider with effective source impedance of 600  $\Omega$  for signal bandwidth less than 10 kHz. A suitable capacitor value used to limit signal bandwidth limits noise coming from the resistor divider network. Care must be taken concerning absolute analog voltage at the multiplexer input pins. This voltage should not exceed VCC and VEE. The clamp at the driver OPA limits the voltage applied to the ADC input.

#### 7.3.2 Reference

The ADS8284 can operate with an external reference with a range from 3.0 V to 4.2 V. The reference voltage on the input pin 10 (REFIN) of the converter is internally buffered. A clean, low noise, well-decoupled reference voltage on this pin is required to ensure good performance of the converter. A low noise band-gap reference like the REF5040 can be used to drive this pin. A 0.1- $\mu$ F decoupling capacitor is required between REFIN and REFM pins (pin 10 and pin 9) of the converter. This capacitor should be placed as close as possible to the pins of the device. Designers should strive to minimize the routing length of the traces that connect the pins of the capacitor to the pins of the converter. An RC network can also be used to filter the reference voltage. A 100- $\Omega$  series resistor and a 0.1- $\mu$ F capacitor, which can also serve as the decoupling capacitor can be used to filter the reference voltage.

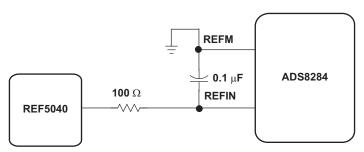


Figure 69. ADS8284 Using External Reference

The ADS8284 also has limited low pass filtering capability built into the converter. The equivalent circuitry on the REFIN input is as shown in Figure 70.

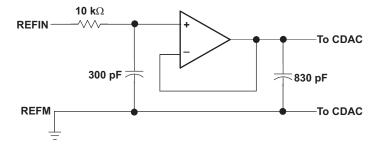


Figure 70. Simplified Reference Input Circuit



#### **Feature Description (continued)**

The REFM input of the ADS8284 should always be shorted to AGND. A 4.096-V internal reference is included. When the internal reference is used, pin 11 (REFOUT) is connected to pin 10 (REFIN) with an 0.1-μF decoupling capacitor and 1-μF storage capacitor between pin 11 (REFOUT) and pin 9 (REFM) (see Figure 74). The internal reference of the converter is double buffered. If an external reference is used, the second buffer provides isolation between the external reference and the CDAC. This buffer is also used to recharge all of the capacitors of the CDAC during conversion (see Figure 70). pin 11 (REFOUT) can be left unconnected (floating) if external reference is used.

#### 7.4 Device Functional Modes

#### 7.4.1 Reading Data

The ADS8284 outputs full parallel data in straight binary format as shown in Table 3. The parallel output is active when  $\overline{\text{CS}}$  and  $\overline{\text{RD}}$  are both low. There is a minimal quiet zone requirement around the falling edge of  $\overline{\text{CONVST}}$ . This is 50 ns prior to the falling edge of  $\overline{\text{CONVST}}$  and  $\overline{\text{40}}$  ns after the falling edge. No data read should attempted within this zone. Any other combination of  $\overline{\text{CS}}$  and  $\overline{\text{RD}}$  sets the parallel output to 3-state. BYTE and BUS18/16 are used for multiword read operations. BYTE is used whenever lower bits on the bus are output on the higher byte of the bus. BUS18/16 is used whenever the last two bits on the 18-bit bus is output on either bytes of the higher 16-bit bus. Refer to Table 3 for ideal output codes.

Table 3. Ideal Input Voltages and Output Codes

DESCRIPTION	ANALOG VALUE	DIGITAL OUTPUT STRAIGHT BINARY				
DESCRIPTION	ANALOG VALUE	BINARY CODY	HEX CODE			
Full scale range	$2 \times (+V_{ref})$					
Least significant bit (LSB)	2 x (+V <sub>ref</sub> )/262144					
+Full scale	(+V <sub>ref</sub> ) - 1 LSB	01 1111 1111 1111 1111	1FFFF			
Midscale	0 V	00 0000 0000 0000 0000	00000			
Midscale – 1 LSB	0 V – 1 LSB	11 1111 1111 1111 1111	3FFFF			
Zero	-V <sub>ref</sub>	10 0000 0000 0000 0000	20000			

The output data is a full 18-bit word (D17–D0) on DB17–DB0 pins (MSB–LSB) if both BUS18/ $\overline{16}$  and BYTE are low.

The result may also be read on an 16-bit bus by using only pins DB17–DB2. In this case two reads are necessary: the first as before, leaving both BUS18/16 and BYTE low and reading the 16 most significant bits (D17–D2) on pins DB17–DB2, then bringing BUS18/16 high while holding BYTE low. When BUS18/16 is high, the lower two bits (D1–D0) appear on pins DB3–DB2.

The result may also be read on an 8-bit bus for convenience. This is done by using only pins DB17–DB10. In this case three reads are necessary: the first as before, leaving both BUS18/16 and BYTE low and reading the 8 most significant bits on pins DB17–DB10, then bringing BYTE high while holding BUS18/16 low. When BYTE is high, the medium bits (D9–D2) appear on pins DB17–DB10. The last read is done by bringing BUS18/16 high while holding BYTE high. When BUS18/16 is high, the lower two bits (D1–D0) appear on pins DB11–DB10. The last read cycle is not necessary if only the first 16 most significant bits are of interest.

All of these multiword read operations can be performed with multiple active  $\overline{RD}$  (toggling) or with  $\overline{RD}$  held low for simplicity. This is referred to as the AUTO READ operation.

**Table 4. Conversion Data Read Out** 

		DATA READ OUT							
BYTE	BUS18/16	TERMINAS DB17-DB12	TERMINAS DB11-DB10	1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 -		TERMINAS DB1-DB0			
High	High	All One's	D1-D0	All One's	All One's	All One's			
Low	High	All One's	All One's	All One's	D1-D0	All One's			
High	Low	D9-D4	D3-D2	All One's	All One's	All One's			
Low	Low	D17-D12	D11-D10	D9-D4	D3-D2	D1-D0			

www.ti.com

### 8 Application and Implementation

#### 8.1 Application Information

As discussed before, the ADS8284 is 18-bit analog SoC that includes various blocks like a multiplexer, ADC driver, internal reference, internal reference buffer, buffered reference output, and Ref/2 output on-board. The following diagram shows the recommended analog and digital interfacing of the ADS8284.

#### 8.2 Typical Applications

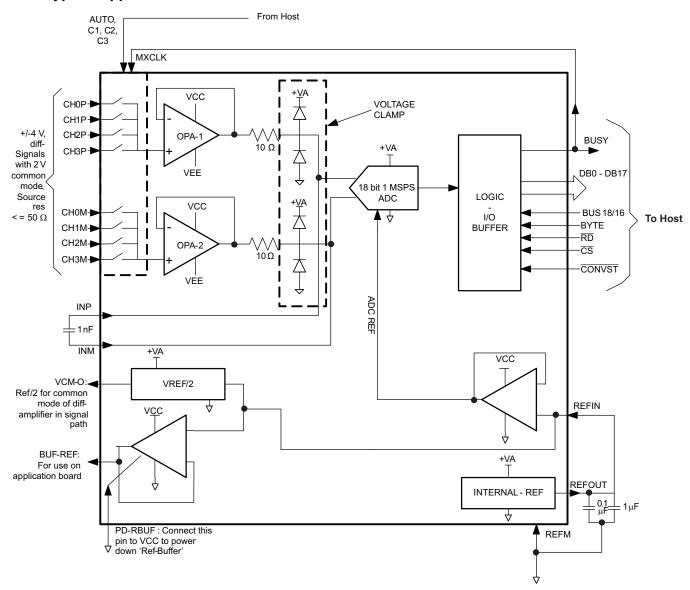


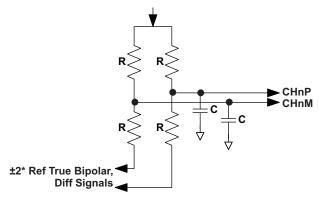
Figure 71. Analog and Digital Interface Diagram



#### **Typical Applications (continued)**

As shown in Figure 71, the ADS8284 accepts unipolar differential analog inputs in the range of  $\pm V_{ref}$  with a common-mode voltage of  $V_{ref}/2$  (0 to  $V_{ref}$  at positive input and  $V_{ref}$  to 0 at negative input). An application may require the interfacing of true bipolar input signals. Figure 72 shows the conversion of bipolar input signals to unipolar differential signals.

#### From BUF-REF o/p of ADC (Use external buffer if current drawn by resistor network exceeds current output specification of reference buffer)



Note: Value of R depends on signal BW Use R = 1.2  $k\Omega$  for signal BW <= 10 kHz. Choose C as per signal BW, 3 dB BW (filt) = RC/2

Figure 72. Conversion of Bipolar Input Signals to Unipolar Differential Signals

www.ti.com

### **Typical Applications (continued)**

Figure 73 shows a parallel interface between the ADS8284 and a typical microcontroller using an 8-bit data bus.

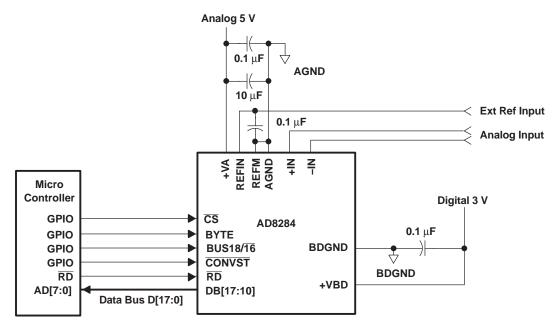


Figure 73. ADS8284 Application Circuitry

The BUSY signal is used as a falling edge interrupt to the microcontroller.

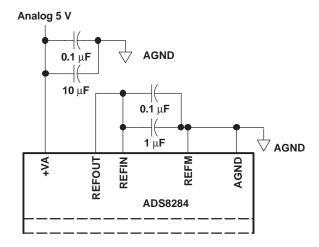


Figure 74. ADS8284 Using Internal Reference



## 9 Power Supply Recommendations

**Table 5. Power Recommendations** 

Voltage Supply	MIN	TYP	MAX
VBD	2.7 V	3.3 V	5.25 V
VA	4.75 V	5 V	5.25 V
VCC	4.75 V	5 V	7.5 V
VEE	−7.5 V	–5 V	-3 V



SLAS628A -MARCH 2009-REVISED APRIL 2014

### 10 Device and Documentation Support

#### 10.1 Trademarks

All trademarks are the property of their respective owners.

#### 10.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 10.3 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms and definitions.

### 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

www.ti.com 10-Nov-2025

#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
ADS8284IBRGCT	NRND	Production	VQFN (RGC)   64	250   SMALL T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	ADS8284 B
ADS8284IBRGCT.A	NRND	Production	VQFN (RGC)   64	250   SMALL T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	ADS8284 B
ADS8284IBRGCT.B	NRND	Production	VQFN (RGC)   64	250   SMALL T&R	-	Call TI	Call TI	-40 to 85	

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

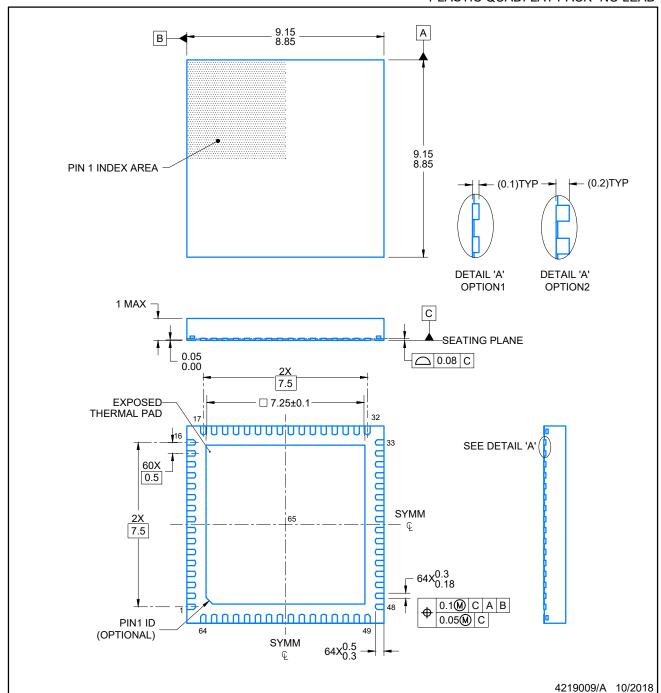


Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4224597/A



PLASTIC QUADFLAT PACK- NO LEAD

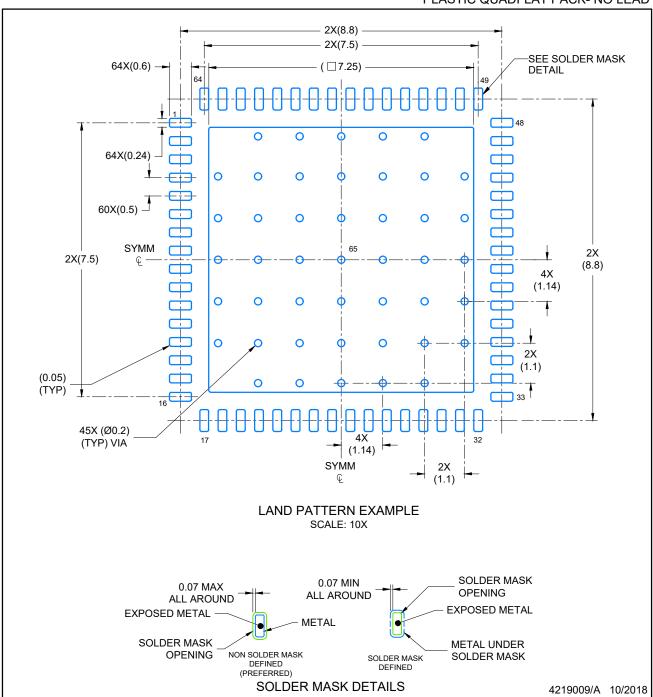


#### NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



PLASTIC QUADFLAT PACK- NO LEAD

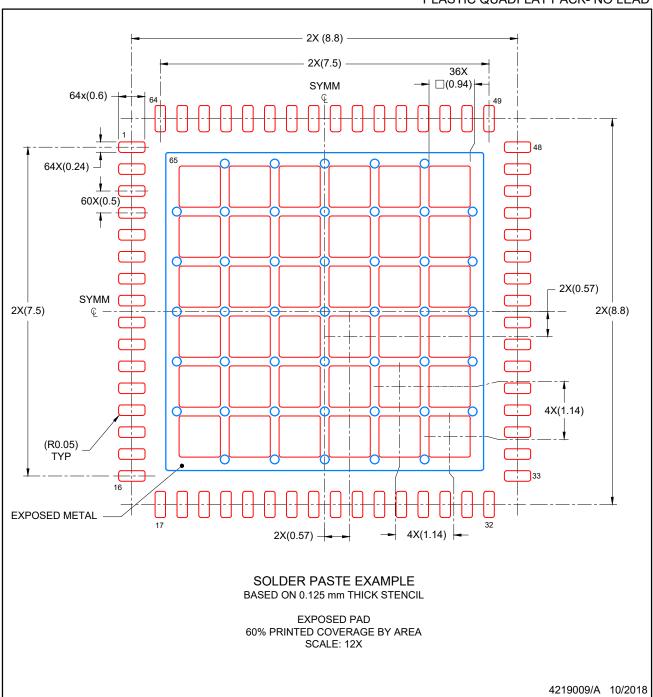


NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUADFLAT PACK- NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



#### IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale, TI's General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025