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# 12-BIT, 3-MSPS, MICROPOWER, MINIATURE SAR ANALOG-TO-DIGITAL CONVERTER

#### **FEATURES**

- 3-MHz Sample Rate Serial Device
- 12-Bit Resolution
- **Zero Latency**
- 48-MHz Serial Interface
- Supply Range: 2.7 V to 5.5 V
- Low Power Dissipation:
  - 6.45 mW at 3-V V<sub>DD</sub>, 2 MSPS
  - 13.5 mw at 5-V V<sub>DD</sub>, 3 MSPS
- ±0.6 LSB INL, ±0.5 LSB DNL
- 72 dB SINAD, -84 dB THD
- Unipolar Input Range: 0 V to V<sub>DD</sub>
- Power-Down Current: 1 µA
- Wide Input Bandwidth: 30 MHz at 3 dB
- 6-Pin SOT23 Package

### **APPLICATIONS**

- **Base Band Converters in Radio** Communication
- Motor Current/Bus Voltage Sensors in Digital **Drives**
- Optical Networking (DWDM, MEMS Based Switching)
- Optical Sensors
- **Battery Powered Systems**
- **Medical Instrumentations**
- **High-Speed Data Acquisition Systems**
- **High-Speed Closed-Loop Systems**

## DESCRIPTION

The ADS7883 is a 12-bit, 3-MSPS analog-to-digital converter (ADC). The device includes a capacitor based SAR A/D converter with inherent sample and hold. The serial interface in the device is controlled by the  $\overline{\text{CS}}$  and SCLK signals for glueless connections with microprocessors and DSPs. The input signal is sampled with the falling edge of CS, and SCLK is used for conversion and serial data output.

The device operates from a wide supply range from 2.7 V to 5.5 V. The low power consumption of the device makes it suitable for battery-powered applications. The device also includes a power saving power-down feature for when the device is operated at lower conversion speeds.

The high level of the digital input to the device is not limited to device V<sub>DD</sub>. Therefore the digital input can go as high as 5.5 V when the device supply is 2.7 V. This feature is useful when digital signals are received from another circuit with different supply levels. This also reduces restrictions on power-up sequencing.

The ADS7883 is available in a 6-pin SOT23 package and is specified for operation from -40°C to 125°C.

### MicroPower Miniature SAR Converter Family

BIT	< 300 KSPS	300 KSPS - 1.25 MSPS	3 MSPS		
10 Dit	ADC7066 (4.2.V) +6.2.6.V )	ADC7006 (2.25 V +o.5.25 V )	4 DC7000	3 MSPS for 4.5 $V_{DD}$ to 5.5 $V_{DD}$	
12-Bit	ADS7866 (1.2 V <sub>DD</sub> to 3.6 V <sub>DD</sub> )	ADS7886 (2.35 V <sub>DD</sub> to 5.25 V <sub>DD</sub> )	ADS7883	2 MSPS for 2.7 $V_{DD}$ to 4.5 $V_{DD}$	
10-Bit	ADS7867 (1.2 V <sub>DD</sub> to 3.6 V <sub>DD</sub> )	ADS7887 (2.35 V <sub>DD</sub> to 5.25 V <sub>DD</sub> )	ADS7884 (2.7 V <sub>DD</sub> to 5.5 V <sub>DD</sub> )		
8-Bit	ADS7868 (1.2 V <sub>DD</sub> to 3.6 V <sub>DD</sub> )	ADS7888 (2.35 V <sub>DD</sub> to 5.25 V <sub>DD</sub> )	ADS7885 (	2.7 V <sub>DD</sub> to 5.5 V <sub>DD</sub> )	



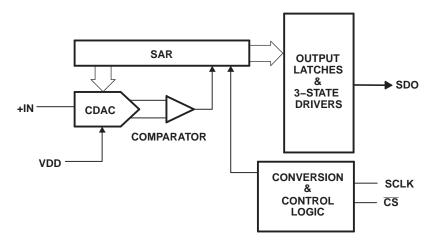
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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



# PACKAGE/ORDERING INFORMATION(1)

DEVICE	MAXIMUM INTEGRAL LINEARITY (LSB)	MAXIMUM DIFFERENTIAL LINEARITY (LSB)	NO MISSING CODES AT RESOLUTION (BIT)	PACKAGE TYPE	PACKAGE DESIGNAT OR	TEMPERATURE RANGE	PACKAGE MARKING	ORDERING INFORMATION	TRANSPORT MEDIA QUANTITY	
ADS7883SB	±1	±1	12		DBV			7883	ADS7883SBDBVT	Small Tape and Reel 250
AD376633B	Ξ1	Ξ1	12	6-Pin SOT23		–40°C to 125°C	7883	ADS7883SBDBVR	Large Tape and Reel 3000	
AD070020	.2	.2	11				7883	ADS7883SDBVT	Small Tape and Reel 250	
ADS7883S	±2	±2					7883	ADS7883SDBVR	Large Tape and Reel 3000	

<sup>(1)</sup> For most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

### ABSOLUTE MAXIMUM RATINGS(1)

		UNIT				
+IN to AGND		-0.3 V to +V <sub>DD</sub> +0.3 V				
+V <sub>DD</sub> to AGND		–0.3 V to 7.0 V				
Digital input voltage to GND	gital input voltage to GND -0.3 V to (7.0 V)					
Digital output to GND	-0.3 V to (+V <sub>DD</sub> + 0.3 V)					
Operating temperature range	ating temperature range -40°C to 125°C					
Storage temperature range		−65°C to 150°C				
Junction temperature (T <sub>J</sub> Max)		150°C				
Power dissipation, SOT23 packa	ge	(T <sub>J</sub> Max–T <sub>A</sub> )/θ <sub>JA</sub>				
Thermal impedance, θ <sub>JA</sub>	SOT23	295.2°C/W				
Load tomporature, coldering	Vapor phase (60 sec)	215°C				
Lead temperature, soldering	Infrared (15 sec)	220°C				

<sup>(1)</sup> Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

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## **ELECTRICAL SPECIFICATIONS**

 $V_{DD}$  = 2.7 V to 5.5 V,  $T_A$  = -40°C to 125°C,  $f_{sample}$  = 2 MSPS for  $V_{DD}$  = 2.7 V to 4.5 V,  $f_{sample}$  = 3 MSPS for  $V_{DD}$  = 4.5 V to 5.5 V

	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALO	G INPUT						_
	Full-scale input voltage s	pan <sup>(1)</sup>		0		$V_{DD}$	V
	Absolute input voltage ra	nge	+IN	-0.2		V <sub>DD</sub> +0.2	V
CI	Input capacitance (2)				27		pF
I <sub>IIkg</sub>	Input leakage current		T <sub>A</sub> = 125°C		40		nA
SYSTEM	M PERFORMANCE						
	Resolution				12		Bits
	Nie odastania da	ADS7883SB		12			D:1-
	No missing codes	ADS7883S		11			Bits
		ADS7883SB		-1	±0.6	1	(3)
INL	Integral nonlinearity	ADS7883S		-2	±0.75	2	LSB <sup>(3)</sup>
		ADS7883SB		-1	±0.5	1	
DNL	Differential nonlinearity	ADS7883S		-2	±0.75	2	LSB
Eo	Offset error <sup>(4)(5)(6)</sup>			-3	±0.2	3	
E <sub>G</sub>	Gain error <sup>(5)</sup>			-3.5	±0.3	3.5	LSB
	ING DYNAMICS						
0, 1,,,,			32-MHz SCLK, V <sub>DD</sub> = 3 V	398	422		T
	Conversion time		48-MHz SCLK, V <sub>DD</sub> = 5 V	265	281		ns
			32-MHz SCLK, V <sub>DD</sub> = 3 V	78	201		
	Acquisition time		48-MHz SCLK, V <sub>DD</sub> = 5 V	52			ns
	Maximum throughput rate		32-MHz SCLK, V <sub>DD</sub> = 2.7 V to 4.5 V	32		2	
			48-MHz SCLK, V <sub>DD</sub> = 4.5 V to 5.5 V			3	MHz
	Anartura dalay		48-IVINZ SCLN, V <sub>DD</sub> = 4:3 V to 5:5 V		10	<u> </u>	
DVNIAM	Aperture delay				10		ns
	IC CHARACTERISTICS	(7)	( 400 111-		0.4		-ID
THD	Total harmonic distortion	(*)	f <sub>I</sub> = 100 kHz	00	-84		dB
SINAD	Signal-to-noise and disto	rtion	f <sub>I</sub> = 100 kHz, ADS7883SB	69	72		dB
			f <sub>I</sub> = 100 kHz, ADS7883S	68	70		
SFDR	Spurious free dynamic ra	nge	f <sub>I</sub> = 100 kHz		86		dB
	Full power bandwidth		At –3 dB	30			MHz
	L INPUT/OUTPUT			_			
Logic fa	mily — CMOS						
$V_{IH}$	High-level input voltage		$V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$	1.5		5.5	V
• 111	- ingir ioro: input rollago		$V_{DD} = 3.6 \text{ V to } 5.5 \text{ V}$	2.2		5.5	
$V_{IL}$	Low-level input voltage		$V_{DD} = 2.7 \text{ V to } 3.6 \text{ V}$			0.4	V
	Low-level iliput voltage		$V_{DD} = 3.6 \text{ V to } 5.5 \text{ V}$			0.8	v
$V_{OH}$	High-level output voltage		At $I_{\text{source}} = 200  \mu\text{A}$	V <sub>DD</sub> -0.2			V
V <sub>OL</sub>	Low-level output voltage		At I <sub>sink</sub> = 200 μA			0.4	v
POWER	SUPPLY REQUIREMENT	S					
+V <sub>DD</sub>	Supply voltage			2.7	3.3	5.5	V

- (1) Ideal input span; does not include gain or offset error
- Refer to Figure 24 for details on sampling circuit
- LSB means least significant bit
- Measured relative to an ideal full-scale input (4)
- Offset error and gain error ensured by characterization
- First transition of 000H to 001H at (V<sub>ref</sub>/2<sup>10</sup>)
  Calculated on the first nine harmonics of the input frequency



# **ELECTRICAL SPECIFICATIONS (continued)**

 $V_{DD}$  = 2.7 V to 5.5 V,  $T_{A}$  = -40°C to 125°C,  $f_{sample}$  = 2 MSPS for  $V_{DD}$  = 2.7 V to 4.5 V,  $f_{sample}$  = 3 MSPS for  $V_{DD}$  = 4.5 V to 5.5 V

PARAMETER	TEST CONDITIONS	MIN TYP	MAX	UNIT
	At V <sub>DD</sub> = 3 V, 2-MSPS throughput	2.15	3	
Supply current (normal mode)	At V <sub>DD</sub> = 3 V, Static state	1.8		mA
Supply current (normal mode)	At $V_{DD} = 5 \text{ V}$ , 3-MSPS throughput	2.7	4	IIIA
	At V <sub>DD</sub> = 5 V, Static state	2		
Dower down state ownship owerest	SCLK off		1	
Power-down state supply current	SCLK on (48 MHz)	90	250	μA
Down discination	V <sub>DD</sub> = 5 V, 3 MSPS	13.5	20	2014/
Power dissipation	V <sub>DD</sub> = 3 V, 2 MSPS	6.45		mW
Devian discination in static state	V <sub>DD</sub> = 5 V	10	12.5	\^/
Power dissipation in static state	$V_{DD} = 3 \text{ V}$	5.4		mW
Power-down time			0.1	μs
Power-up time			0.8	μs
TEMPERATURE RANGE				
Specified performance		-40	125	°C

# TIMING REQUIREMENTS (see Figure 21)

All specifications typical at  $T_A = -40$ °C to 125°C,  $V_{DD} = 2.7$  V to 5.5 V, unless otherwise specified.

	PARAMETER	TEST CONDITIONS <sup>(1)</sup>	MIN	TYP	MAX	UNIT	
	Conversion time	V <sub>DD</sub> = 3 V			13.5 × t <sub>SCLK</sub>	ns	
t <sub>conv</sub>	Conversion time	V <sub>DD</sub> = 5 V		13.5 × t <sub>SCLK</sub>	113		
	A quicition time	$V_{DD} = 3 V$	78			nc	
t <sub>acq</sub>	Aquisition time	V <sub>DD</sub> = 5 V	52			ns	
	Minimum quiet time needed from bus 3-state to start	V <sub>DD</sub> = 3 V	10				
t <sub>q</sub>	of next conversion	V <sub>DD</sub> = 5 V	10			ns	
	Delay time, CS low to first data (0) out	V <sub>DD</sub> = 3 V		9	15	no	
t <sub>d1</sub>	Delay time, CS low to first data (0) out	V <sub>DD</sub> = 5 V		8	11	ns	
	Setup time CS love to SCL K love	$V_{DD} = 3 V$	7			20	
t <sub>su1</sub>	Setup time, CS low to SCLK low	V <sub>DD</sub> = 5 V	5			ns	
	Delay time, SCLK falling to SDO	V <sub>DD</sub> = 3 V		11	20	no	
t <sub>d2</sub>	belay time, SCLN familing to SDO	$V_{DD} = 5 V$		9	12	ns	
	Hold time, SCLK falling to data valid (2)	V <sub>DD</sub> < 3 V	5.5			ns	
t <sub>h1</sub>	Hold liftle, SCLK failing to data valid	V <sub>DD</sub> > 5 V	4				
	Delay time, 16th SCLK falling edge to SDO 3-state	$V_{DD} = 3 V$		9	15		
t <sub>d3</sub>	belay time, Total SCLK failing edge to SDO 3-state	$V_{DD} = 5 V$		8	11	ns	
+	Pulse duration, $\overline{\text{CS}}$	$V_{DD} = 3 V$	10			200	
t <sub>w1</sub>	ruise duration, CS	$V_{DD} = 5 V$	10			ns	
	Delay time, CS high to SDO 3-state,	$V_{DD} = 3 V$		9	15	20	
t <sub>d4</sub>	belay time, CS high to SDO 3-state,	V <sub>DD</sub> = 5 V		8	11	ns	
	Dulas duration CCLV high	V <sub>DD</sub> = 3 V	0.45 × t <sub>SCLK</sub>	0.45 × t <sub>SCLK</sub>			
t <sub>wH</sub>	Pulse duration, SCLK high	V <sub>DD</sub> = 5 V	0.45 × t <sub>SCLK</sub>			ns	
	Pulse duration, SCLK low	V <sub>DD</sub> = 3 V	0.45 × t <sub>SCLK</sub>		ns		
$t_{wL}$	Fuise duration, SCLN IOW	V <sub>DD</sub> = 5 V	0.45 × t <sub>SCLK</sub>				

<sup>(1) 3-</sup>V Specifications apply from 2.7 V to 3.6 V, and 5-V specifications apply from 4.5 V to 5.5 V.

4

<sup>(2)</sup> With 10-pf load.

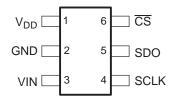
# TIMING REQUIREMENTS (see Figure 21) (continued)

All specifications typical at  $T_A = -40$ °C to 125°C,  $V_{DD} = 2.7$  V to 5.5 V, unless otherwise specified.

	PARAMETER	TEST CONDITIONS <sup>(1)</sup>	MIN	TYP	MAX	UNIT		
	Fraguency COLV	$V_{DD} = 2.7 \text{ V to } 4.5 \text{ V}$			32	NAL I-		
	Frequency, SCLK	V <sub>DD</sub> = 4.5 V to 5.5 V			48	MHz		
	Delay time, second falling edge of clock and $\overline{\text{CS}}$ to	V <sub>DD</sub> = 3 V	-2		4			
t <sub>d5</sub>	enter in powerdown (use min spec not to accidently enter in powerdown) see Figure 22	V <sub>DD</sub> = 5 V	-2		3	ns		
	Delay time, CS and 10th falling edge of clock to enter	V <sub>DD</sub> = 3 V	-2		4			
t <sub>d6</sub>	in powerdown (use max spec not to accidently enter in powerdown) see Figure 22	V <sub>DD</sub> = 5 V	-2		3	ns		

# **DEVICE INFORMATION**

## SOT23 PACKAGE (TOP VIEW)



## **TERMINAL FUNCTIONS**

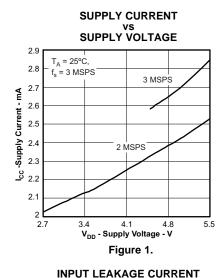
TERMINAL		1/0	DESCRIPTION					
NAME	NO.	1/0	DESCRIPTION					
$V_{DD}$	1	_	Power supply input, also acts like a reference voltage to ADC.					
GND	2	_	Ground for power supply, all analog and digital signals are referred with respect to this pin.					
VIN	3	I	Analog signal input					
SCLK	4	I	Serial clock					
SDO	5	0	Serial data out					
CS	6	I	Chip select signal, active low					

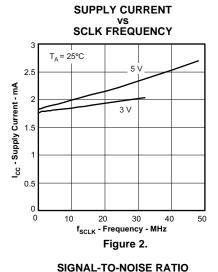
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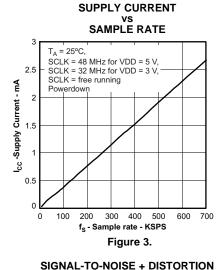
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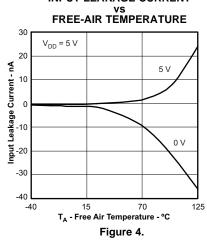
### TYPICAL CHARACTERISTICS

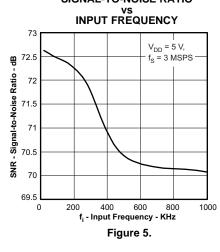


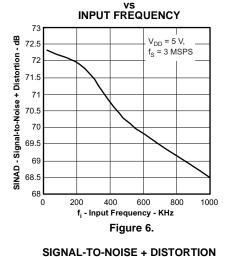


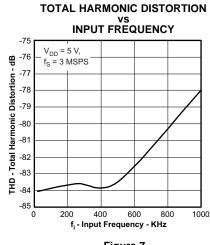


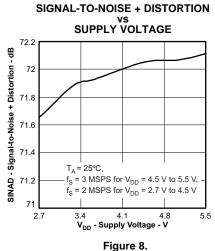












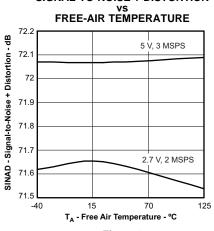
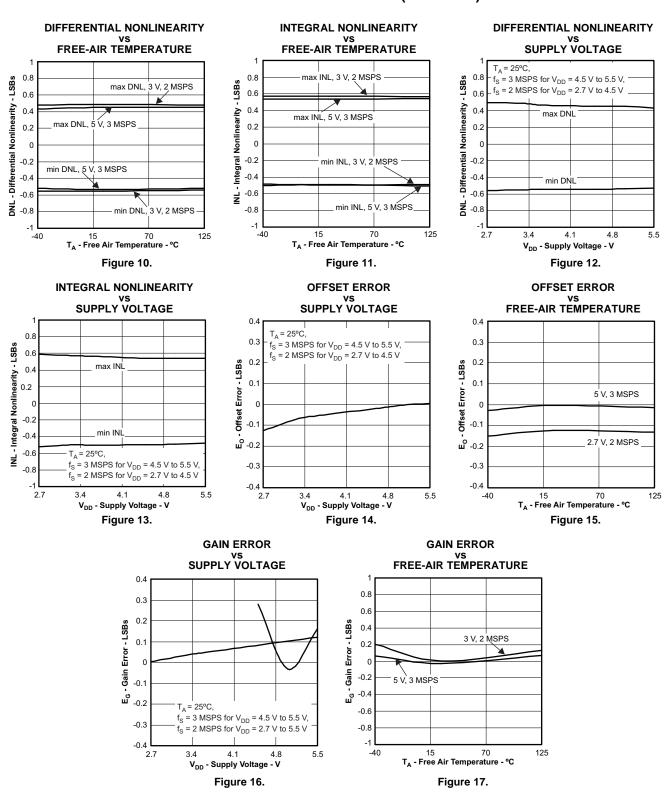


Figure 9.

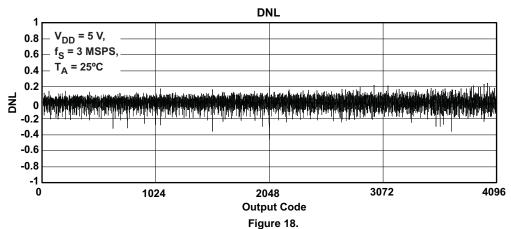


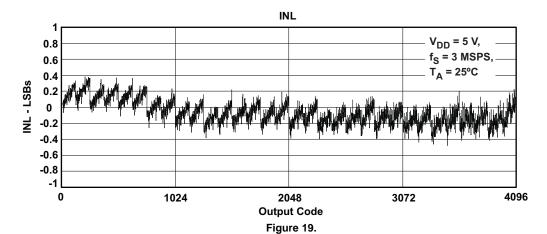
## **TYPICAL CHARACTERISTICS (continued)**

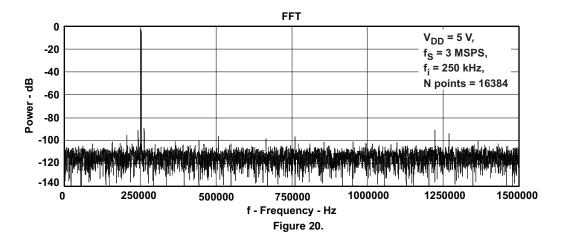




# **TYPICAL CHARACTERISTICS (continued)**







#### NORMAL OPERATION

The cycle begins with the falling edge of  $\overline{CS}$ . This point is indicated as **a** in Figure 21. With the falling edge of  $\overline{CS}$ , the input signal is sampled and the conversion process is initiated. The device outputs data while the conversion is in progress. The data word contains two leading zeros, followed by 12-bit data in MSB first format and padded by two lagging zeros.

The falling edge of  $\overline{CS}$  clocks out the first zero, and a second zero is clocked out on the first falling edge of the clock. Data is in MSB first format with the MSB being clocked out on the 2nd falling edge. Data is padded with two lagging zeros as shown in Figure 21. The conversion ends on the first rising edge of SCLK after the 13th falling edge. At this point the device enters the acquisition phase. This point is indicated by **b** in Figure 21.

Figure 21 shows the device data is read in a sixteen clock frame. However,  $\overline{CS}$  can be asserted (pulled high) any time after point **b**. SDO goes to 3-state with the  $\overline{CS}$  high level. The next conversion should not be started (by pulling  $\overline{CS}$  low) until the end of the quiet sampling time ( $t_q$ ) after SDO goes to 3-state or until the minimum acquisition time ( $t_{acq}$ ) has elapsed. To continue normal operation, it is necessary that  $\overline{CS}$  is not pulled high until point **b**. Without this, the device does not enter the acquisition phase and no valid data is available in the next cycle. (Also refer to the Power-Down Mode section for more details.)  $\overline{CS}$  going high any time during the conversion aborts the ongoing conversion and SDO goes to 3-state.

The high level of the digital input to the device is not limited to device  $V_{DD}$ . This means the digital input can go as high as 5.5 V when the device supply is 2.7 V. This feature is useful when digital signals are received from another circuit with different supply levels. Also, this relaxes the restriction on power-up sequencing. However, the digital output levels ( $V_{OH}$  and  $V_{OL}$ ) are governed by  $V_{DD}$  as listed in the Electrical Specifications table.

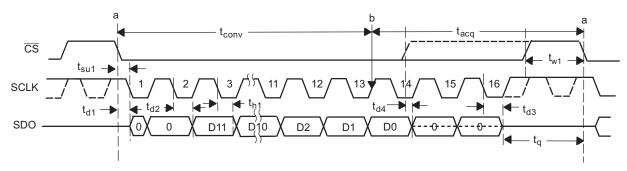


Figure 21. Interface Timing Diagram

#### **POWER-DOWN MODE**

The device enters power-down mode if  $\overline{\text{CS}}$  goes high anytime after the 2nd SCLK falling edge to before the 10th SCLK falling edge. An ongoing conversion stops and SDO goes to 3-state under this power-down condition as shown in Figure 22.

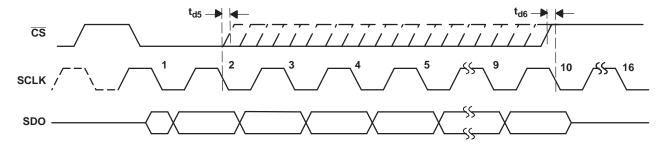


Figure 22. Entering Power-Down Mode

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A dummy cycle with  $\overline{\text{CS}}$  low for more than 10 SCLK falling edges brings the device out of power-down mode. For the device to reach the fully powered up condition requires 0.8  $\mu$ s.  $\overline{\text{CS}}$  can be pulled high any time after the 10th falling edge as shown in Figure 23. Note that the power-up time of 0.8  $\mu$ s is more than a single conversion cycle at 3-MSPS speed. This means the device requires three dummy conversion frames at 3-MSPS speed or one elongated dummy conversion frame. The data during the dummy conversion frames is invalid.

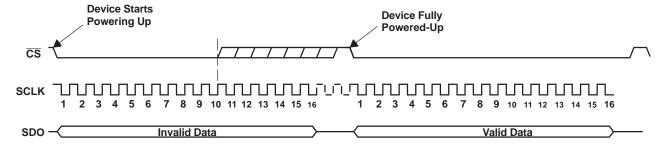


Figure 23. Exiting Power-Down Mode

#### APPLICATION INFORMATION

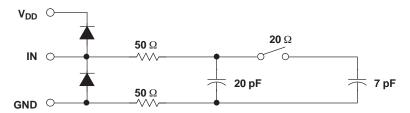


Figure 24. Typical Equivalent Sampling Circuit

## Driving the VIN and V<sub>DD</sub> Pins

The VIN input to the ADS7883 should be driven with a low impedance source. In most cases additional buffers are not required. In cases where the source impedance exceeds 200  $\Omega$ , using a buffer would help achieve the rated performance of the converter. The THS4031 is a good choice for the driver amplifier buffer.

The reference voltage for the ADS7883 A/D converter is derived from the supply voltage internally. The device offers limited low-pass filtering functionality on-chip. The supply to these converters should be driven with a low impedance source and should be decoupled to the ground. A 1-µF storage capacitor and a 10-nF decoupling capacitor should be placed close to the device. Wide, low impedance traces should be used to connect the capacitor to the pins of the device. The ADS7883 draws very little current from the supply lines. The supply line can be driven by either:

- Directly from the system supply.
- A reference output from a low drift and low drop out reference voltage generator like the REF5030 or REF5050. The ADS7883 can operate with a wide range of supply voltages. The actual choice of the reference voltage generator depends upon the system. Figure 26 shows one possible application circuit.
- A low-pass filtered version of the system supply followed by a buffer like the zero-drift OPA735 can also be
  used in cases where the system power supply is noisy. Care should be taken to ensure that the voltage at the
  V<sub>DD</sub> input does not exceed 7 V (especially during power up) to avoid damage to the converter. This can be
  done easily using single supply CMOS amplifiers like the OPA735. Figure 27 shows one possible application
  circuit.

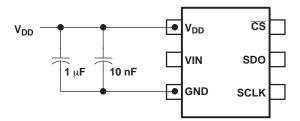


Figure 25. Supply/Reference Decoupling Capacitors

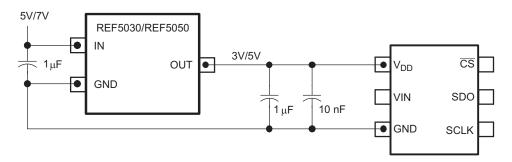


Figure 26. Using the REF5030/REF5050 Reference

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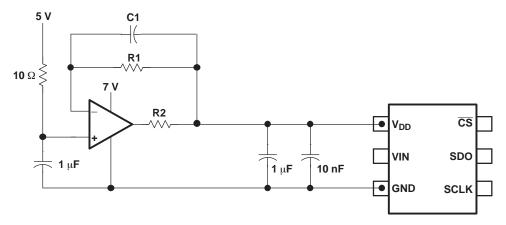


Figure 27. Buffering with the OPA735

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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
ADS7883SBDBVR	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	7883
ADS7883SBDBVR.A	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	7883
ADS7883SBDBVT	Active	Production	SOT-23 (DBV)   6	250   SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	7883
ADS7883SBDBVT.A	Active	Production	SOT-23 (DBV)   6	250   SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	7883
ADS7883SDBVR	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	7883
ADS7883SDBVR.A	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	7883
ADS7883SDBVT	Active	Production	SOT-23 (DBV)   6	250   SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	7883
ADS7883SDBVT.A	Active	Production	SOT-23 (DBV)   6	250   SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	7883

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No. RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

# **PACKAGE OPTION ADDENDUM**

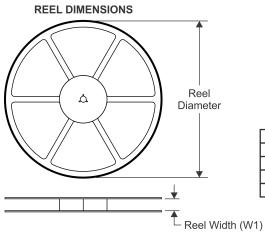
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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

# PACKAGE MATERIALS INFORMATION

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# TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

All difficusions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7883SBDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADS7883SBDBVT	SOT-23	DBV	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADS7883SDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADS7883SDBVT	SOT-23	DBV	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

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\*All dimensions are nominal

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Device	Device Package Type		Pins SPQ		Length (mm)	Width (mm)	Height (mm)			
ADS7883SBDBVR	SOT-23	DBV	6	3000	213.0	191.0	35.0			
ADS7883SBDBVT	SOT-23	DBV	6	250	213.0	191.0	35.0			
ADS7883SDBVR	SOT-23	DBV	6	3000	213.0	191.0	35.0			
ADS7883SDBVT	SOT-23	DBV	6	250	213.0	191.0	35.0			



SMALL OUTLINE TRANSISTOR



### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

- 4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- 5. Refernce JEDEC MO-178.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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