



12-Bit, 8-Channel Sampling ANALOG-TO-DIGITAL CONVERTER with I²C™ Interface

FEATURES

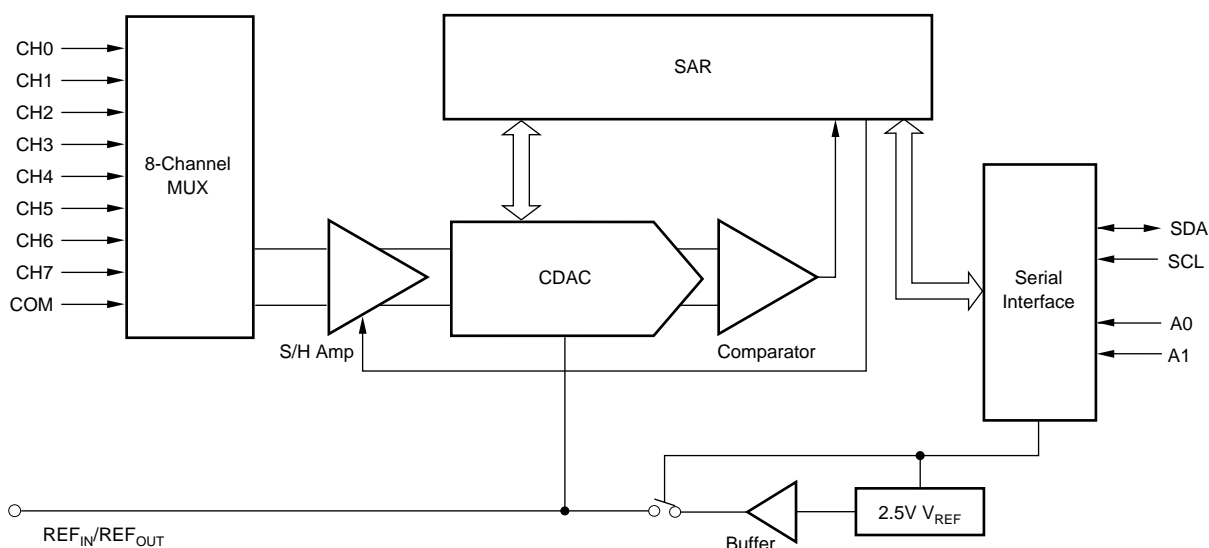
- 8-CHANNEL MULTIPLEXER
- 50kHz SAMPLING RATE
- NO MISSING CODES
- 2.7V TO 5V OPERATION
- INTERNAL 2.5V REFERENCE
- I²C INTERFACE SUPPORTS:
Standard, Fast, and High-Speed Modes
- TSSOP-16 PACKAGE

DESCRIPTION

The ADS7828 is a single-supply, low-power, 12-bit data acquisition device that features a serial I²C interface and an 8-channel multiplexer. The Analog-to-Digital (A/D) converter features a sample-and-hold amplifier and internal, asynchronous clock. The combination of an I²C serial, 2-wire interface and micropower consumption makes the ADS7828 ideal for applications requiring the A/D converter to be close to the input source in remote locations and for applications requiring isolation. The ADS7828 is available in a TSSOP-16 package.

APPLICATIONS

- VOLTAGE-SUPPLY MONITORING
- ISOLATED DATA ACQUISITION
- TRANSDUCER INTERFACES
- BATTERY-OPERATED SYSTEMS
- REMOTE DATA ACQUISITION



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

I²C is a trademark of Koninklijke Philips Electronics N.V. All other trademarks are the property of their respective owners.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

+V _{DD} to GND	-0.3V to +6V
Digital Input Voltage to GND	-0.3V to +V _{DD} + 0.3V
Operating Temperature Range	-40°C to +105°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature (T _J max)	+150°C
TSSOP Package	
Power Dissipation	(T _J max - T _A)/θ _{JA}
θ _{JA} Thermal Impedance	240°C/W
Lead Temperature, Soldering	
Vapor Phase (60s)	+215°C
Infrared (15s)	+220°C

NOTE: (1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

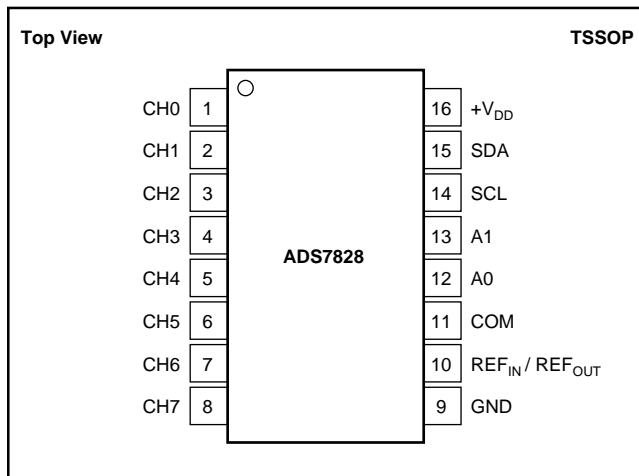
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION⁽¹⁾

PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS7828E	±2	TSSOP-16	PW	-40°C to +85°C	ADS7828E/250	Tape and Reel, 250
"	"	"	"	"	ADS7828E/2K5	Tape and Reel, 2500
ADS7828EB	±1	TSSOP-16	PW	-40°C to +85°C	ADS7828EB/250	Tape and Reel, 250
"	"	"	"	"	ADS7828EB/2K5	Tape and Reel, 2500

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI web site at www.ti.com.

PIN CONFIGURATION



PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	CH0	Analog Input Channel 0
2	CH1	Analog Input Channel 1
3	CH2	Analog Input Channel 2
4	CH3	Analog Input Channel 3
5	CH4	Analog Input Channel 4
6	CH5	Analog Input Channel 5
7	CH6	Analog Input Channel 6
8	CH7	Analog Input Channel 7
9	GND	Analog Ground
10	REF _{IN} / REF _{OUT}	Internal +2.5V Reference, External Reference Input
11	COM	Common to Analog Input Channel
12	A0	Slave Address Bit 0
13	A1	Slave Address Bit 1
14	SCL	Serial Clock
15	SDA	Serial Data
16	+V _{DD}	Power Supply, 3.3V Nominal

ELECTRICAL CHARACTERISTICS: +2.7V

At $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $+V_{DD} = +2.7\text{V}$, $V_{REF} = +2.5\text{V}$, SCL Clock Frequency = 3.4MHz (High-Speed Mode), unless otherwise noted.

PARAMETER	CONDITIONS	ADS7828E			ADS7828EB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUT								
Full-Scale Input Scan	Positive Input - Negative Input	0		V_{REF}	0		V_{REF}	V
Absolute Input Range	Positive Input	-0.2		$+V_{DD} + 0.2$	-0.2		$+V_{DD} + 0.2$	V
	Negative Input	-0.2		+0.2	-0.2		+0.2	V
Capacitance			25			25		pF
Leakage Current			± 1			± 1		μA
SYSTEM PERFORMANCE								
No Missing Codes		12			12			Bits
Integral Linearity Error			± 1.0	± 2		± 0.5	± 1	LSB ⁽¹⁾
Differential Linearity Error			± 1.0	± 2		± 0.5	-1, +2	LSB
Offset Error			± 1.0	± 3		± 0.75	± 2	LSB
Offset Error Match			± 0.2	± 1		± 0.2	± 1	LSB
Gain Error			± 1.0	± 4		± 0.75	± 3	LSB
Gain Error Match			± 0.2	± 1		± 0.2	± 1	LSB
Noise			33			33		μVRMS
Power-Supply Rejection			82			82		dB
SAMPLING DYNAMICS								
Throughput Frequency	High Speed Mode: SCL = 3.4MHz Fast Mode: SCL = 400kHz Standard Mode, SCL = 100kHz			50 8 2			50 8 2	kHz
Conversion Time			6			6		μs
AC ACCURACY								
Total Harmonic Distortion	$V_{IN} = 2.5V_{PP}$ at 10kHz		-82			-82		dB ⁽²⁾
Signal-to-Ratio	$V_{IN} = 2.5V_{PP}$ at 10kHz		72			72		dB
Signal-to-(Noise+Distortion) Ratio	$V_{IN} = 2.5V_{PP}$ at 10kHz		71			71		dB
Spurious-Free Dynamic Range	$V_{IN} = 2.5V_{PP}$ at 10kHz		86			86		dB
Isolation Channel-to-Channel			120			120		dB
VOLTAGE REFERENCE OUTPUT								
Range		2.475	2.5	2.525	2.475	2.5	2.525	V
Internal Reference Drift			15			15		ppm/ $^{\circ}\text{C}$
Output Impedance	Internal Reference ON		110			110		Ω
	Internal Reference OFF		1			1		G Ω
Quiescent Current	Int. Ref. ON, SCL and SDA pulled HIGH		850			850		μA
VOLTAGE REFERENCE INPUT								
Range		0.05		V_{DD}	0.05		V_{DD}	V
Resistance			1			1		G Ω
Current Drain	High Speed Mode: SCL= 3.4MHz		20			20		μA
DIGITAL INPUT/OUTPUT								
Logic Family			CMOS			CMOS		
Logic Levels:		$+V_{DD} \cdot 0.7$		$+V_{DD} + 0.5$	$+V_{DD} \cdot 0.7$		$+V_{DD} + 0.5$	V
V_{IH}		-0.3		$+V_{DD} \cdot 0.3$	-0.3		$+V_{DD} \cdot 0.3$	V
V_{IL}				0.4			0.4	V
V_{OL}				10			10	μA
Input Leakage: I_{IH}	Min. 3mA Sink Current							μA
I_{IL}	$V_{IH} = +V_{DD} + 0.5$ $V_{IL} = -0.3$	-10			-10			μA
Data Format			Straight Binary			Straight Binary		
ADS7828 HARDWARE ADDRESS			10010			10010		Binary
POWER-SUPPLY REQUIREMENTS								
Power-Supply Voltage, $+V_{DD}$	Specified Performance	2.7		3.6	2.7		3.6	V
Quiescent Current	High Speed Mode: SCL = 3.4MHz		225	320		225	320	μA
	Fast Mode: SCL = 400kHz		100			100		μA
	Standard Mode, SCL = 100kHz		60			60		μA
Power Dissipation	High Speed Mode: SCL = 3.4MHz		675	1000		675	1000	μW
	Fast Mode: SCL = 400kHz		300			300		μW
	Standard Mode, SCL = 100kHz		180			180		μW
Power-Down Mode	High Speed Mode: SCL = 3.4MHz		70			70		μA
w/Wrong Address Selected	Fast Mode: SCL = 400kHz		25			25		μA
	Standard Mode, SCL = 100kHz		6			6		μA
Full Power-Down	SCL Pulled HIGH, SDA Pulled HIGH		400	3000		400	3000	nA
TEMPERATURE RANGE								
Specified Performance		-40		85	-40		85	$^{\circ}\text{C}$

NOTES: (1) LSB means Least Significant Bit. With V_{REF} equal to 2.5V, 1LSB is 610 μV .

(2) THD measured out to the 9th-harmonic.

ELECTRICAL CHARACTERISTICS: +5V

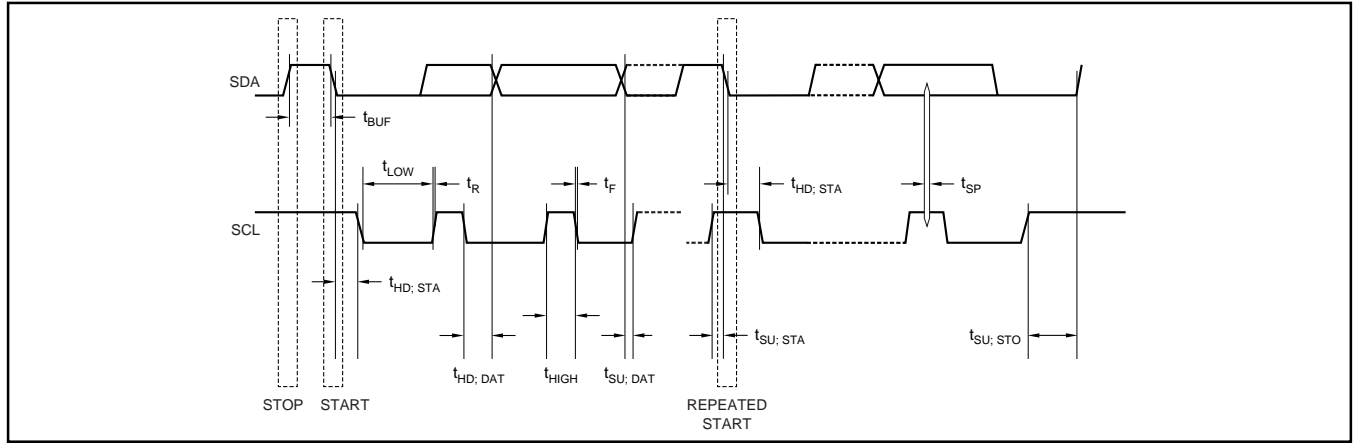
At $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $+V_{DD} = +5.0\text{V}$, $V_{REF} = \text{External } +5.0\text{V}$, SCL Clock Frequency = 3.4MHz (High-Speed Mode), unless otherwise noted.

PARAMETER	CONDITIONS	ADS7828E			ADS7828EB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUT								
Full-Scale Input Scan	Positive Input - Negative Input	0		V_{REF}	0		V_{REF}	V
Absolute Input Range	Positive Input	-0.2		$+V_{DD} + 0.2$	-0.2		$+V_{DD} + 0.2$	V
	Negative Input	-0.2		+0.2	-0.2		+0.2	V
Capacitance			25			25		pF
Leakage Current			± 1			± 1		μA
SYSTEM PERFORMANCE								
No Missing Codes		12			12			Bits
Integral Linearity Error			± 1.0	± 2		± 0.5	± 1	LSB ⁽¹⁾
Differential Linearity Error			± 1.0	± 2		± 0.5	-1, +2	LSB
Offset Error			± 1.0	± 3		± 0.75	± 2	LSB
Offset Error Match				± 1			± 1	LSB
Gain Error			± 1.0	± 3		± 0.75	± 2	LSB
Gain Error Match				± 1			± 1	LSB
Noise			33			33		μVRMS
Power-Supply Rejection			82			82		dB
SAMPLING DYNAMICS								
Throughput Frequency	High Speed Mode: SCL = 3.4MHz Fast Mode: SCL = 400kHz Standard Mode, SCL = 100kHz			50			50	kHz
				8			8	kHz
				2			2	kHz
Conversion Time			6			6		μs
AC ACCURACY								
Total Harmonic Distortion	$V_{IN} = 2.5V_{PP}$ at 10kHz		-82			-82		dB ⁽²⁾
Signal-to-Ratio	$V_{IN} = 2.5V_{PP}$ at 10kHz		72			72		dB
Signal-to-(Noise+Distortion) Ratio	$V_{IN} = 2.5V_{PP}$ at 10kHz		71			71		dB
Spurious-Free Dynamic Range	$V_{IN} = 2.5V_{PP}$ at 10kHz		86			86		dB
Isolation Channel-to-Channel			120			120		dB
VOLTAGE REFERENCE OUTPUT								
Range		2.475	2.5	2.525	2.475	2.5	2.525	V
Internal Reference Drift			15			15		ppm/ $^{\circ}\text{C}$
Output Impedance	Internal Reference ON		110			110		Ω
	Internal Reference OFF		1			1		G Ω
Quiescent Current	Int. Ref. ON, SCL and SDA pulled HIGH		1300			1300		μA
VOLTAGE REFERENCE INPUT								
Range		0.05		V_{DD}	0.05		V_{DD}	V
Resistance			1			1		G Ω
Current Drain	High Speed Mode: SCL = 3.4MHz		20			20		μA
DIGITAL INPUT/OUTPUT								
Logic Family		CMOS			CMOS			
Logic Levels:		$+V_{DD} \cdot 0.7$		$+V_{DD} + 0.5$	$+V_{DD} \cdot 0.7$		$+V_{DD} + 0.5$	V
		-0.3		$+V_{DD} \cdot 0.3$	-0.3		$+V_{DD} \cdot 0.3$	V
				0.4			0.4	V
Input Leakage:	Min. 3mA Sink Current			10			10	μA
	$V_{IH} = +V_{DD} + 0.5$							μA
	$V_{IL} = -0.3$							μA
Data Format		-10	Straight Binary		-10	Straight Binary		
ADS7828 HARDWARE ADDRESS			10010			10010		Binary
POWER-SUPPLY REQUIREMENTS								
Power-Supply Voltage, $+V_{DD}$	Specified Performance	4.75	5	5.25	4.75	5	5.25	V
Quiescent Current	High Speed Mode: SCL = 3.4MHz		750	1000		750	1000	μA
	Fast Mode: SCL = 400kHz		300			300		μA
	Standard Mode, SCL = 100kHz		150			150		μA
Power Dissipation	High Speed Mode: SCL = 3.4MHz		3.75	5		3.75	5	mW
	Fast Mode: SCL = 400kHz		1.5			1.5		mW
	Standard Mode, SCL = 100kHz		0.75			0.75		mW
Power-Down Mode	High Speed Mode: SCL = 3.4MHz		400			400		μA
w/Wrong Address Selected	Fast Mode: SCL = 400kHz		150			150		μA
	Standard Mode, SCL = 100kHz		35			35		μA
Full Power-Down	SCL Pulled HIGH, SDA Pulled HIGH		400	3000		400	3000	nA
TEMPERATURE RANGE								
Specified Performance		-40		+85	-40		+85	$^{\circ}\text{C}$

NOTES: (1) LSB means Least Significant Bit. With V_{REF} equal to 5.0V, 1LSB is 1.22mV.

(2) THD measured out to the 9th-harmonic.

TIMING DIAGRAM



TIMING CHARACTERISTICS(1)

At $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $+V_{DD} = +2.7\text{V}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
SCL Clock Frequency	f_{SCL}	Standard Mode Fast Mode High-Speed Mode, $C_B = 100\text{pF}$ max High-Speed Mode, $C_B = 400\text{pF}$ max		100 400 3.4 1.7	kHz kHz MHz MHz
Bus Free Time Between a STOP and START Condition	t_{BUF}	Standard Mode Fast Mode	4.7 1.3		μs μs
Hold Time (Repeated) START Condition	$t_{\text{HD:STA}}$	Standard Mode Fast Mode High-Speed Mode	4.0 600 160		μs ns ns
LOW Period of the SCL Clock	t_{LOW}	Standard Mode Fast Mode High-Speed Mode, $C_B = 100\text{pF}$ max ⁽²⁾ High-Speed Mode, $C_B = 400\text{pF}$ max ⁽²⁾	4.7 1.3 160 320		μs μs ns ns
HIGH Period of the SCL Clock	t_{HIGH}	Standard Mode Fast Mode High-Speed Mode, $C_B = 100\text{pF}$ max ⁽²⁾ High-Speed Mode, $C_B = 400\text{pF}$ max ⁽²⁾	4.0 600 60 120		μs ns ns ns
Setup Time for a Repeated START Condition	$t_{\text{SU:STA}}$	Standard Mode Fast Mode High-Speed Mode	4.7 600 160		μs ns ns
Data Setup Time	$t_{\text{SU:DAT}}$	Standard Mode Fast Mode High-Speed Mode	250 100 10		ns ns ns
Data Hold Time	$t_{\text{HD:DAT}}$	Standard Mode Fast Mode High-Speed Mode, $C_B = 100\text{pF}$ max ⁽²⁾ High-Speed Mode, $C_B = 400\text{pF}$ max ⁽²⁾	0 0 0 ⁽³⁾ 0 ⁽³⁾	3.45 0.9 70 150	μs μs ns ns
Rise Time of SCL Signal	t_{RCL}	Standard Mode Fast Mode High-Speed Mode, $C_B = 100\text{pF}$ max ⁽²⁾ High-Speed Mode, $C_B = 400\text{pF}$ max ⁽²⁾	$20 + 0.1C_B$ 10 10 20	1000 300 40 80	ns ns ns ns
Rise Time of SCL Signal After a Repeated START Condition and After an Acknowledge Bit	t_{RCL1}	Standard Mode Fast Mode High-Speed Mode, $C_B = 100\text{pF}$ max ⁽²⁾ High-Speed Mode, $C_B = 400\text{pF}$ max ⁽²⁾	$20 + 0.1C_B$ 10 10 20	1000 300 80 160	ns ns ns ns
Fall Time of SCL Signal	t_{FCL}	Standard Mode Fast Mode High-Speed Mode, $C_B = 100\text{pF}$ max ⁽²⁾ High-Speed Mode, $C_B = 400\text{pF}$ max ⁽²⁾	$20 + 0.1C_B$ 10 10 20	300 300 40 80	ns ns ns ns

NOTES: (1) All values referred to V_{IHMIN} and V_{ILMAX} levels.

(2) For bus line loads C_B between 100pF and 400pF the timing parameters must be linearly interpolated.

(3) A device must internally provide a data hold time to bridge the undefined part between V_{IH} and V_{IL} of the falling edge of the SCLH signal. An input circuit with a threshold as low as possible for the falling edge of the SCLH signal minimizes this hold time.

TIMING CHARACTERISTICS⁽¹⁾ (Cont.)

At $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $+V_{DD} = +2.7\text{V}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Rise Time of SDA Signal	t_{RDA}	Standard Mode		1000	ns
		Fast Mode	$20 + 0.1C_B$	300	ns
		High-Speed Mode, $C_B = 100\text{pF}$ max ⁽²⁾	10	80	ns
		High-Speed Mode, $C_B = 400\text{pF}$ max ⁽²⁾	20	160	ns
Fall Time of SDA Signal	t_{FDA}	Standard Mode		300	ns
		Fast Mode	$20 + 0.1C_B$	300	ns
		High-Speed Mode, $C_B = 100\text{pF}$ max ⁽²⁾	10	80	ns
		High-Speed Mode, $C_B = 400\text{pF}$ max ⁽²⁾	20	160	ns
Setup Time for STOP Condition	$t_{SU; STO}$	Standard Mode	4.0		μs
		Fast Mode	600		ns
		High-Speed Mode	160		ns
Capacitive Load for SDA and SCL Line	C_B			400	pF
Pulse Width of Spike Suppressed	t_{SP}	Fast Mode		50	ns
		High-Speed Mode		10	ns
Noise Margin at the HIGH Level for Each Connected Device (Including Hysteresis)	V_{NH}	Standard Mode			
		Fast Mode	$0.2V_{DD}$		V
		High-Speed Mode			
Noise Margin at the LOW Level for Each Connected Device (Including Hysteresis)	V_{NL}	Standard Mode			
		Fast Mode	$0.1V_{DD}$		V
		High-Speed Mode			

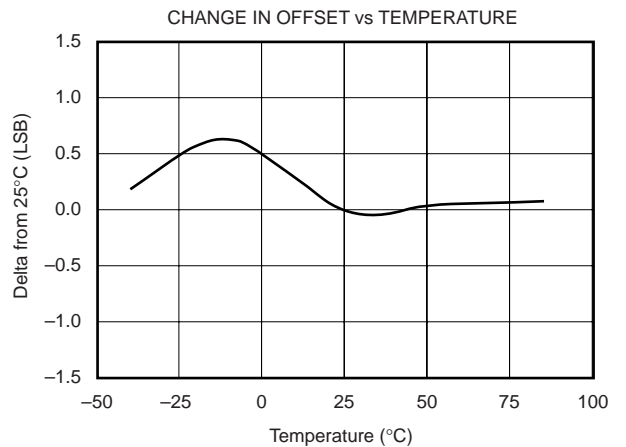
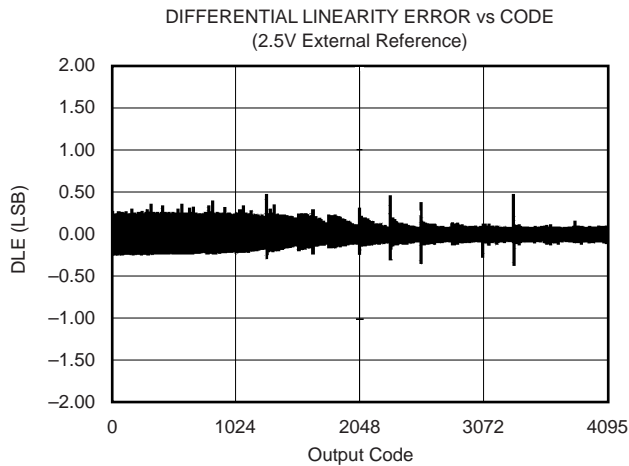
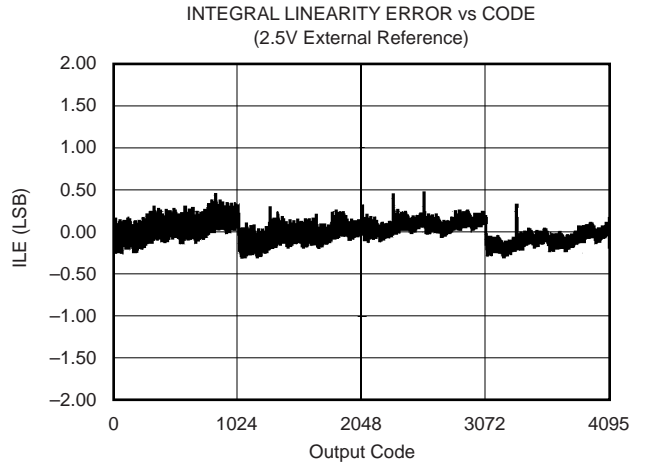
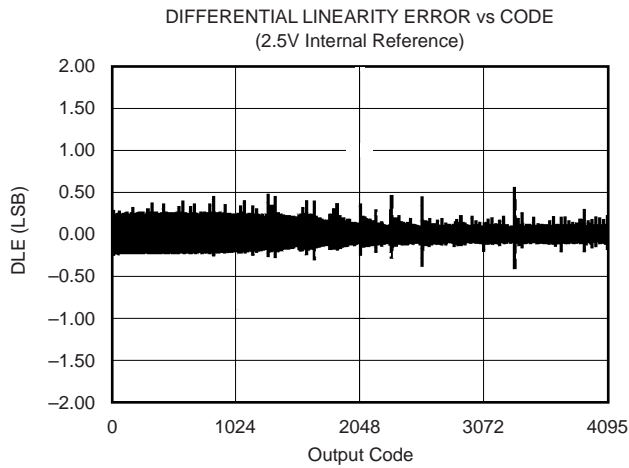
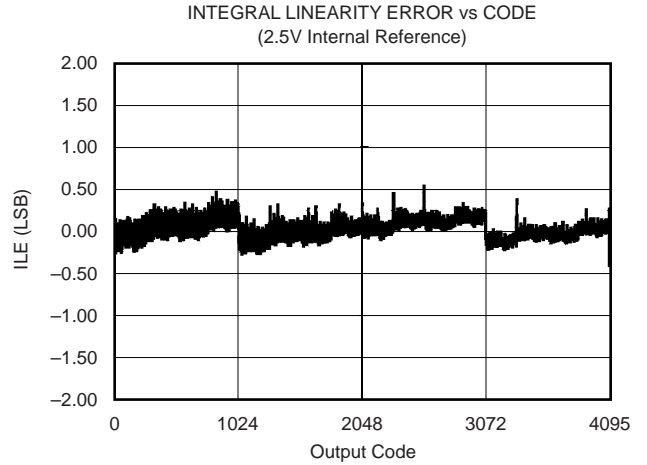
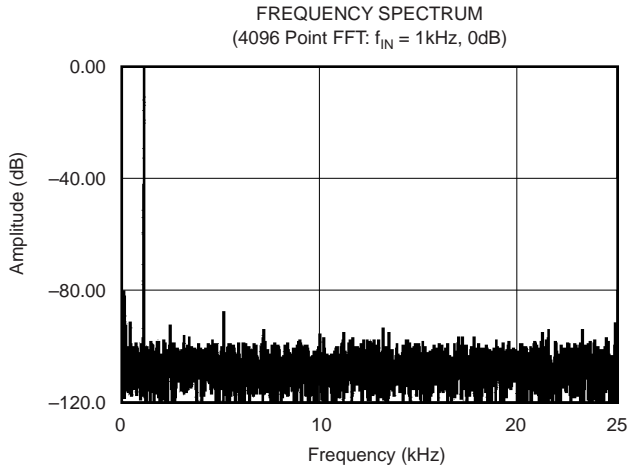
NOTES: (1) All values referred to V_{IHMIN} and V_{ILMAX} levels.

(2) For bus line loads C_B between 100pF and 400pF the timing parameters must be linearly interpolated.

(3) A device must internally provide a data hold time to bridge the undefined part between V_{IH} and V_{IL} of the falling edge of the SCLH signal. An input circuit with a threshold as low as possible for the falling edge of the SCLH signal minimizes this hold time.

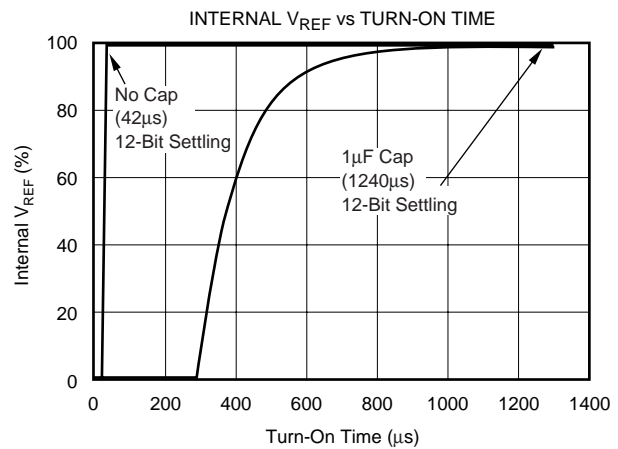
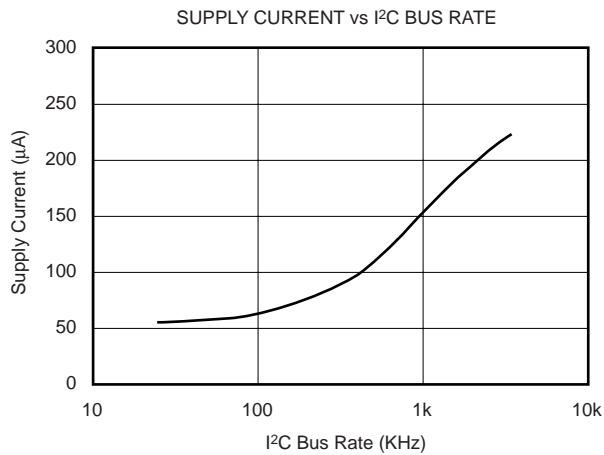
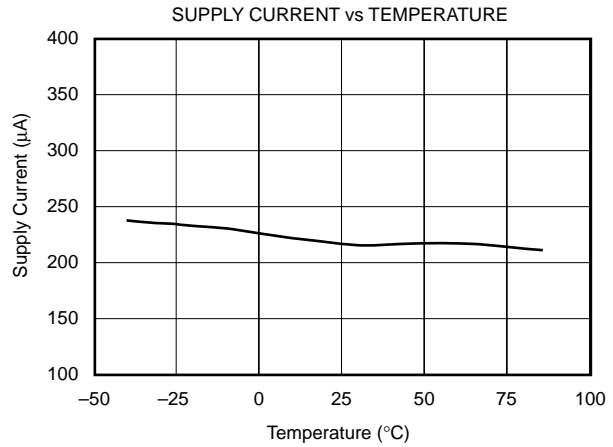
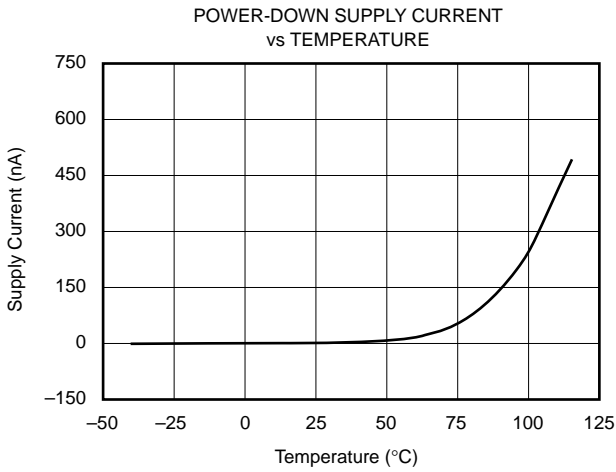
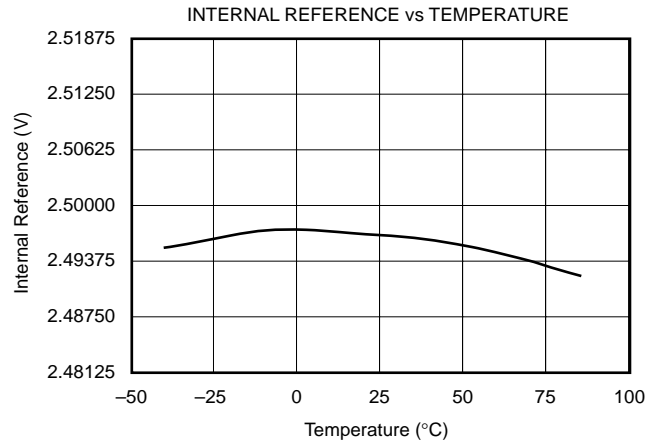
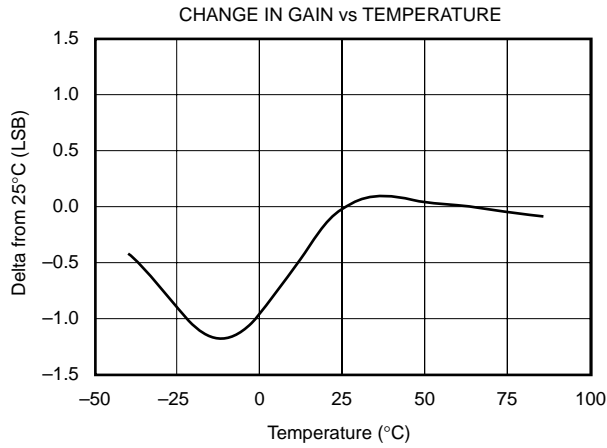
TYPICAL CHARACTERISTICS

$T_A = +25^\circ\text{C}$, $V_{DD} = +2.7\text{V}$, $V_{REF} = \text{External } +2.5\text{V}$, $f_{\text{SAMPLE}} = 50\text{kHz}$, unless otherwise noted.



TYPICAL CHARACTERISTICS (Cont.)

$T_A = +25^\circ\text{C}$, $V_{DD} = +2.7\text{V}$, $V_{REF} = \text{External } +2.5\text{V}$, $f_{\text{SAMPLE}} = 50\text{kHz}$, unless otherwise noted.



THEORY OF OPERATION

The ADS7828 is a classic Successive Approximation Register (SAR) A/D converter. The architecture is based on capacitive redistribution which inherently includes a sample-and-hold function. The converter is fabricated on a 0.6 μ m CMOS process.

The ADS7828 core is controlled by an internally generated free-running clock. When the ADS7828 is not performing conversions or being addressed, it keeps the A/D converter core powered off, and the internal clock does not operate.

The simplified diagram of input and output for the ADS7828 is shown in Figure 1.

ANALOG INPUT

When the converter enters the hold mode, the voltage on the selected CHx pin is captured on the internal capacitor array. The input current on the analog inputs depends on the conversion rate of the device. During the sample period, the source must charge the internal sampling capacitor (typically 25pF). After the capacitor has been fully charged, there is no further input current. The amount of charge transfer from the analog source to the converter is a function of conversion rate.

REFERENCE

The ADS7828 can operate with an internal 2.5V reference or an external reference. If a +5V supply is used, an external +5V reference is required in order to provide full dynamic range for a 0V to +V_{DD} analog input. This external reference can be as low as 50mV. When using a +2.7V supply, the

internal +2.5V reference will provide full dynamic range for a 0V to +V_{DD} analog input.

As the reference voltage is reduced, the analog voltage weight of each digital output code is reduced. This is often referred to as the LSB (least significant bit) size and is equal to the reference voltage divided by 4096. This means that any offset or gain error inherent in the A/D converter will appear to increase, in terms of LSB size, as the reference voltage is reduced.

The noise inherent in the converter will also appear to increase with lower LSB size. With a 2.5V reference, the internal noise of the converter typically contributes only 0.32LSB peak-to-peak of potential error to the output code. When the external reference is 50mV, the potential error contribution from the internal noise will be 50 times larger—16LSBs. The errors due to the internal noise are Gaussian in nature and can be reduced by averaging consecutive conversion results.

DIGITAL INTERFACE

The ADS7828 supports the I²C serial bus and data transmission protocol, in all three defined modes: standard, fast, and high-speed. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a “master.” The devices that are controlled by the master are “slaves.” The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The ADS7828 operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O lines SDA and SCL.

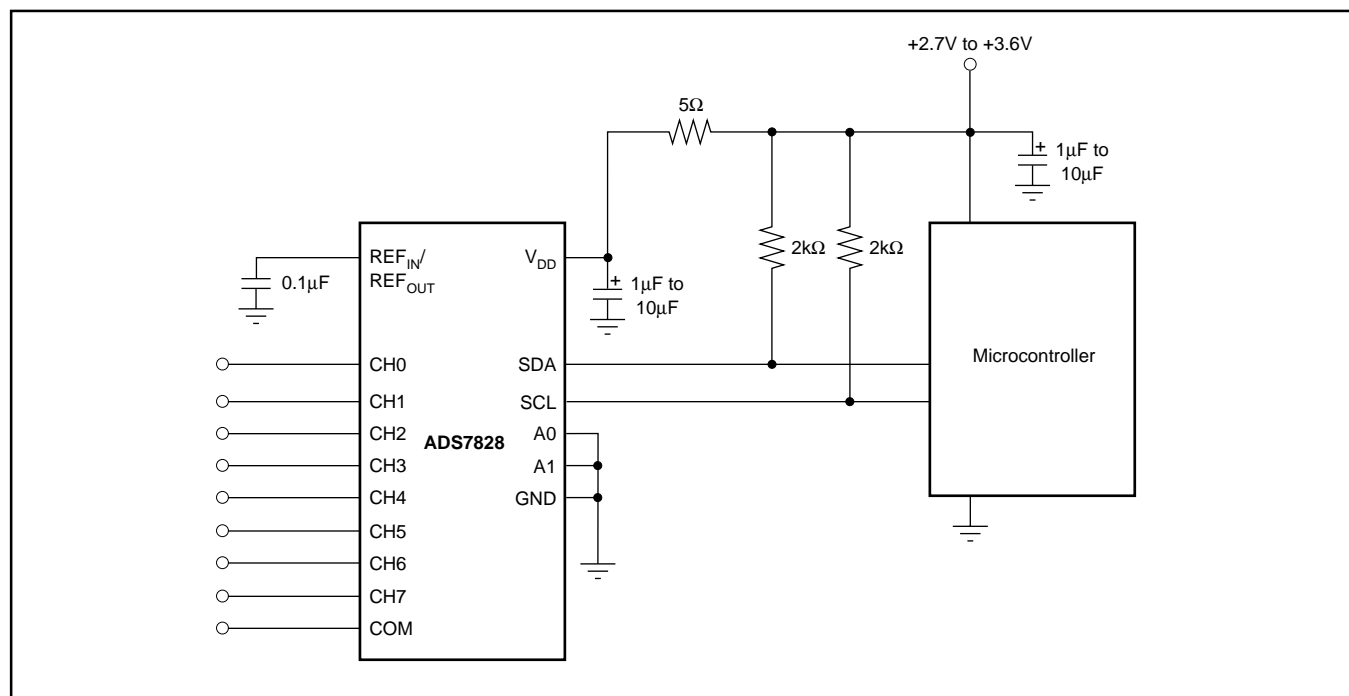


FIGURE 1. Simplified I/O of the ADS7828.

The following bus protocol has been defined (as shown in Figure 2):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus Not Busy: Both data and clock lines remain HIGH.

Start Data Transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop Data Transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data Valid: The state of the data line represents valid data, when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth-bit.

Within the I²C bus specifications a standard mode (100kHz clock rate), a fast mode (400kHz clock rate), and a high-speed mode (3.4MHz clock rate) are defined. The ADS7828 works in all three modes.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Of course, setup and hold times

must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Figure 2 details how data transfer is accomplished on the I²C bus. Depending upon the state of the R/W bit, two types of data transfer are possible:

- 1. Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after the slave address and each received byte.
- 2. Data transfer from a slave transmitter to a master receiver.** The first byte, the slave address, is transmitted by the master. The slave then returns an acknowledge bit. Next, a number of data bytes are transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a not-acknowledge is returned.

The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

The ADS7828 may operate in the following two modes:

- **Slave Receiver Mode:** Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.
- **Slave Transmitter Mode:** The first byte (the slave address) is received and handled as in the slave receiver mode. However, in this mode the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the ADS7828 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

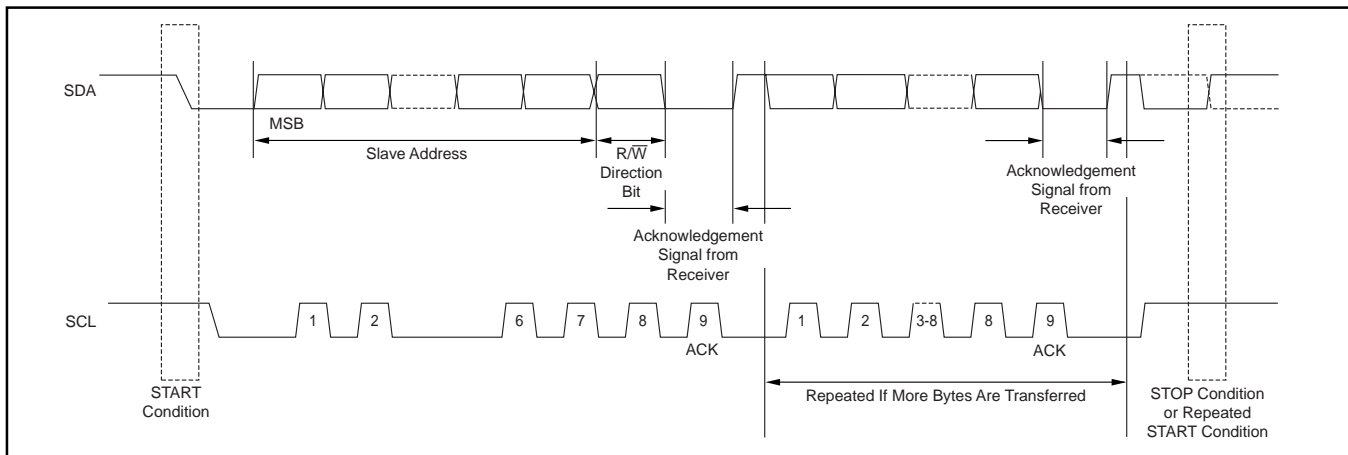


FIGURE 2. Basic Operation of the ADS7828.

ADDRESS BYTE

MSB	6	5	4	3	2	1	LSB
1	0	0	1	0	A1	A0	R/W

The address byte is the first byte received following the START condition from the master device. The first five bits (MSBs) of the slave address are factory pre-set to 10010. The next two bits of the address byte are the device select bits, A1 and A0. Input pins (A1-A0) on the ADS7828 determine these two bits of the device address for a particular ADS7828. A maximum of four devices with the same pre-set code can therefore be connected on the same bus at one time.

The A1-A0 Address Inputs can be connected to V_{DD} or digital ground. The device address is set by the state of these pins upon power-up of the ADS7828.

The last bit of the address byte (R/\overline{W}) defines the operation to be performed. When set to a '1' a read operation is selected; when set to a '0' a write operation is selected. Following the START condition the ADS7828 monitors the SDA bus, checking the device type identifier being transmitted. Upon receiving the 10010 code, the appropriate device select bits, and the R/\overline{W} bit, the slave device outputs an acknowledge signal on the SDA line.

COMMAND BYTE

MSB	6	5	4	3	2	1	LSB
SD	C2	C1	C0	PD1	PD0	X	X

The ADS7828 operating mode is determined by a command byte which is illustrated above.

SD: Single-Ended/Differential Inputs

0: Differential Inputs

1: Single-Ended Inputs

C2 - C0: Channel Selections

PD1 - 0: Power-Down Selection

X: Unused

See Table I for a power-down selection summary.

See Table II for a channel selection control summary.

PD1	PD0	DESCRIPTION
0	0	Power Down Between A/D Converter Conversions
0	1	Internal Reference OFF and A/D Converter ON
1	0	Internal Reference ON and A/D Converter OFF
1	1	Internal Reference ON and A/D Converter ON

TABLE I. Power-Down Selection

CHANNEL SELECTION CONTROL												
SD	C2	C1	C0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	COM
0	0	0	0	+IN	-IN	—	—	—	—	—	—	—
0	0	0	1	—	—	+IN	-IN	—	—	—	—	—
0	0	1	0	—	—	—	—	+IN	-IN	—	—	—
0	0	1	1	—	—	—	—	—	—	+IN	-IN	—
0	1	0	0	-IN	+IN	—	—	—	—	—	—	—
0	1	0	1	—	—	-IN	+IN	—	—	—	—	—
0	1	1	0	—	—	—	—	-IN	+IN	—	—	—
0	1	1	1	—	—	—	—	—	—	-IN	+IN	—
1	0	0	0	+IN	—	—	—	—	—	—	—	-IN
1	0	0	1	—	—	+IN	—	—	—	—	—	-IN
1	0	1	0	—	—	—	—	+IN	—	—	—	-IN
1	0	1	1	—	—	—	—	—	—	+IN	—	-IN
1	1	0	0	—	+IN	—	—	—	—	—	—	-IN
1	1	0	1	—	—	—	+IN	—	—	—	—	-IN
1	1	1	0	—	—	—	—	—	—	+IN	—	-IN
1	1	1	1	—	—	—	—	—	—	—	+IN	-IN

TABLE II. Channel Selection Control Addressed by Command Byte.

INITIATING CONVERSION

Provided the master has write-addressed it, the ADS7828 turns on the A/D converter's section and begins conversions when it receives BIT 4 of the command byte shown in the Command Byte. If the command byte is correct, the ADS7828 will return an ACK condition.

READING DATA

Data can be read from the ADS7828 by read-addressing the part (LSB of address byte set to 1) and receiving the transmitted bytes. Converted data can only be read from the ADS7828 once a conversion has been initiated as described in the preceding section.

Each 12-bit data word is returned in two bytes, as shown below, where D11 is the MSB of the data word, and D0 is the LSB. Byte 0 is sent first, followed by Byte 1.

	MSB	6	5	4	3	2	1	LSB
BYTE 0	0	0	0	0	D11	D10	D9	D8
BYTE 1	D7	D6	D5	D4	D3	D2	D1	D0

READING IN F/S MODE

Figure 3 describes the interaction between the master and the slave ADS7828 in Fast or Standard (F/S) mode. At the end of reading conversion data the ADS7828 can be issued a repeated START condition by the master to secure bus operation for subsequent conversions of the A/D converter. This would be the most efficient way to perform continuous conversions.

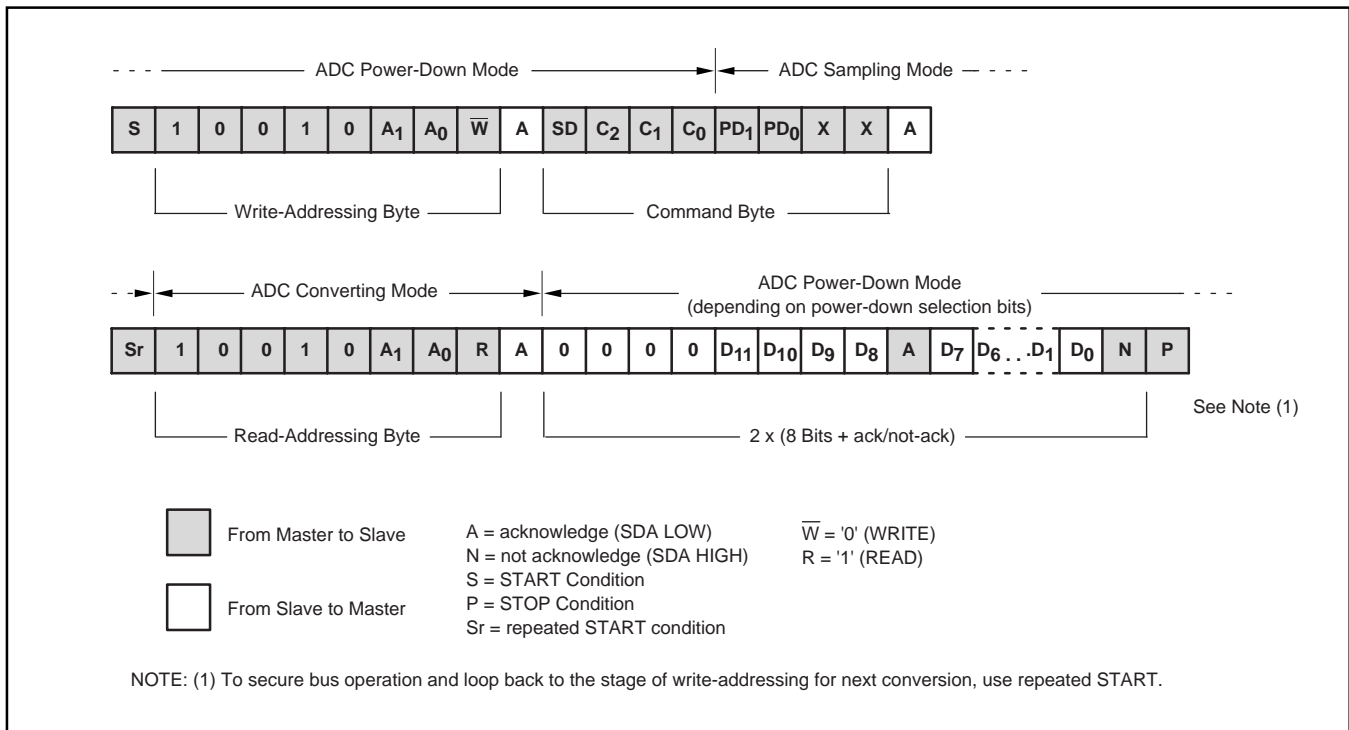


FIGURE 3. Typical Read Sequence in F/S Mode.

READING IN HS MODE

High Speed (HS) mode is fast enough that codes can be read out one at a time. In HS mode, there is not enough time for a single conversion to complete between the reception of a repeated START condition and the read-addressing byte, so the ADS7828 stretches the clock after the read-addressing byte has been fully received, holding it LOW until the conversion is complete.

See Figure 4 for a typical read sequence for HS mode. Included in the read sequence is the shift from F/S to HS modes. It may be desirable to remain in HS mode after reading a conversion; to do this, issue a repeated START instead of a STOP at the end of the read sequence, since a STOP causes the part to return to F/S mode.

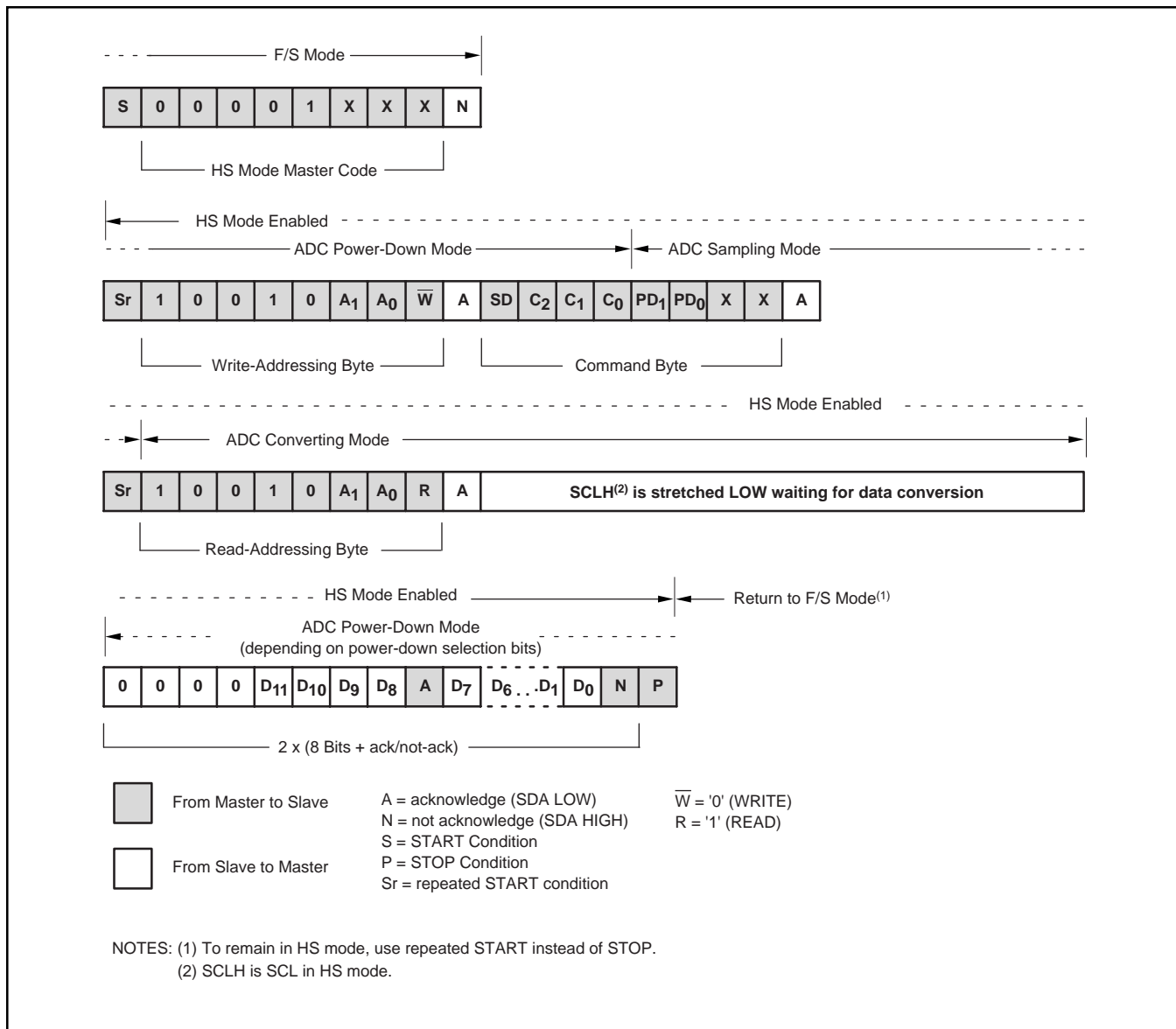


FIGURE 4. Typical Read Sequence in HS Mode.

READING WITH REFERENCE ON/OFF

The internal reference defaults to off when the ADS7828 power is on. To turn the internal reference on or off, see Table I. If the reference (internal or external) is constantly turned on and off, a proper amount of settling time must be added before a normal conversion cycle can be started. The exact amount of settling time needed varies depending on the configuration.

See Figure 5 for an example of the proper internal reference turn-on sequence before issuing the typical read sequences required for the F/S mode when an internal reference is used.

When using an internal reference, there are three things that must be done:

- 1) In order to use the internal reference, the PD1 bit of Command Byte must always be set to logic '1' for each sample conversion that is issued by the sequence, as shown in Figure 3.
- 2) In order to achieve 12-bit accuracy conversion when using the internal reference, the internal reference settling time must be considered, as shown in the

Internal V_{REF} vs Turn-On Time Typical Characteristic plot. If the PD1 bit has been set to logic '0' while using the ADS7828, then the settling time must be reconsidered after PD1 is set to logic '1'. In other words, whenever the internal reference is turned on after it has been turned off, the settling time must be long enough to get 12-bit accuracy conversion.

- 3) When the internal reference is off, it is not turned on until both the first Command Byte with PD1 = '1' is sent *and then* a STOP condition or repeated START condition is issued. (The actual turn-on time occurs once the STOP or repeated START condition is issued.) Any Command Byte with PD1 = '1' issued after the internal reference is turned on serves only to keep the internal reference on. Otherwise, the internal reference would be turned off by any Command Byte with PD1 = '0'.

The example in Figure 5 can be generalized for a HS mode conversion cycle by simply swapping the timing of the conversion cycle.

If using an external reference, PD1 must be set to '0', and the external reference must be settled. The typical sequence in Figure 3 or Figure 4 can then be used.

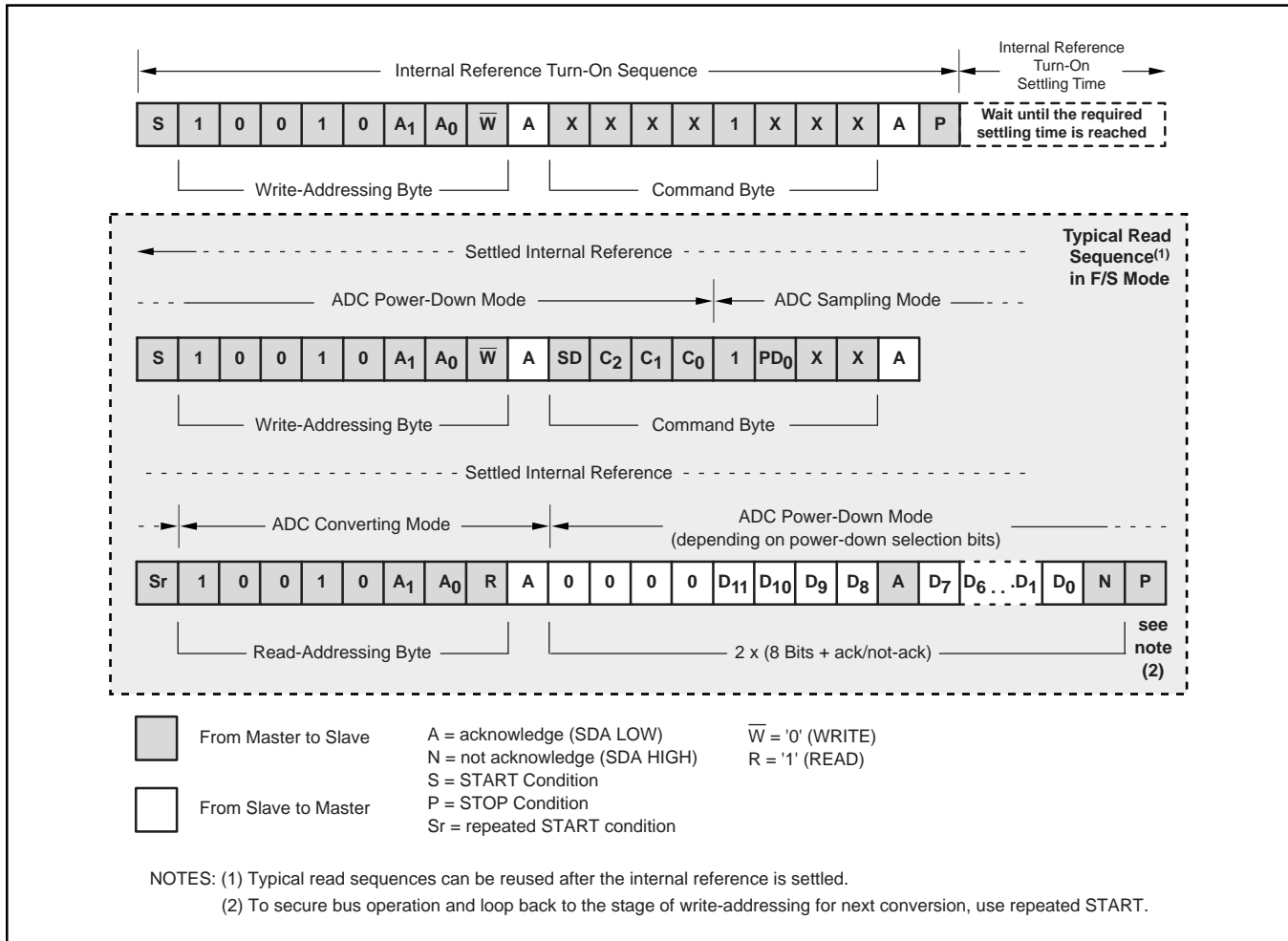


FIGURE 5. Internal Reference Turn-On Sequence and Typical Read Sequence (F/S mode shown).

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS7828 circuitry. The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Therefore, during any single conversion for an “n-bit” SAR converter, there are n “windows” in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high-power devices.

With this in mind, power to the ADS7828 should be clean and well-bypassed. A 0.1 μ F ceramic bypass capacitor should be placed as close to the device as possible. A 1 μ F to 10 μ F capacitor may also be needed if the impedance of the connection between +V_{DD} and the power supply is high.

The ADS7828 architecture offers no inherent rejection of noise or voltage variation in regards to using an external reference input. This is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply will appear directly in the digital results. While high-frequency noise can be filtered out, voltage variation due to line frequency (50Hz or 60Hz) can be difficult to remove.

The GND pin should be connected to a clean ground point. In many cases, this will be the “analog” ground. Avoid connections that are too near the grounding point of a microcontroller or digital signal processor. The ideal layout will include an analog ground plane dedicated to the converter and associated analog circuitry.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS7828E/250	Active	Production	TSSOP (PW) 16	250 SMALL T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 85	ADS 7828E
ADS7828E/250.B	Active	Production	TSSOP (PW) 16	250 SMALL T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 85	ADS 7828E
ADS7828E/250G4	Active	Production	TSSOP (PW) 16	250 SMALL T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 85	ADS 7828E
ADS7828E/2K5	Active	Production	TSSOP (PW) 16	2500 LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 85	ADS 7828E
ADS7828E/2K5.B	Active	Production	TSSOP (PW) 16	2500 LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 85	ADS 7828E
ADS7828E/2K5G4	Active	Production	TSSOP (PW) 16	2500 LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 85	ADS 7828E
ADS7828EB/250	Active	Production	TSSOP (PW) 16	250 SMALL T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 85	ADS 7828E
ADS7828EB/250.B	Active	Production	TSSOP (PW) 16	250 SMALL T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 85	ADS 7828E
ADS7828EB/250G4	Active	Production	TSSOP (PW) 16	250 SMALL T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 85	ADS 7828E
ADS7828EB/2K5	Active	Production	TSSOP (PW) 16	2500 LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 85	ADS 7828E
ADS7828EB/2K5.B	Active	Production	TSSOP (PW) 16	2500 LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 85	ADS 7828E

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

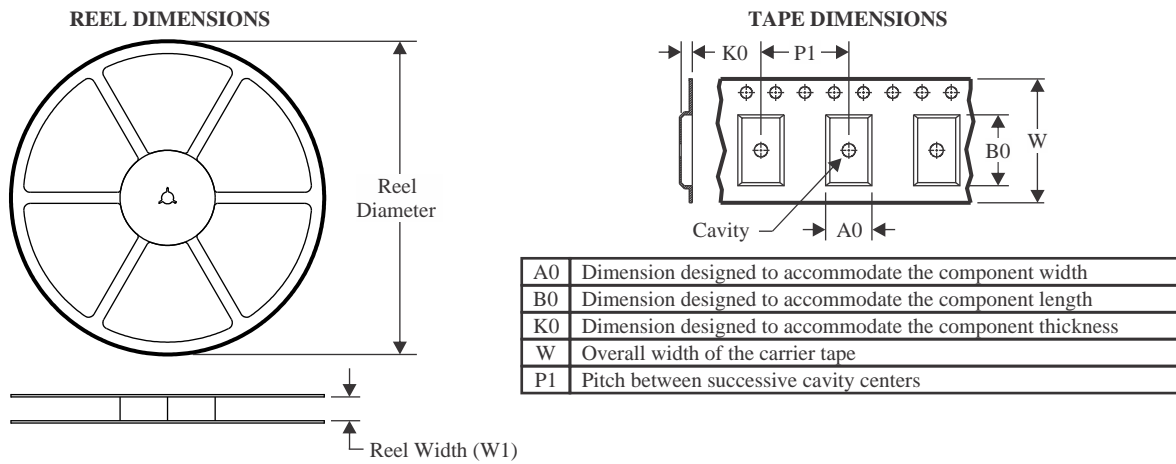
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF ADS7828 :

- Automotive : [ADS7828-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7828E/250	TSSOP	PW	16	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
ADS7828E/2K5	TSSOP	PW	16	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
ADS7828EB/250	TSSOP	PW	16	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
ADS7828EB/2K5	TSSOP	PW	16	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7828E/250	TSSOP	PW	16	250	213.0	191.0	35.0
ADS7828E/2K5	TSSOP	PW	16	2500	353.0	353.0	32.0
ADS7828EB/250	TSSOP	PW	16	250	213.0	191.0	35.0
ADS7828EB/2K5	TSSOP	PW	16	2500	353.0	353.0	32.0



4220204/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2025, Texas Instruments Incorporated