

ADS7046 12-Bit, 3-MSPS, Single-Ended Input, Small-Size, Low-Power SAR ADC

1 Features

- 3-MSPS Throughput
- Small Package Size:
 - X2QFN-8 Package (1.5 mm × 1.5 mm)
- Unipolar Input Range: 0 V to AVDD
- Wide Operating Range:
 - AVDD: 2.35 V to 3.6 V
 - DVDD: 1.65 V to 3.6 V (Independent of AVDD)
 - Temperature Range: –40°C to +125°C
- Excellent Performance:
 - 12-Bit NMC DNL, ±0.3-LSB INL
 - 71.2-dB SINAD at 2 kHz
 - 69.5-dB SINAD at 1 MHz
- Low Power Consumption:
 - 3.8 mW at 3 MSPS With 3.3-V AVDD
 - 115 µW at 100 kSPS With 3.3-V AVDD
 - 67 µW at 100 kSPS With 2.5-V AVDD
- Integrated Offset Calibration
- SPI-Compatible Serial Interface: 60 MHz
- JESD8-7A Compliant Digital I/O

2 Applications

- Optical Encoders
- Sonar Receivers
- Fish Finders
- I-Q Demodulators
- Optical Line Cards and Modules
- Thermal Imaging Cameras
- Ultrasonic Flow Meters
- Handheld Radios

3 Description

The ADS7046 device belongs to a family of pin-to-pin compatible, high-speed, low-power, single-channel successive-approximation register (SAR) type analog-to-digital converters (ADCs). The device family includes multiple resolutions, throughputs, and analog input variants (see [Table 1](#) for a list of devices).

The ADS7046 is a 12-bit, 3-MSPS SAR ADC that supports a single-ended input in the range of 0 V to AVDD, for AVDD in the range of 2.35 V to 3.6 V.

The internal offset calibration feature maintains excellent offset specifications over the entire AVDD and temperature operating range.

The device supports an SPI-compatible serial interface that is controlled by the \overline{CS} and SCLK signals. The input signal is sampled with the \overline{CS} falling edge and SCLK is used for both conversion and serial data output. The device supports a wide digital supply range (1.65 V to 3.6 V), enabling direct interfacing to a variety of host controllers. The ADS7046 complies with the JESD8-7A standard for a normal DVDD range (1.65 V to 1.95 V).

The ADS7046 is available in an 8-pin, small, X2QFN package and is specified over the extended industrial temperature range (–40°C to +125°C). The small form-factor and extremely-low power consumption make this device suitable for space-constrained and battery-powered applications that require high-speed, high-resolution data acquisition.

Device Information⁽¹⁾

PART NAME	PACKAGE	BODY SIZE (NOM)
ADS7046	X2QFN (8)	1.50 mm × 1.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application

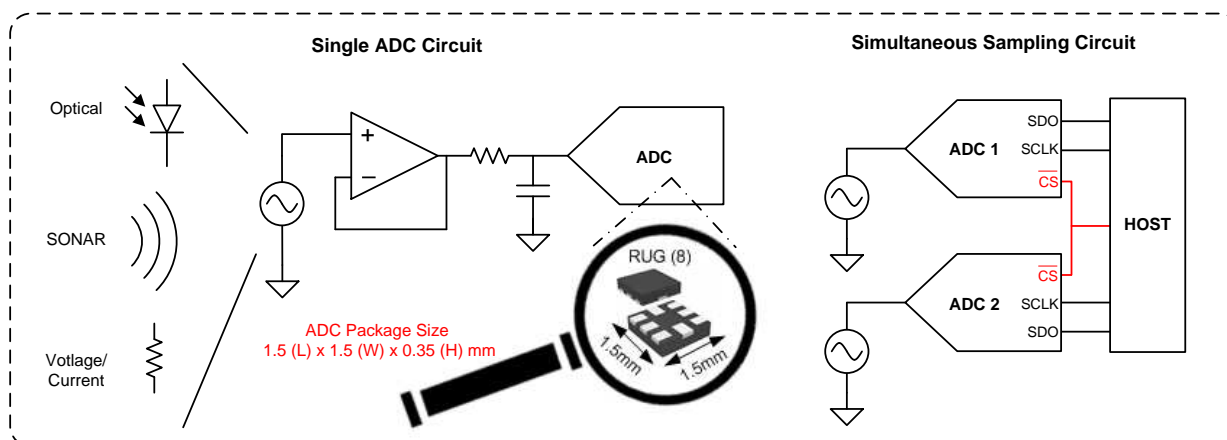


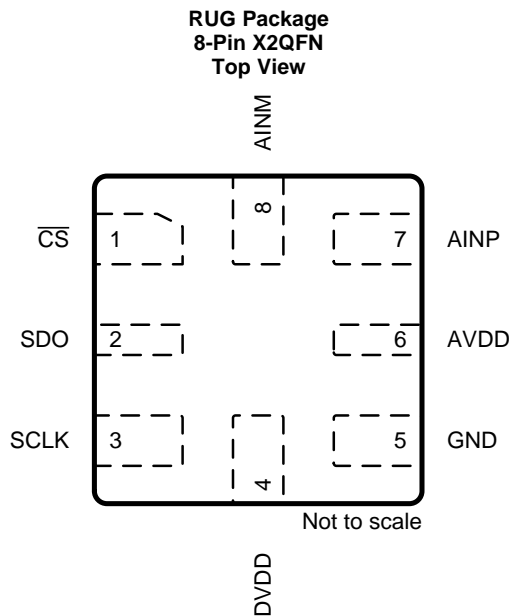
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4 Revision History

DATE	REVISION	NOTES
December 2017	*	Initial release.

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	$\overline{\text{CS}}$	Digital input	Chip-select signal, active low
2	SDO	Digital output	Serial data out
3	SCLK	Digital input	Serial clock
4	DVDD	Supply	Digital I/O supply voltage
5	GND	Supply	Ground for power supply, all analog and digital signals are referred to this pin
6	AVDD	Supply	Analog power-supply input, also provides the reference voltage to the ADC
7	AINP	Analog input	Analog signal input, positive
8	AINM	Analog input	Analog signal input, negative

6 Specifications

6.1 Absolute Maximum Ratings⁽¹⁾

	MIN	MAX	UNIT
AVDD to GND	−0.3	3.9	V
DVDD to GND	−0.3	3.9	V
AINP to GND	−0.3	AVDD + 0.3	V
AINM to GND	−0.3	0.3	V
Input current to any pin except supply pins	−10	10	mA
Digital input voltage to GND	−0.3	DVDD + 0.3	V
Storage temperature, T _{stg}	−60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
AVDD	Analog supply voltage range	2.35	3.3	3.6	V
DVDD	Digital supply voltage range	1.65	1.8	3.6	V
T _A	Operating free-air temperature	−40	25	125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		ADS7046	UNIT
		RUG (X2QFN)	
		8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	177.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	51.5	°C/W
R _{θJB}	Junction-to-board thermal resistance	76.7	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	1	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	76.7	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

at $V_{DD} = 3.3\text{ V}$, $DVDD = 1.65\text{ V to }3.6\text{ V}$, $f_{\text{sample}} = 3\text{ MSPS}$, and $V_{\text{AINM}} = 0\text{ V}$ (unless otherwise noted); minimum and maximum values for $T_A = -40^\circ\text{C to }+125^\circ\text{C}$; typical values at $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
ANALOG INPUT							
Full-scale input voltage span ⁽¹⁾		0		AVDD	V		
Absolute input voltage range	AINP to GND	-0.1		AVDD + 0.1	V		
	AINM to GND	-0.1		0.1			
C_S	Sampling capacitance		16		pF		
SYSTEM PERFORMANCE							
Resolution			12		Bits		
NMC	No missing codes	12			Bits		
INL ⁽²⁾	Integral nonlinearity	-1	±0.3	1	LSB ⁽³⁾		
DNL	Differential nonlinearity	-0.5	±0.15	0.5	LSB		
E_O ⁽²⁾	Offset error	After calibration ⁽⁴⁾		-3	±1	3	LSB
dV_{OS}/dT	Offset error drift with temperature		1.75			ppm/°C	
E_G ⁽²⁾	Gain error	-0.1	±0.01	0.1		%FS	
	Gain error drift with temperature		0.5			ppm/°C	
SAMPLING DYNAMICS							
t_{CONV}	Conversion time		15 × t_{SCLK}		ns		
t_{ACQ}	Acquisition time	80			ns		
f_{SAMPLE}	Maximum throughput rate	60-MHz SCLK, AVDD = 2.35 V to 3.6 V		3	MHz		
	Aperture delay		3		ns		
	Aperture jitter, RMS		12		ps		
DYNAMIC CHARACTERISTICS							
SNR	Signal-to-noise ratio ⁽⁵⁾	AVDD = 3.3 V, $f_{\text{IN}} = 2\text{ kHz}$	69	71.2	dB		
		AVDD = 2.5 V, $f_{\text{IN}} = 2\text{ kHz}$		70.4			
THD	Total harmonic distortion ⁽⁵⁾⁽⁶⁾	$f_{\text{IN}} = 2\text{ kHz}$		-86	dB		
		$f_{\text{IN}} = 500\text{ kHz}$		-85			
		$f_{\text{IN}} = 1000\text{ kHz}$		-84.5			
SINAD	Signal-to-noise and distortion ⁽⁵⁾	$f_{\text{IN}} = 2\text{ kHz}$	69	71.1	dB		
		$f_{\text{IN}} = 500\text{ kHz}$		70.9			
		$f_{\text{IN}} = 1000\text{ kHz}$		70.8			
SFDR	Spurious-free dynamic range ⁽⁵⁾	$f_{\text{IN}} = 2\text{ kHz}$		90	dB		
		$f_{\text{IN}} = 500\text{ kHz}$		90			
		$f_{\text{IN}} = 1000\text{ kHz}$		88			
$BW_{(fp)}$	Full-power bandwidth	At -3 dB		200	MHz		

(1) Ideal input span; does not include gain or offset error.

(2) See [Figure 31](#), [Figure 29](#), and [Figure 30](#) for statistical distribution data for INL, offset error, and gain error.

(3) LSB means least significant bit.

(4) See the [OFFCAL State](#) section for details.

(5) All specifications expressed in decibels (dB) refer to the full-scale input (FSR) and are tested with an input signal 0.5 dB below full-scale, unless otherwise noted.

(6) Calculated on the first nine harmonics of the input frequency.

Electrical Characteristics (continued)

at AVDD = 3.3 V, DVDD = 1.65 V to 3.6 V, $f_{\text{sample}} = 3 \text{ MSPS}$, and $V_{\text{AINM}} = 0 \text{ V}$ (unless otherwise noted); minimum and maximum values for $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$; typical values at $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
DIGITAL INPUT/OUTPUT (CMOS Logic Family)						
V_{IH}	High-level input voltage ⁽⁷⁾		0.65 DVDD	DVDD + 0.3	V	
V_{IL}	Low-level input voltage ⁽⁷⁾		-0.3	0.35 DVDD	V	
V_{OH}	High-level output voltage ⁽⁷⁾	At $I_{\text{source}} = 500 \mu\text{A}$	0.8 DVDD	DVDD	V	
		At $I_{\text{source}} = 2 \text{ mA}$	DVDD - 0.45	DVDD		
V_{OL}	Low-level output voltage ⁽⁷⁾	At $I_{\text{sink}} = 500 \mu\text{A}$	0	0.2 DVDD	V	
		At $I_{\text{sink}} = 2 \text{ mA}$	0	0.45		
POWER-SUPPLY REQUIREMENTS						
AVDD	Analog supply voltage		2.35	3	3.6	V
DVDD	Digital I/O supply voltage		1.65	3	3.6	V
I_{AVDD}	Analog supply current	AVDD = 3.3 V, $f_{\text{SAMPLE}} = 3 \text{ MSPS}$		1150	1300	μA
		AVDD = 3.3 V, $f_{\text{SAMPLE}} = 100 \text{ kSPS}$		36	45	
		AVDD = 3.3 V, $f_{\text{SAMPLE}} = 10 \text{ kSPS}$		5		
		AVDD = 2.5 V, $f_{\text{SAMPLE}} = 3 \text{ MSPS}$		800		
		Static current with $\overline{\text{CS}}$ and SCLK high		0.02		
I_{DVDD}	Digital supply current	DVDD = 1.8 V, CS $\overline{\text{DO}} = 20 \text{ pF}$, output code = AAAh ⁽⁸⁾		650		μA
		DVDD = 1.8 V, static current with $\overline{\text{CS}}$ and SCLK high		0.01		

(7) Digital voltage levels comply with the JESD8-7A standard for DVDD from 1.65 V to 1.95 V; see the [Parameter Measurement Information](#) section for details.

(8) See the [Estimating Digital Power Consumption](#) section for details.

6.6 Timing Requirements

all specifications are at AVDD = 2.35 V to 3.6 V, DVDD = 1.65 V to 3.6 V, and C_{LOAD-SDO} = 20 pF (unless otherwise noted); minimum and maximum values for T_A = –40°C to +125°C; typical values at T_A = 25°C

		MIN	TYP	MAX	UNIT
t _{CLK}	Time period of SCLK	16.66			ns
t _{su_CSCK}	Setup time: \overline{CS} falling edge to SCLK falling edge	7			ns
t _{ht_CKCS}	Hold time: SCLK rising edge to \overline{CS} rising edge	8			ns
t _{ph_CK}	SCLK high time	0.45		0.55	t _{SCLK}
t _{pl_CK}	SCLK low time	0.45		0.55	t _{SCLK}
t _{ph_CS}	\overline{CS} high time	15			ns

6.7 Switching Characteristics

all specifications are at AVDD = 2.35 V to 3.6 V, DVDD = 1.65 V to 3.6 V, and C_{LOAD-SDO} = 20 pF (unless otherwise noted); minimum and maximum values for T_A = –40°C to +125°C; typical values at T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{CYCLE} ⁽¹⁾	Cycle time	333			ns
t _{CONV}	Conversion time		15 × t _{SCLK}		ns
t _{den_CSDO}	Delay time: \overline{CS} falling edge to data enable			6.5	ns
t _{d_CKDO}	Delay time: SCLK rising edge to (next) data valid on SDO			10	ns
t _{ht_CKDO}	SCLK rising edge to current data invalid	2.5			ns
t _{dz_CSDO}	Delay time: \overline{CS} rising edge to SDO going to tri-state	5.5			ns

(1) t_{CYCLE} = 1 / f_{SAMPLE}.

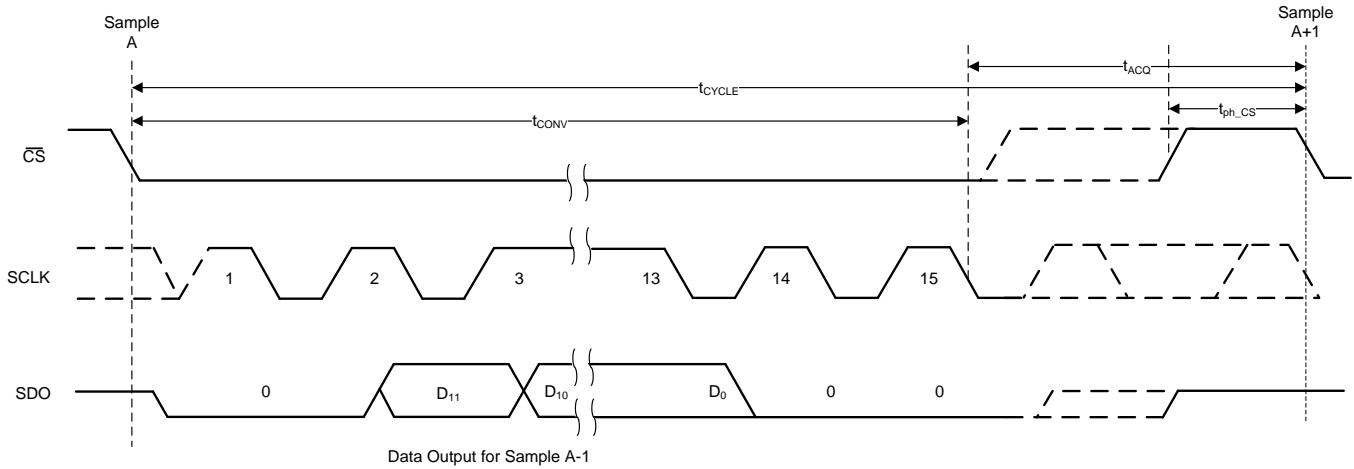


Figure 1. Serial Transfer Frame

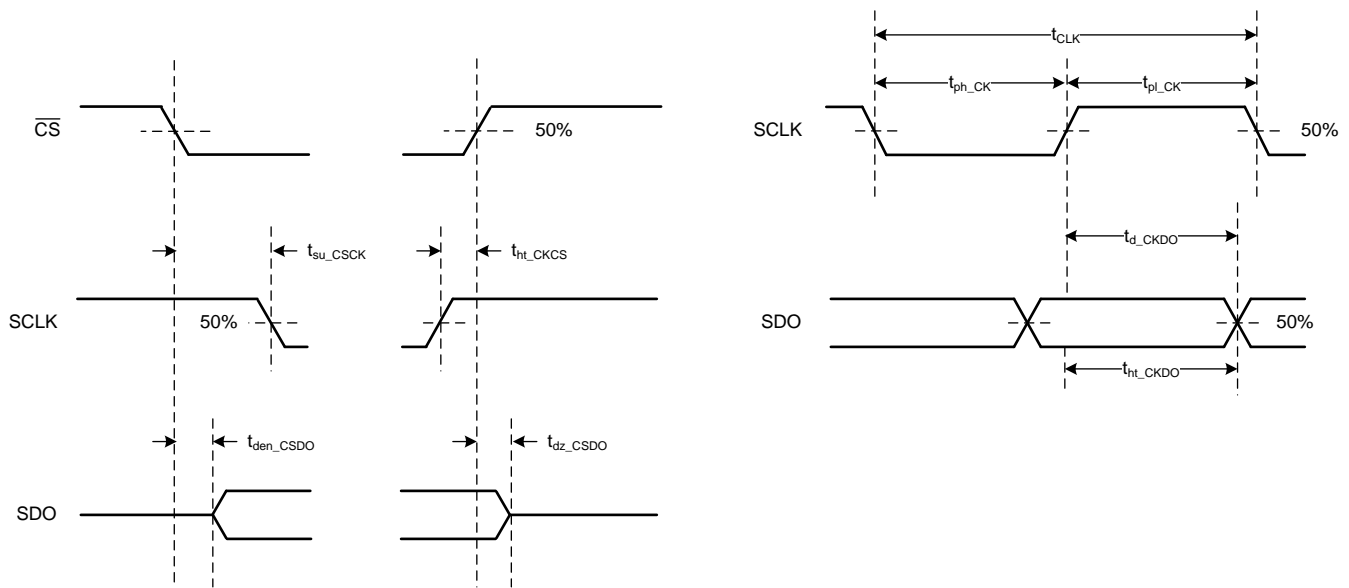
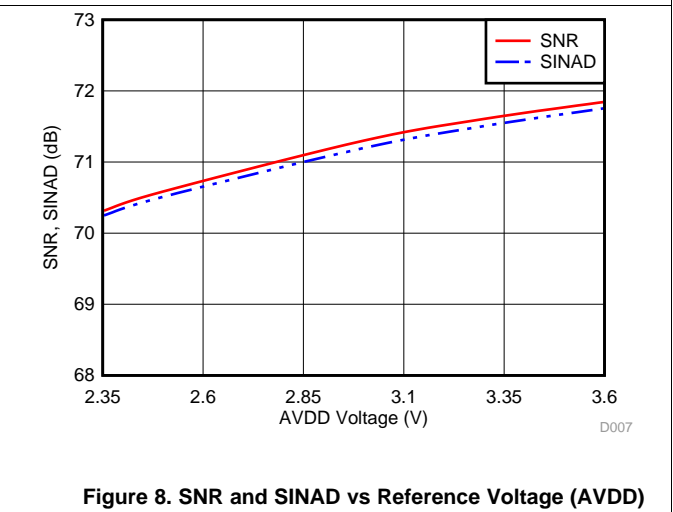
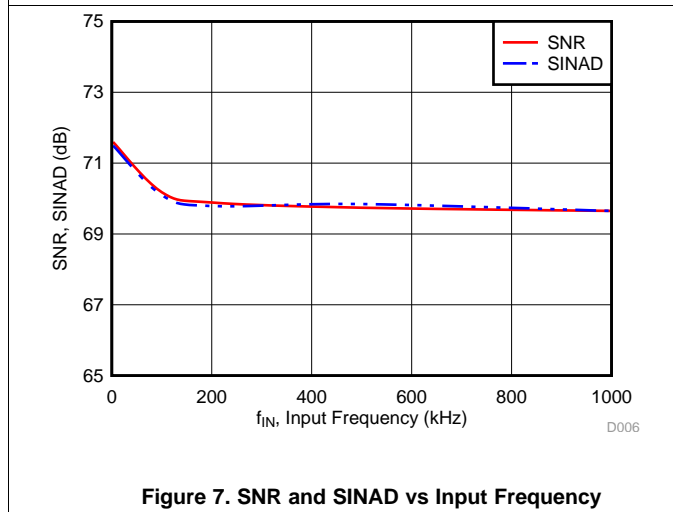
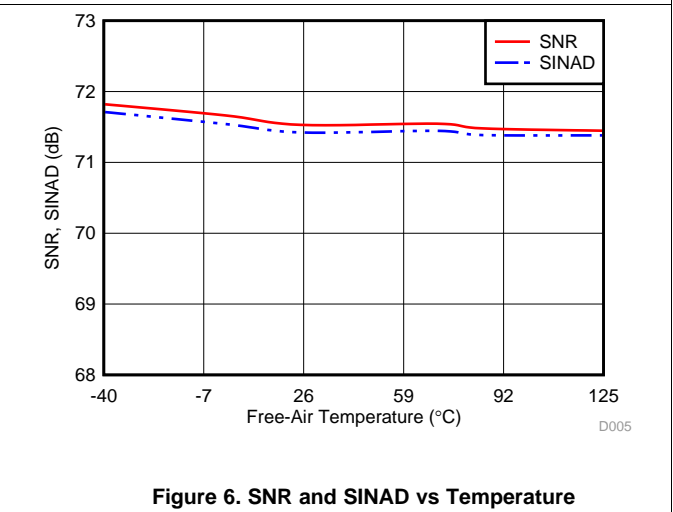
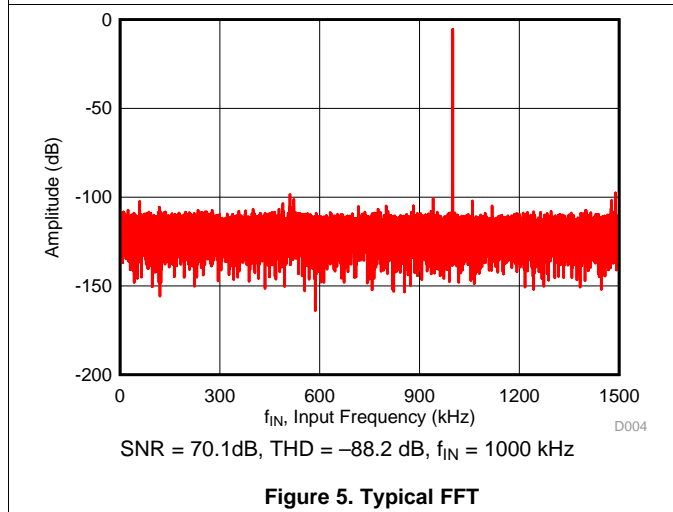
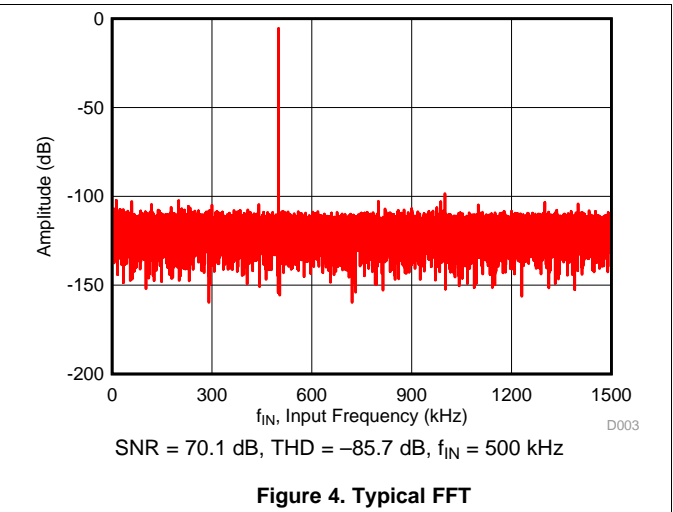
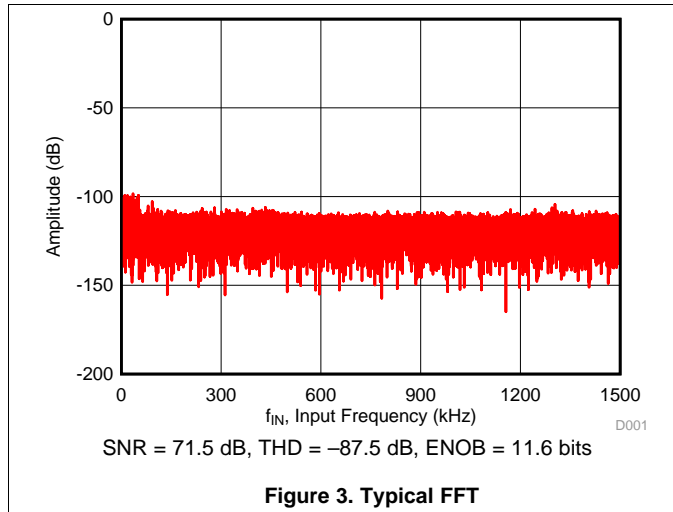


Figure 2. Timing Specifications

6.8 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $AVDD = 3.3\text{ V}$, $DVDD = 1.8\text{ V}$, $f_{IN} = 2\text{ kHz}$, and $f_{\text{sample}} = 3\text{ MSPS}$ (unless otherwise noted)



Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $AVDD = 3.3\text{ V}$, $DVDD = 1.8\text{ V}$, $f_{IN} = 2\text{ kHz}$, and $f_{sample} = 3\text{ MSPS}$ (unless otherwise noted)

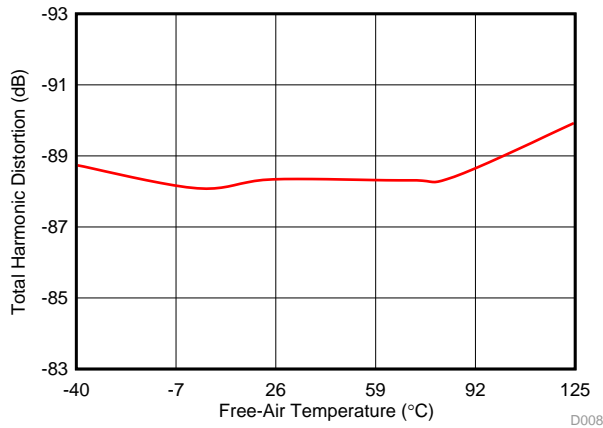


Figure 9. THD vs Temperature

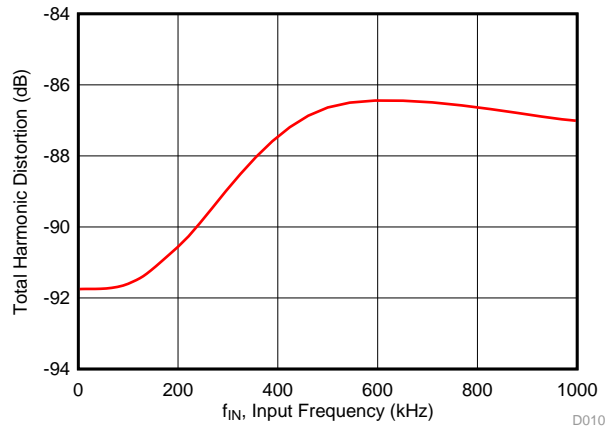


Figure 10. THD vs Input Frequency

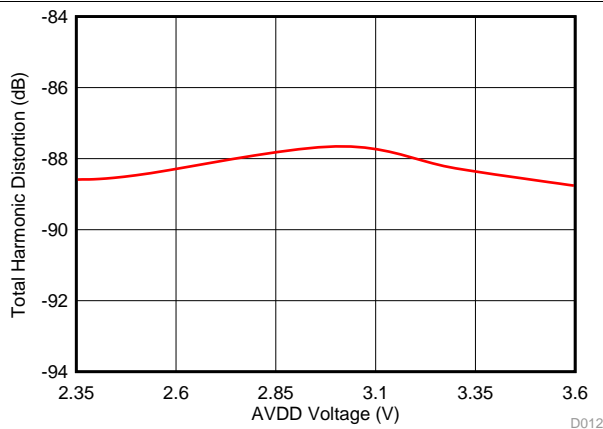


Figure 11. THD vs Reference Voltage (AVDD)

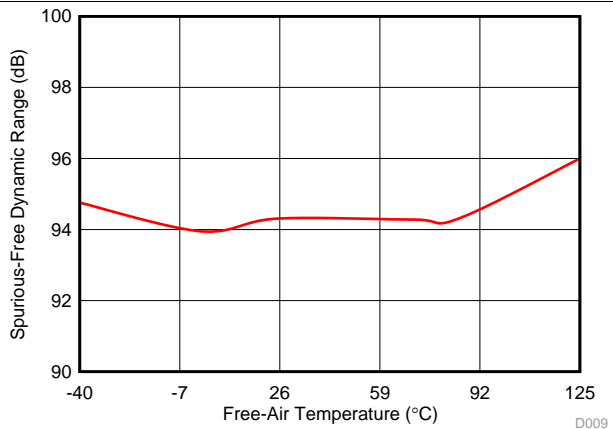


Figure 12. SFDR vs Temperature

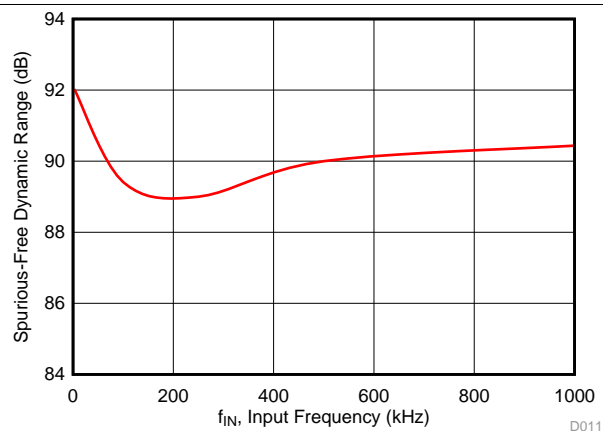


Figure 13. SFDR vs Input Frequency

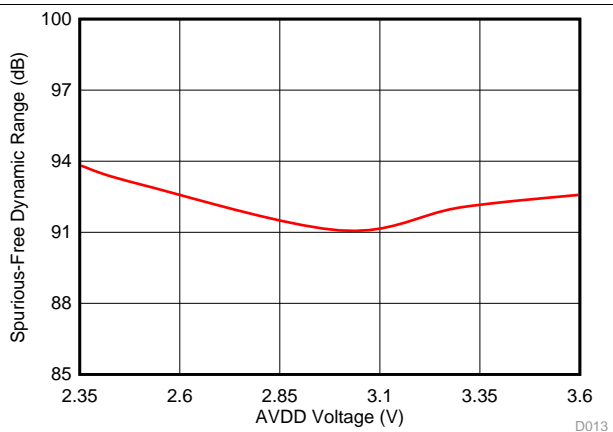


Figure 14. SFDR vs Reference Voltage (AVDD)

Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $AVDD = 3.3\text{ V}$, $DVDD = 1.8\text{ V}$, $f_{IN} = 2\text{ kHz}$, and $f_{sample} = 3\text{ MSPS}$ (unless otherwise noted)

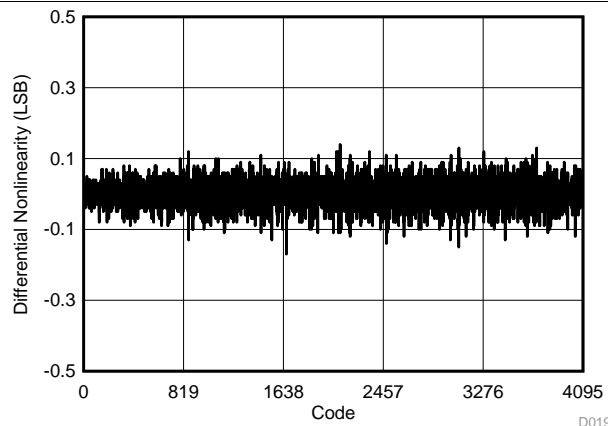


Figure 15. Typical DNL

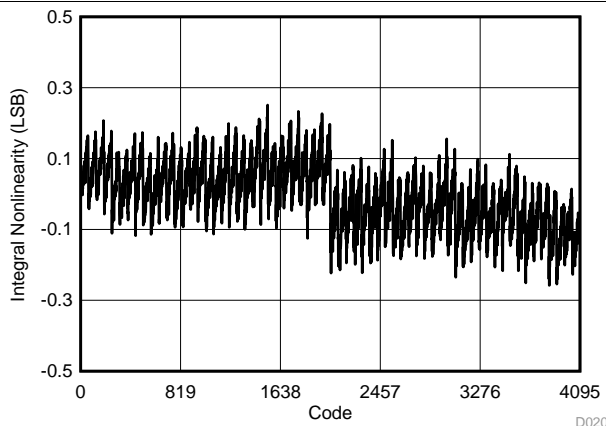


Figure 16. Typical INL

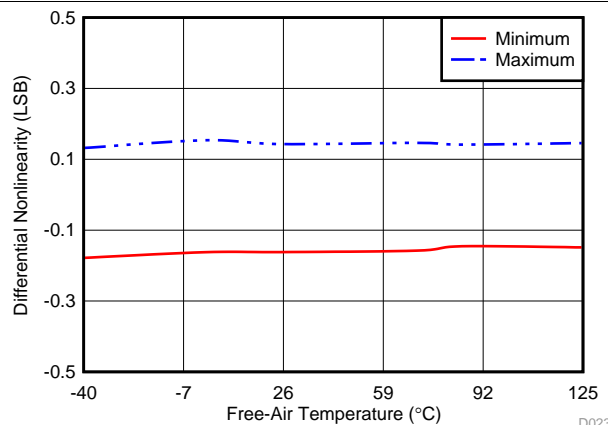


Figure 17. DNL vs Temperature

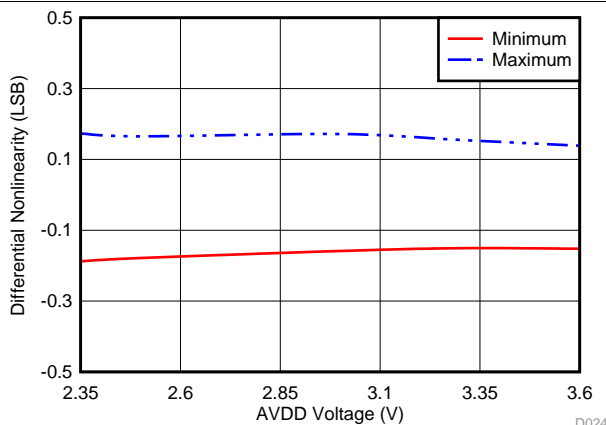


Figure 18. DNL vs Reference Voltage

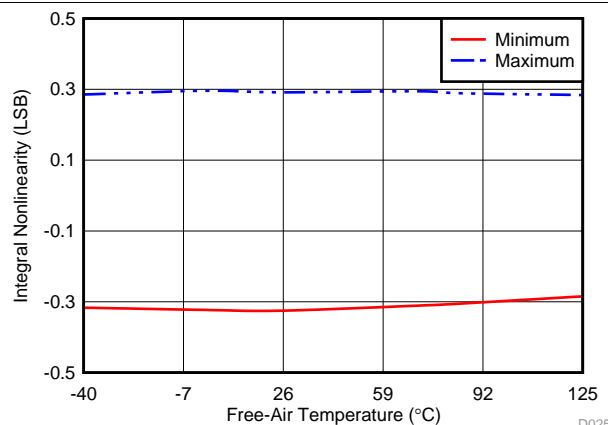


Figure 19. INL vs Temperature

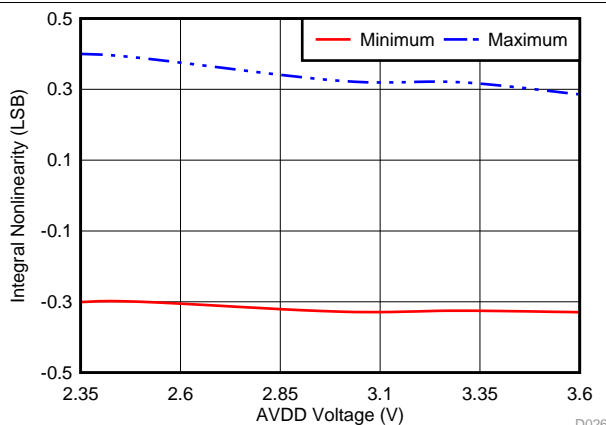
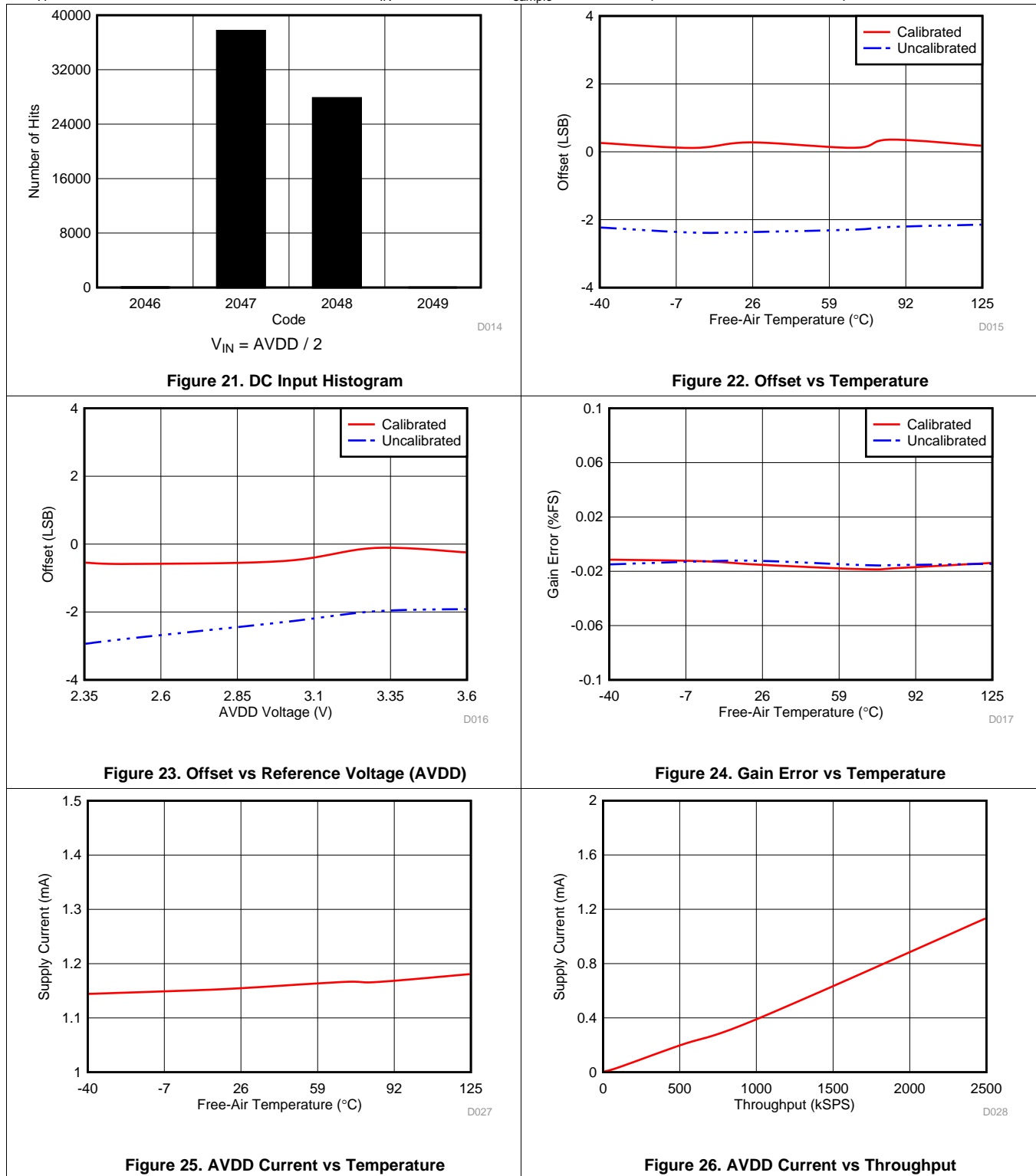


Figure 20. INL vs Reference Voltage

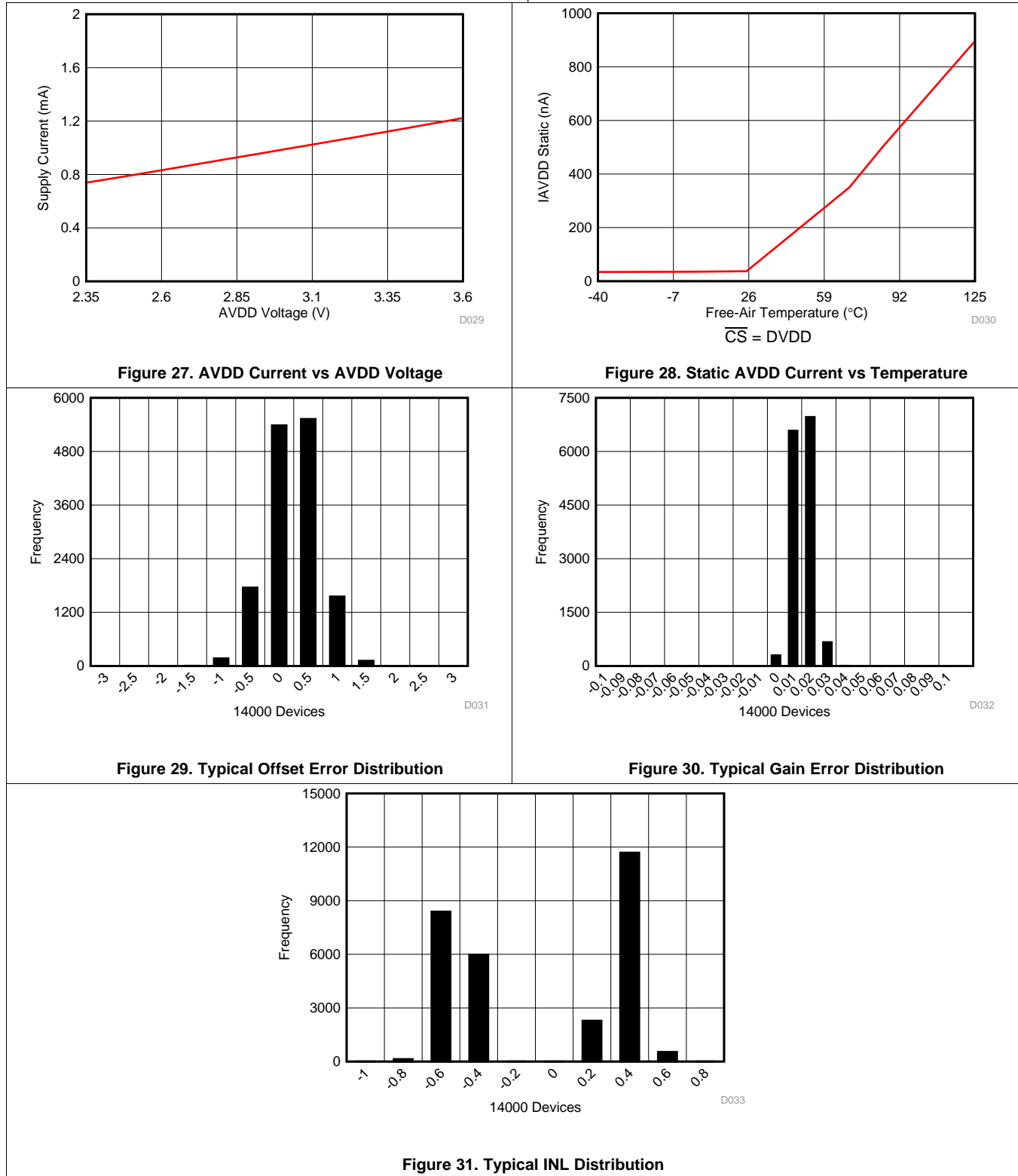
Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $AVDD = 3.3\text{ V}$, $DVDD = 1.8\text{ V}$, $f_{IN} = 2\text{ kHz}$, and $f_{sample} = 3\text{ MSPS}$ (unless otherwise noted)



Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $AVDD = 3.3\text{ V}$, $DVDD = 1.8\text{ V}$, $f_{IN} = 2\text{ kHz}$, and $f_{sample} = 3\text{ MSPS}$ (unless otherwise noted)



7 Parameter Measurement Information

7.1 Digital Voltage Levels

The device complies with the JESD8-7A standard for DVDD from 1.65 V to 1.95 V. Figure 32 shows voltage levels for the digital input and output pins.

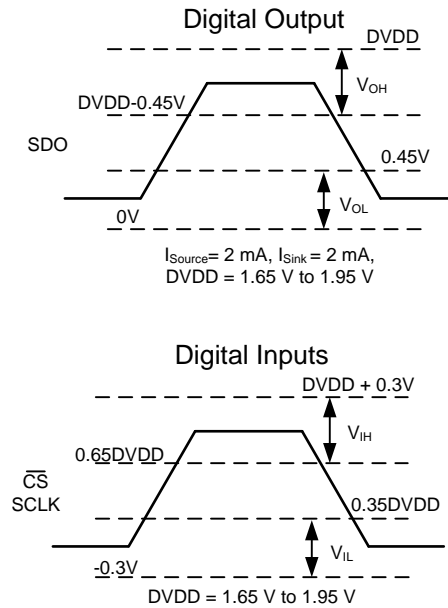


Figure 32. Digital Voltage Levels as per the JESD8-7A Standard

8 Detailed Description

8.1 Overview

The ADS7046 device belongs to a family of pin-to-pin compatible, high-speed, low-power, single-channel successive-approximation register (SAR) type analog-to-digital converters (ADCs). The device family includes multiple resolutions, throughputs, and analog input variants (see [Table 1](#) for a list of devices).

The ADS7046 is a 12-bit, 3-MSPS SAR ADC that supports a single-ended input in the range of 0 V to AVDD, for AVDD in the range of 2.35 V to 3.6 V (see the [Analog Input](#) section for details on the analog input pins).

The internal offset calibration feature (see the [OFFCAL State](#) section) maintains excellent offset specifications over the entire AVDD and temperature operating range.

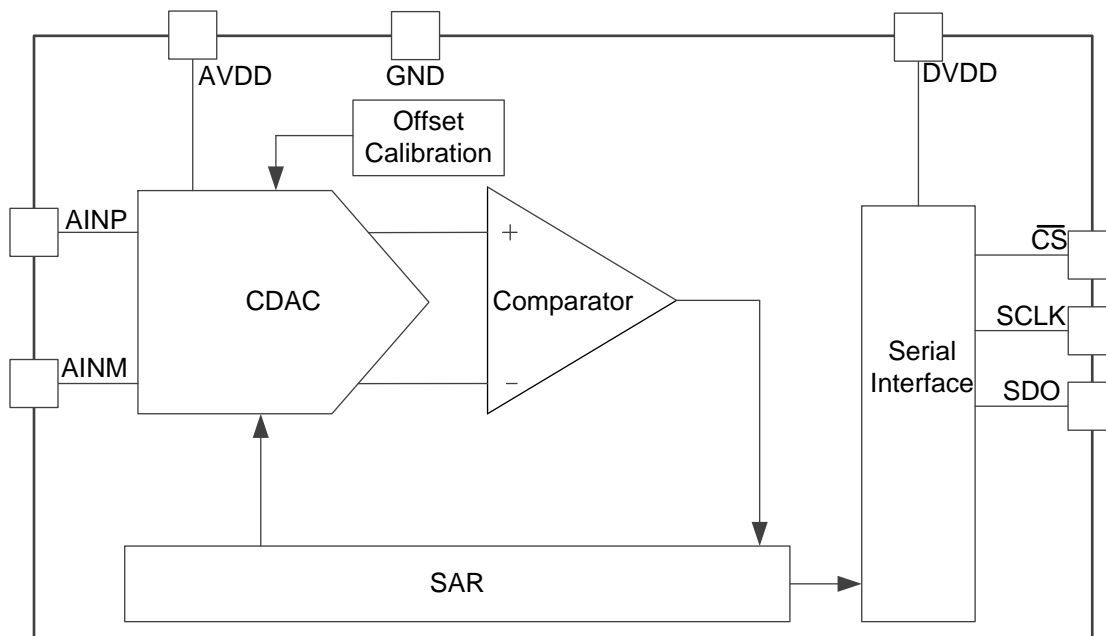
The device supports an SPI-compatible serial interface that is controlled by the \overline{CS} and SCLK signals. The input signal is sampled with the \overline{CS} falling edge and SCLK is used for both, conversion and serial data output (see the [Device Functional Modes](#) section, [Timing Requirements](#) table, and [Switching Characteristics](#) table).

The device supports a wide digital supply range (1.65 V to 3.6 V), enabling direct interfacing to a variety of host controllers. The ADS7046 complies with the JESD8-7A standard (see the [Digital Voltage Levels](#) section) for a normal DVDD range (1.65 V to 1.95 V).

The ADS7046 is available in an 8-pin, small, X2QFN package (see the [Mechanical, Packaging, and Orderable Information](#) section for more details) and is specified over the extended industrial temperature range (–40°C to +125°C).

The small form-factor and extremely-low power consumption make this device suitable for space-constrained and battery-powered applications that require high-speed, high-resolution data acquisition (see the [Application Information](#) section).

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Product Family

The devices listed in [Table 1](#) are all part of the same pin-to-pin compatible, high-speed, low-power, single-channel SAR ADC family. This device family includes multiple different ADC resolutions, throughputs, and analog input types to allow for greater flexibility in the end system. Devices in the same package are pin-compatible to offer a scalable family of devices for varying levels of end-system performance. The ADCs with device numbers ending in -Q1 are also AEC-Q100 qualified for automotive applications.

Table 1. Device Family Comparison

DEVICE NUMBER	RESOLUTION (Bits)	THROUGHPUT (MSPS)	INPUT TYPE	PACKAGES ⁽¹⁾
ADS7040	8	1	Single-ended	X2QFN (8): 1.5 mm × 1.5 mm VSSOP (8): 2.0 mm × 3.1 mm
ADS7041	10	1	Single-ended	X2QFN (8): 1.5 mm × 1.5 mm VSSOP (8): 2.0 mm × 3.1 mm
ADS7042	12	1	Single-ended	X2QFN (8): 1.5 mm × 1.5 mm VSSOP (8): 2.0 mm × 3.1 mm
ADS7043	12	1	Pseudo-differential	X2QFN (8): 1.5 mm × 1.5 mm VSSOP (8): 2.0 mm × 3.1 mm
ADS7044	12	1	Fully-differential	X2QFN (8): 1.5 mm × 1.5 mm VSSOP (8): 2.0 mm × 3.1 mm
ADS7029-Q1	8	2	Single-ended	VSSOP (8): 2.0 mm × 3.1 mm
ADS7039-Q1	10	2	Single-ended	VSSOP (8): 2.0 mm × 3.1 mm
ADS7049-Q1	12	2	Single-ended	VSSOP (8): 2.0 mm × 3.1 mm
ADS7046	12	3	Single-ended	X2QFN (8): 1.5 mm × 1.5 mm
ADS7047	12	3	Fully-differential	X2QFN (8): 1.5 mm × 1.5 mm
ADS7052	14	1	Single-ended	X2QFN (8): 1.5 mm × 1.5 mm
ADS7054	14	1	Fully-differential	X2QFN (8): 1.5 mm × 1.5 mm
ADS7056	14	2.5	Single-ended	X2QFN (8): 1.5 mm × 1.5 mm
ADS7057	14	2.5	Fully-differential	X2QFN (8): 1.5 mm × 1.5 mm

(1) Devices listed in the same package are pin-compatible.

8.3.2 Analog Input

The device supports a unipolar, single-ended analog input signal. Figure 33 shows a small-signal equivalent circuit of the sample-and-hold circuit. The sampling is represented by a resistance (R_{S1} and R_{S2} , typically $50\ \Omega$) in series with an ideal switch (SW_1 and SW_2). The sampling capacitors, C_{S1} and C_{S2} , are typically $16\ \text{pF}$.

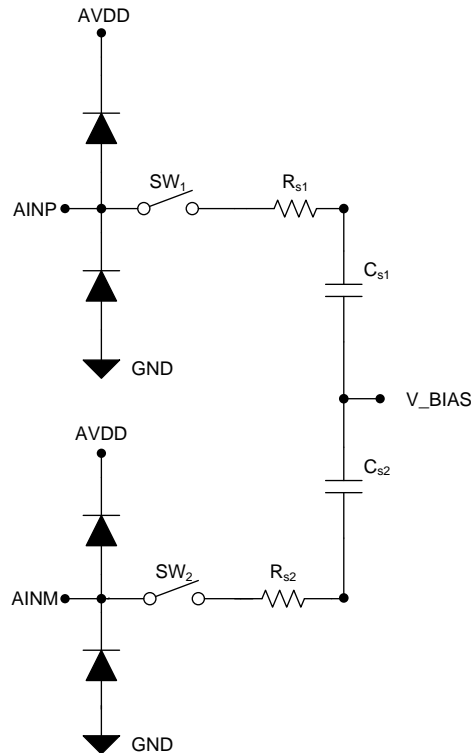


Figure 33. Equivalent Input Circuit for the Sampling Stage

During the acquisition process, both positive and negative inputs are individually sampled on C_{S1} and C_{S2} , respectively. During the conversion process, the device converts for the voltage difference between the two sampled values: $V_{AINP} - V_{AINM}$.

Each analog input pin has electrostatic discharge (ESD) protection diodes to AVDD and GND. Keep the analog inputs within the specified range to avoid turning the diodes on.

The full-scale analog input range (FSR) is 0 V to AVDD.

8.3.3 Reference

The device uses the analog supply voltage (AVDD) as the reference voltage for the analog to digital conversion. During the conversion process, the internal capacitors are switched to the AVDD pin as per the successive approximation algorithm. A voltage reference must be selected with low temperature drift, high output current drive and low output impedance. TI recommends a 3.3- μF (C_{AVDD}), low equivalent series resistance (ESR) ceramic capacitor between the AVDD and GND pins. This decoupling capacitor provides the instantaneous charge required by the internal circuit during the conversion process and maintains a stable dc voltage on the AVDD pin.

See the [Power Supply Recommendations](#) and [Layout Example](#) sections for component recommendations and layout guidelines.

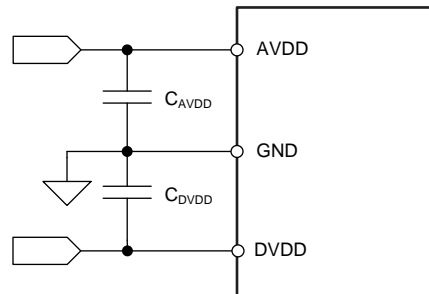


Figure 34. Reference for the Device

8.3.4 ADC Transfer Function

The device supports a unipolar, single-ended analog input signal. The output is in straight binary format. Figure 35 and Table 2 show the ideal transfer characteristics for the device.

The least significant bit for the device is given by:

$$1 \text{ LSB} = V_{\text{REF}} / 2^N$$

where:

- V_{REF} = Voltage applied between the AVDD and GND pins
 - $N = 12$
- (1)

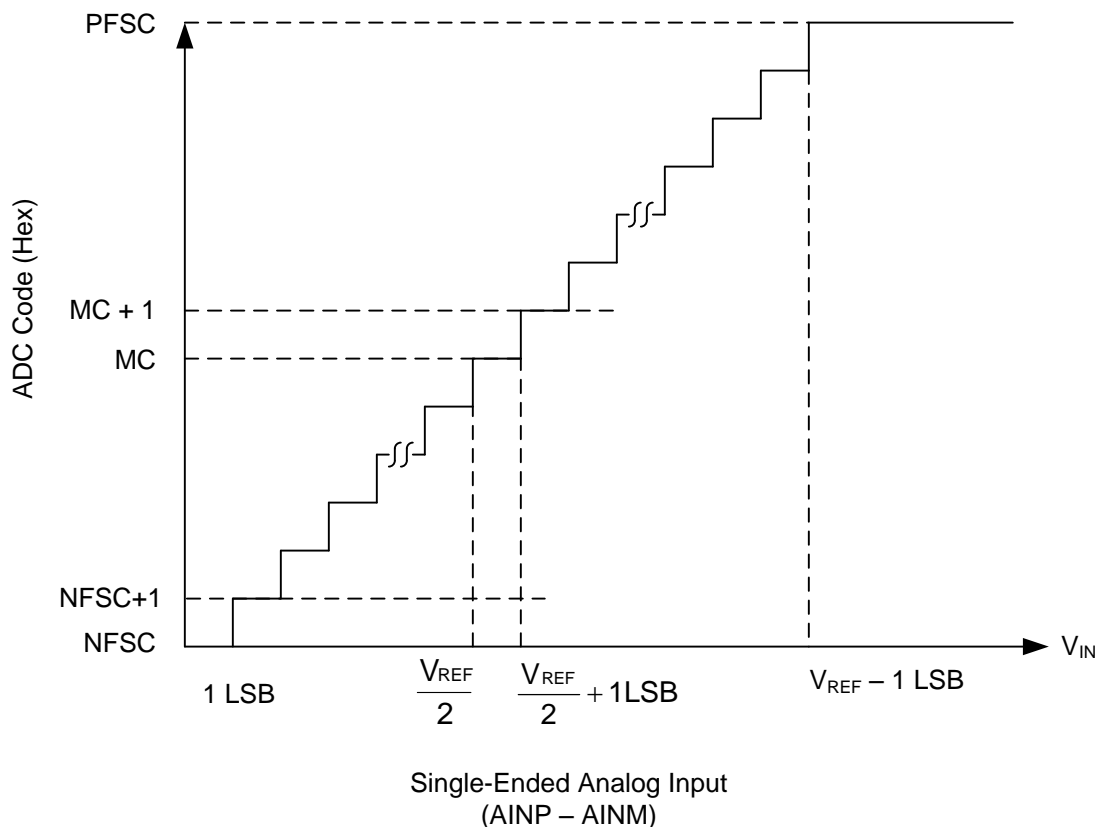


Figure 35. Ideal Transfer Characteristics

Table 2. Transfer Characteristics

INPUT VOLTAGE (AINP – AINM)	CODE	DESCRIPTION	IDEAL OUTPUT CODE (Hex)
$\leq 1 \text{ LSB}$	NFSC	Negative full-scale code	000
1 LSB to 2 LSB	NFSC + 1	—	001
$V_{\text{REF}} / 2$ to $V_{\text{REF}} / 2 + 1 \text{ LSB}$	MC	Mid code	7FF
$V_{\text{REF}} / 2 + 1 \text{ LSB}$ to $V_{\text{REF}} / 2 + 2 \text{ LSB}$	MC + 1	—	800
$\geq V_{\text{REF}} - 1 \text{ LSB}$	PFSC	Positive full-scale code	FFF

8.4 Device Functional Modes

The device supports a simple, SPI-compatible interface to the external host. On power-up, the device is in the ACQ state. The \overline{CS} signal defines one conversion and serial data transfer frame. A frame starts with a \overline{CS} falling edge and ends with a \overline{CS} rising edge. The SDO pin is tri-stated when \overline{CS} is high. With \overline{CS} low, the clock provided on the SCLK pin is used for conversion and data transfer. Output data are available on the SDO pin.

As shown in Figure 36, the device supports three functional states: acquisition (ACQ), conversion (CNV), and offset calibration (OFFCAL). The device status depends on the \overline{CS} and SCLK signals provided by the host controller.

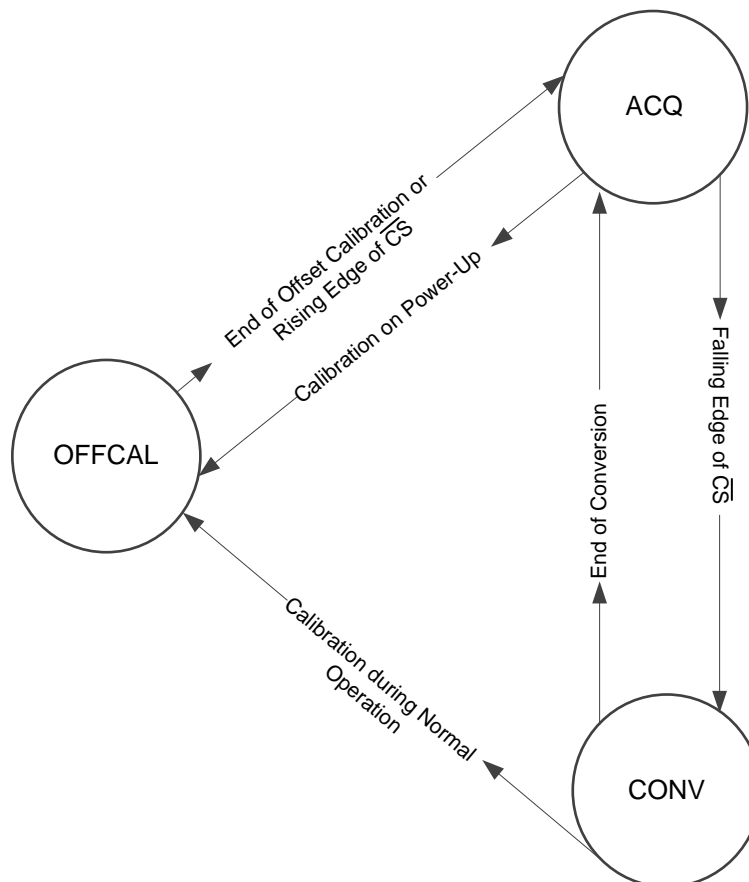


Figure 36. Functional State Diagram

8.4.1 ACQ State

In the ACQ state, switches SW_1 and SW_2 connected to the analog input pins close and the device acquires the analog input signal on C_{S1} and C_{S2} . The device enters ACQ state at power-up, at the end of every conversion, and after completing the offset calibration. A \overline{CS} falling edge takes the device from the ACQ state to the CNV state.

The device consumes extremely low power from the AVDD and DVDD power supplies when in ACQ state.

Device Functional Modes (continued)

8.4.2 CNV State

In the CNV state, the device uses the external clock to convert the sampled analog input signal to an equivalent digital code as per the transfer function illustrated in Figure 35. The conversion process requires a minimum of 15 SCLK falling edges to be provided within the frame. After the end of conversion process, the device automatically moves from the CNV state to the ACQ state. For acquisition of the next sample, a minimum time of t_{ACQ} must be provided.

Figure 37 shows a detailed timing diagram for the serial interface. In the first serial transfer frame after power-up, the device provides the first data as all zeros. In any frame, the clocks provided on the SCLK pin are also used to transfer the output data for the previous conversion. A leading 0 is output on the SDO pin on the \overline{CS} falling edge. The most significant bit (MSB) of the output data is launched on the SDO pin on the rising edge after the first SCLK falling edge. Subsequent output bits are launched on the subsequent rising edges provided on SCLK. When all 12 output bits are shifted out, the device outputs 0's on the subsequent SCLK rising edges. The device enters the ACQ state after 15 clocks and a minimum time of t_{ACQ} must be provided for acquiring the next sample. If the device is provided with less than 15 SCLK falling edges in the present serial transfer frame, the device provides an invalid conversion result in the next serial transfer frame.

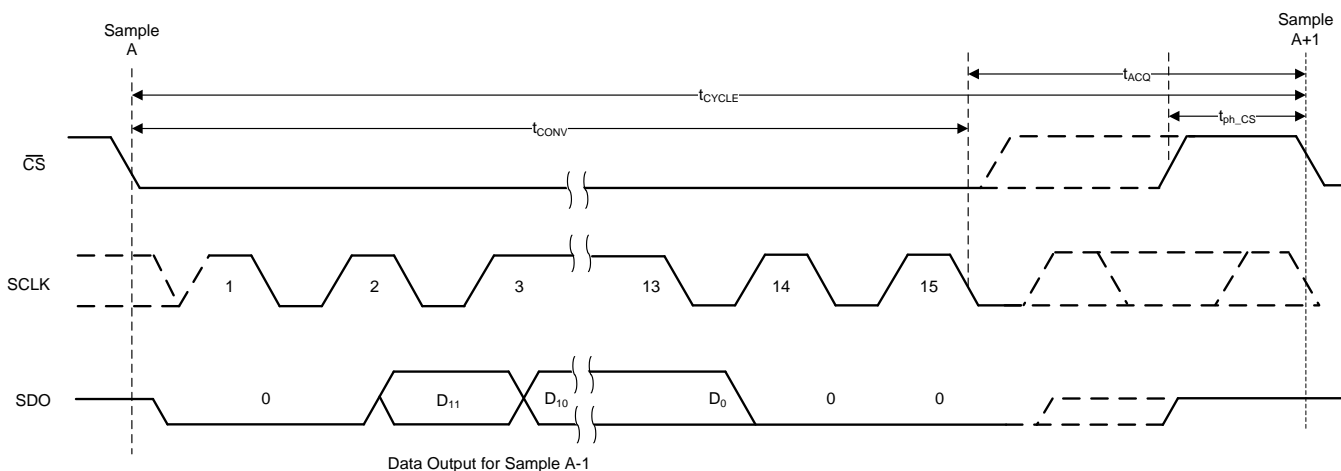


Figure 37. Serial Interface Timing Diagram

Device Functional Modes (continued)

8.4.3 OFFCAL State

In the offset calibration (OFFCAL) state, the sampling capacitors are disconnected from the analog input pins (AINP and AINM) and the device calibrates and corrects for any internal offset errors. The offset calibration is effective for all subsequent conversions until the device is powered off. An offset calibration cycle is recommended at power-up and whenever there is a significant change in the operating conditions for the device (such as in the AVDD voltage and operating temperature).

The host controller must provide a serial transfer frame as described in [Figure 38](#) or in [Figure 39](#) to enter the OFFCAL state.

8.4.3.1 Offset Calibration on Power-Up

On power-up, the host must provide 24 SCLKs in the first serial transfer to enter the OFFCAL state. The device provides 0's on SDO during offset calibration. For acquisition of the next sample, a minimum time of t_{ACQ} must be provided.

If the host controller starts the offset calibration process but then pulls the \overline{CS} pin high before providing 24 SCLKs, then the offset calibration process is aborted and the device enters the ACQ state. [Figure 38](#) and [Table 3](#) provide the timing for offset calibration on power-up.

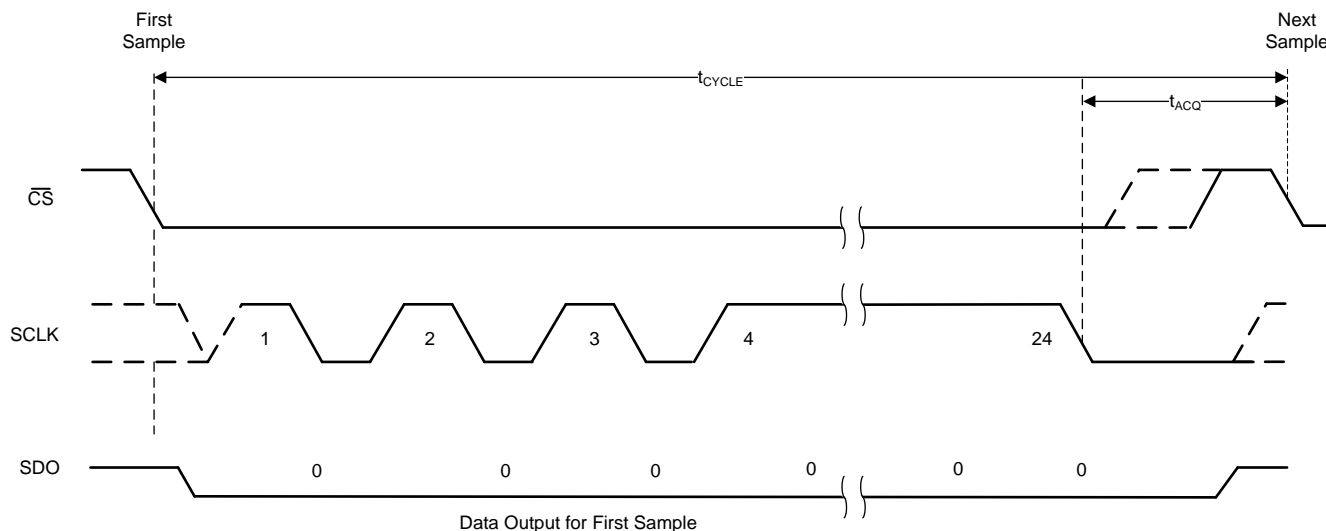


Figure 38. Timing for Offset Calibration on Power-Up

Table 3. Timing Specifications for Offset Calibration on Power-Up⁽¹⁾

		MIN	TYP	MAX	UNIT
t_{cycle}	Cycle time for offset calibration on power-up	$24 \times t_{CLK} + t_{ACQ}$			ns
t_{ACQ}	Acquisition time	80			ns
f_{SCLK}	Frequency of SCLK	60			MHz

(1) In addition to the timing specifications of [Figure 38](#) and [Table 3](#), the timing specifications described in [Figure 2](#) and the [Timing Requirements](#) table are also applicable for offset calibration on power-up.

8.4.3.2 Offset Calibration During Normal Operation

During normal operation, the host must provide 64 SCLKs in the serial transfer frame to enter the OFFCAL state. The device provides the conversion result for the previous sample during the first 15 SCLKs and 0's on SDO for the rest of the SCLKs in the serial transfer frame. For acquisition of the next sample, a minimum time of t_{ACQ} must be provided.

If the host controller provides more than 15 SCLKs but pulls the \overline{CS} high before providing 64 SCLKs, then the offset calibration process is aborted and the device enters the ACQ state. Figure 39 and Table 4 provide the timing for offset calibration during normal operation.

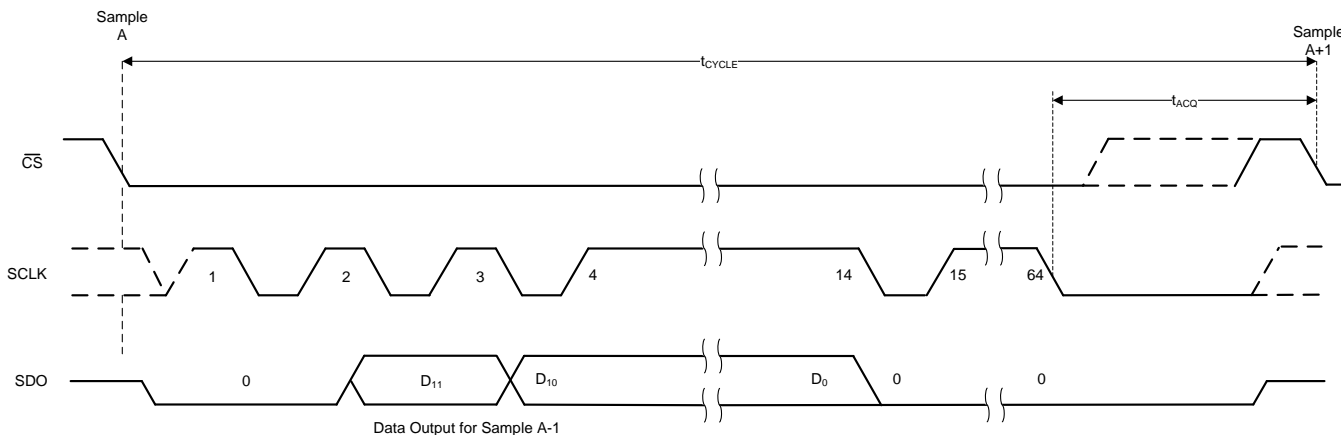


Figure 39. Timing for Offset Calibration During Normal Operation

Table 4. Timing Specifications for Offset Calibration During Normal Operation⁽¹⁾

		MIN	TYP	MAX	UNIT
t_{cycle}	Cycle time for offset calibration on power-up	$64 \times t_{CLK} + t_{ACQ}$			ns
t_{ACQ}	Acquisition time	80			ns
f_{SCLK}	Frequency of SCLK	60			MHz

(1) In addition to the timing specifications of Figure 39 and Table 4, the timing specifications described in Figure 2 and the [Timing Requirements](#) table are also applicable for offset calibration during normal operation.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The two primary supporting circuits required to maximize the performance of a high-precision, successive approximation register (SAR) analog-to-digital converter (ADC) are the input driver and the reference driver circuits. This section details some general principles for designing the input driver circuit, reference driver circuit, and provides typical application circuits designed for the device.

9.2 Typical Applications

9.2.1 Single-Supply Data Acquisition With the ADS7046

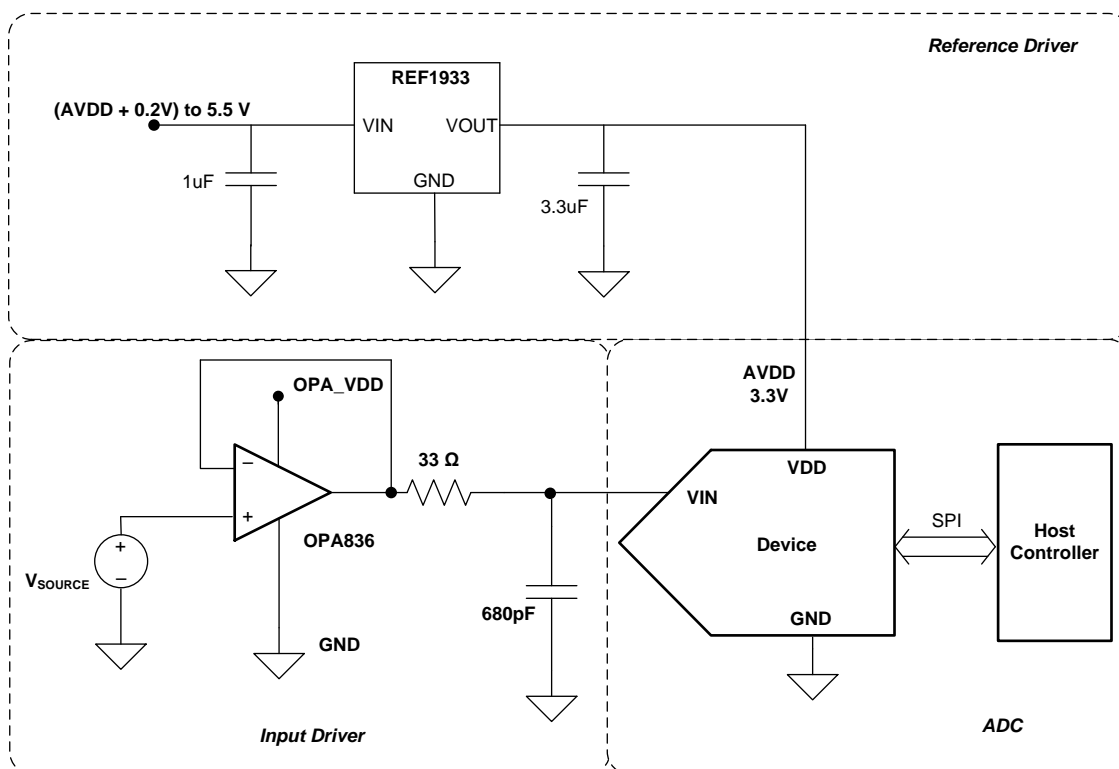


Figure 40. DAQ Circuit: Single-Supply DAQ

9.2.1.1 Design Requirements

The goal of the circuit shown in [Figure 40](#) is to design a single-supply data acquisition (DAQ) circuit based on the ADS7046 with SNR greater than 70 dB and THD less than -85 dB for input frequencies of 2 kHz to 200 kHz at a throughput of 3 MSPS for applications such as sonar receivers and ultrasonic flow meters.

Typical Applications (continued)

9.2.1.2 Detailed Design Procedure

The input driver circuit for a high-precision ADC mainly consists of two parts: a driving amplifier and charge kickback filter. Careful design of the front-end circuit is critical to meet the linearity and noise performance of a high-precision ADC.

9.2.1.2.1 Low Distortion Charge Kickback Filter Design

Figure 41 shows the input circuit of a typical SAR ADC. During the acquisition phase, the SW switch closes and connects the sampling capacitor (C_{SH}) to the input driver circuit. This action introduces a transient on the input pins of the SAR ADC. An ideal amplifier with $0\ \Omega$ of output impedance and infinite current drive can settle this transient in zero time. For a real amplifier with non-zero output impedance and finite drive strength, this switched capacitor load can create stability issues.

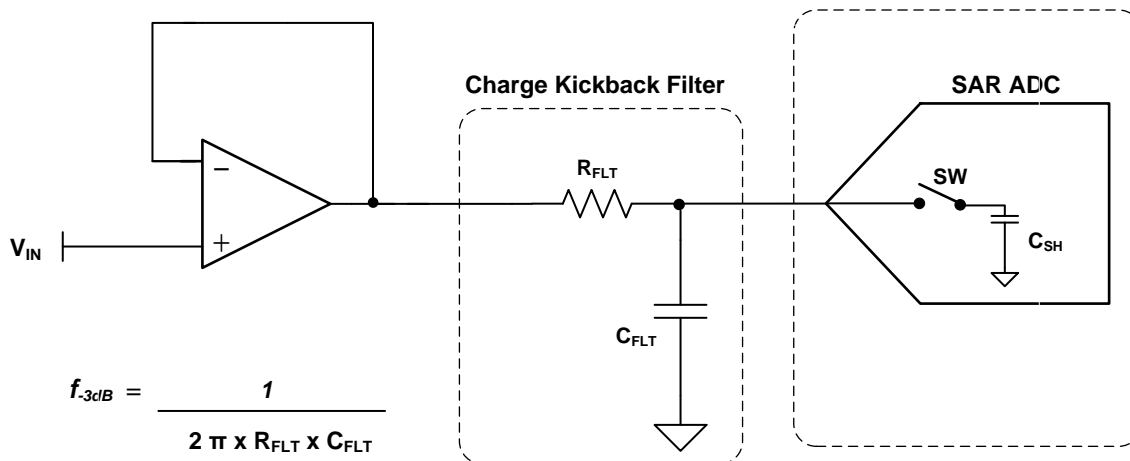


Figure 41. Input Sample-and-Hold Circuit for a Typical SAR ADC

For ac signals, the filter bandwidth must be kept low to band-limit the noise fed into the ADC input, thereby increasing the signal-to-noise ratio (SNR) of the system. Besides filtering the noise from the front-end drive circuitry, the RC filter also helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC. A filter capacitor, C_{FLT} , is connected across the ADC inputs. This capacitor helps reduce the sampling charge injection and provides a charge bucket to quickly charge the internal sample-and-hold capacitors during the acquisition process. As a rule of thumb, the value of this capacitor is at least 20 times the specified value of the ADC sampling capacitance. For this device, the input sampling capacitance is equal to 16 pF. Thus, the value of C_{FLT} is greater than 320 pF. Select a COG- or NPO-type capacitor because these capacitor types have a high-Q, low-temperature coefficient, and stable electrical characteristics under varying voltages, frequency, and time.

Driving capacitive loads can degrade the phase margin of the input amplifiers, thus making the amplifier marginally unstable. To avoid amplifier stability issues, series isolation resistors (R_{FLT}) are used at the output of the amplifiers. A higher value of R_{FLT} is helpful from the amplifier stability perspective, but adds distortion as a result of interactions with the nonlinear input impedance of the ADC. Distortion increases with source impedance, input signal frequency, and input signal amplitude. Therefore, the selection of R_{FLT} requires balancing the stability and distortion of the design.

Typical Applications (continued)

9.2.1.2.2 Input Amplifier Selection

The input amplifier bandwidth is typically much higher than the cutoff frequency of the charge kickback filter. Thus, TI strongly recommends performing a SPICE simulation to confirm that the amplifier has more than 40° phase margin with the selected filter. Simulation is critical because even with high-bandwidth amplifiers, some amplifiers can require more bandwidth than others to drive similar filters. To learn more about the SAR ADC input driver design, see the [TI Precision Labs training video series](#).

For the application circuit of [Figure 40](#), the [OPA836](#) is selected for its high bandwidth (205 MHz), low noise (4.6 nV/√Hz), high output drive capacity (45 mA), and fast settling response (22 ns for 0.1% settling).

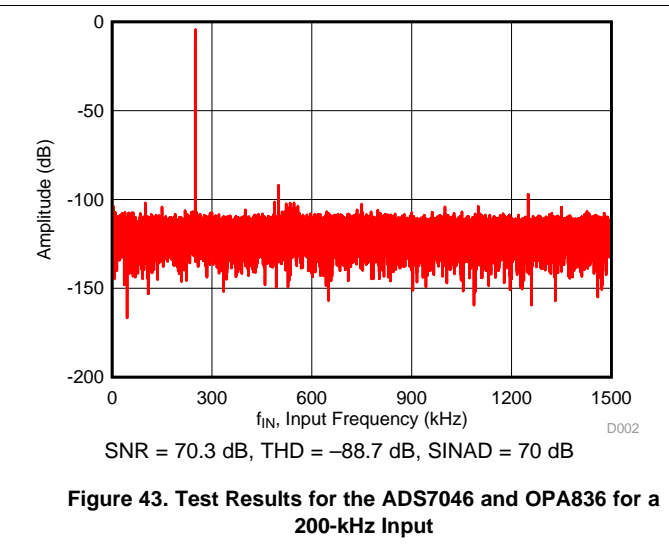
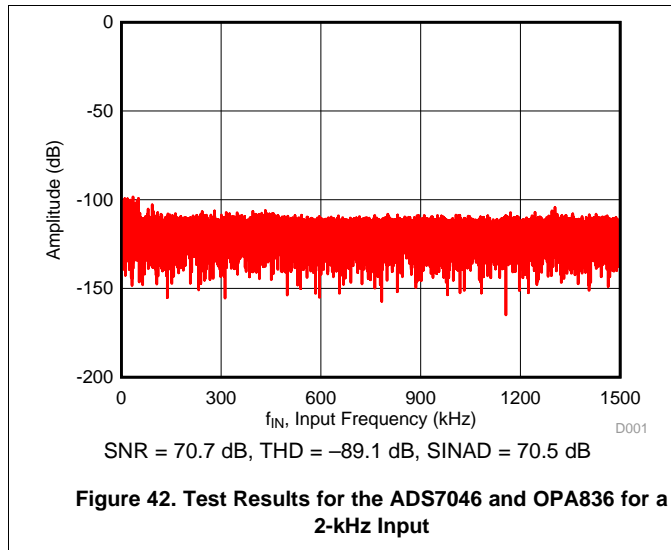
9.2.1.2.3 Reference Circuit

The ADS70xx uses the analog supply voltage (AVDD) as the reference voltage for the analog to digital conversion. During the conversion process, the internal capacitors are switched to the level of the AVDD pin as per the successive approximation algorithm. A voltage reference must be selected with low temperature drift, high output current drive and low output impedance. For this application, the [REF1933](#) was selected as the voltage reference and analog power supply for the ADC. The [REF1933](#) has excellent temperature drift performance (25 ppm/°C), good initial accuracy (0.1%), high output drive capability (25 mA), and low quiescent current (360 μA). The [REF1933](#) also provides a bias voltage output of half the reference voltage (VREF/2) which can be used as the common mode input for the amplifier.

TI recommends a 3.3-μF (C_{AVDD}), low equivalent series resistance (ESR) ceramic capacitor between the AVDD and GND pins. This decoupling capacitor provides the instantaneous charge required by the internal circuit during the conversion process and maintains a stable dc voltage on the AVDD pin.

9.2.1.3 Application Curves

[Figure 42](#) and [Figure 43](#) provide the measurement results for the circuit described in [Figure 40](#).



Typical Applications (continued)

9.2.2 High Bandwidth (1 MHz) Data Acquisition With the ADS7046

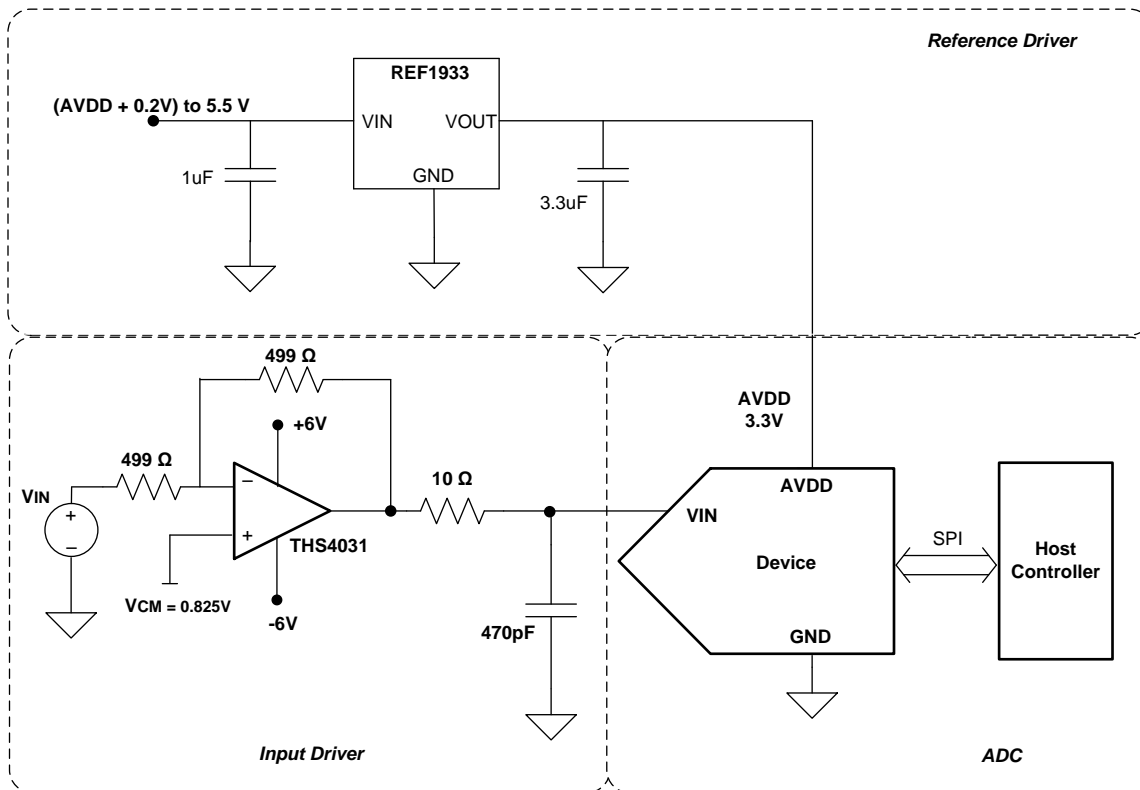


Figure 44. High Bandwidth DAQ Circuit

9.2.2.1 Design Requirements

Applications such as sonar, ultrasonic flow meters, global positioning systems (GPS), handheld radios, and motor controls need analog-to-digital converters that are interfaced to high-frequency sensors (100 kHz to 1 MHz). The goal of the circuit described in Figure 44 is to design a circuit based on the ADS7046 with SNR greater than 70 dB and THD less than -80 dB for input frequencies of 200 kHz to 1 MHz at a throughput of 3 MSPS.

9.2.2.2 Detailed Design Procedure

To achieve a SINAD greater than 69 dB, the operational amplifier must have high bandwidth in order to settle the input signal within the acquisition time of the ADC. The operational amplifier must have low noise to keep the total system noise below 20% of the input-referred noise of the ADC. For the application circuit shown in Figure 44, the THS4031 is selected for its high bandwidth (275 MHz), low total harmonic distortion of -90 dB at 1 MHz, and ultra-low noise of $1.6 \text{ nV}/\sqrt{\text{Hz}}$. The THS4031 is powered up from dual power supply ($V_{DD} = 6 \text{ V}$ and $V_{SS} = -6 \text{ V}$).

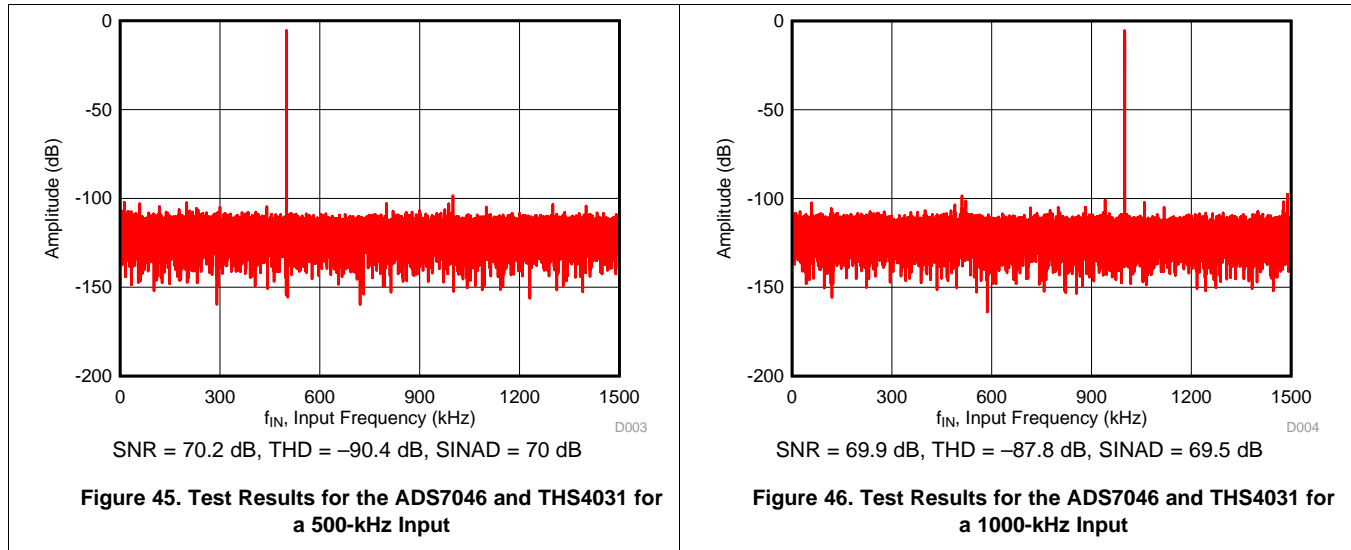
For this application, the REF1933 was selected as the voltage reference and analog power supply for the ADC. The REF1933 has excellent temperature drift performance ($25 \text{ ppm}/^\circ\text{C}$), good initial accuracy (0.1%), high output drive capability (25 mA), and low quiescent current (360 μA). The REF1933 also provides a bias voltage output of half the reference voltage ($V_{REF} / 2$) that can be used as the common-mode input for the amplifier.

The SNR performance at higher input frequency is highly dependant on jitter on the sampling signal (\overline{CS}). TI recommends selecting a clock source that has very low jitter ($< 20\text{-ps RMS}$).

Typical Applications (continued)

9.2.2.3 Application Curves

Figure 45 shows the FFT plot for the ADS7046 with a 500-kHz input frequency used for the circuit in Figure 44. Figure 46 shows the FFT plot for the ADS7046 with a 1000-kHz input frequency used for the circuit in Figure 44.



Typical Applications (continued)

9.2.3 12-Bit, 10-kSPS DAQ Circuit Optimized for DC Sensor Measurements

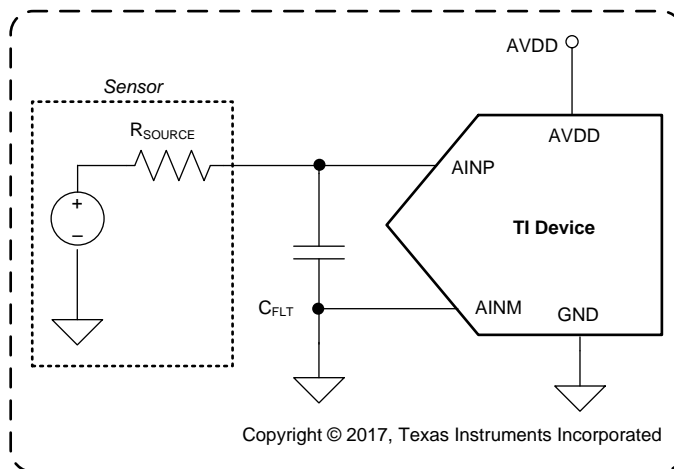


Figure 47. Interfacing the Device Directly With Sensors

In applications where the input is very slow moving and the overall system ENOB is not a critical parameter, a DAQ circuit can be designed without the input driver for the ADC. This type of a use case is of particular interest for applications in which the primary goal is to achieve the absolute lowest power possible. Typical applications that fall into this category are low-power sensor applications (such as temperature, pressure, humidity, gas, and chemical).

9.2.3.1 Design Requirements

For this design example, use the parameters listed in Table 5 as the input parameters.

Table 5. Design Parameters

DESIGN PARAMETER	GOAL VALUE
Throughput	10 kSPS
SNR at 100 Hz	70 dB
THD at 100 Hz	-75 dB
SINAD at 100 Hz	69 dB
ENOB	11 bits
Power	20 μ W

9.2.3.2 Detailed Design Procedure

The ADS7046 can be directly interfaced with sensors at lower throughput without the need of an amplifier buffer, however, the output impedance of the sensor must be taken into account. The sensor must be capable of driving the switched capacitor load of a SAR ADC and settling the analog input signal within the acquisition time of the SAR ADC. Figure 47 shows the simplified circuit for a sensor as a voltage source with output impedance (R_{source}). As the output impedance of the sensor increases, the device requires more acquisition time to settle the input signal to the desired accuracy.

The acquisition time of a SAR ADC (such as the ADS7046) can be increased by reducing throughput in the following ways:

1. Reducing the SCLK frequency to reduce the throughput or
2. Keeping the SCLK fixed at the highest permissible value (that is, 60 MHz for the device) and increasing the CS high time

Table 6 lists the acquisition time for the above two cases for a throughput of 10 kSPS. Clearly, case 2 provides more acquisition time for the input signal to settle.

Table 6. Acquisition Time With Different SCLK Frequencies

CASE	SCLK	t_{cycle}	CONVERSION TIME (= $18 \times t_{\text{SCLK}}$)	ACQUISITION TIME (= $t_{\text{cycle}} - t_{\text{conv}}$)
1	0.24 MHz	100 μs	75 μs	25 μs
2	60 MHz	100 μs	0.3 μs	99.7 μs

9.2.3.3 Application Curve

Figure 48 provides the results for ENOB achieved from the ADS7046 for case 2 at different throughputs with different values of sensor output impedance.

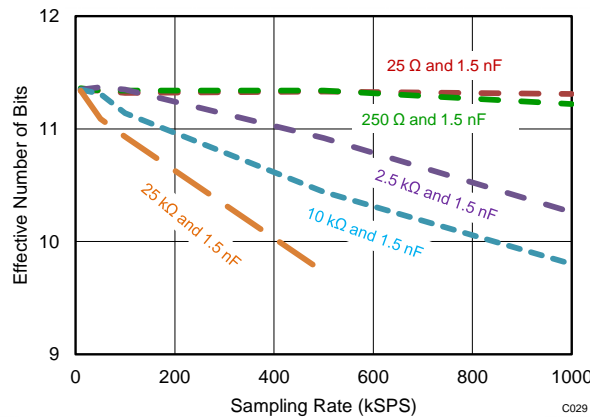


Figure 48. Effective Number of Bits (ENOB) Achieved From the ADS7046 at Different Throughputs

Table 7 shows the results and performance summary for this 12-bit, 10-kSPS DAQ circuit application with a sensor output impedance of 22 k Ω .

Table 7. Results and Performance Summary for a 12-Bit, 10-kSPS DAQ Circuit for DC Sensor Measurements

DESIGN PARAMETER	GOAL VALUE	ACHIEVED RESULT
Throughput	10 kSPS	10 kSPS
SNR at 100 Hz	70 dB	70.6 dB
THD at 100 Hz	-75 dB	-83.5 dB
SINAD at 100 Hz	69 dB	70.4 dB
ENOB	11 bits	11.4 bits
Power	20 μW	17 μW

10 Power Supply Recommendations

10.1 AVDD and DVDD Supply Recommendations

The device has two separate power supplies: AVDD and DVDD.

AVDD powers the analog blocks and is also used as the reference voltage for the analog-to-digital conversion. Use a low-noise, low-dropout regulator (LDO) or a discrete reference to supply AVDD (see the [Reference](#) and [Application Information](#) sections). Always set the AVDD supply to be greater than or equal to the maximum input signal to avoid code saturation. Decouple the AVDD pin to the GND pin with a 3.3- μ F ceramic decoupling capacitor.

DVDD is used for the interface circuits. Decouple the DVDD pin to the GND pin with a 1- μ F ceramic decoupling capacitor. [Figure 49](#) shows the decoupling recommendations.

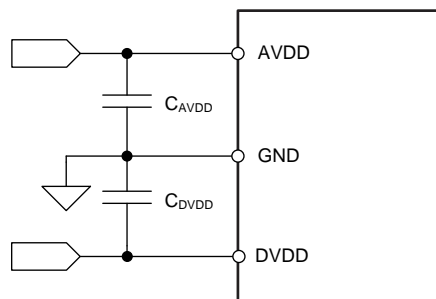


Figure 49. Power-Supply Decoupling

10.2 Optimizing Power Consumed by the Device

In order to best optimize the power consumed by the device, use the following design considerations:

- Keep the analog supply voltage (AVDD) in the specified operating range and equal to the maximum analog input voltage.
- Keep the digital supply voltage (DVDD) in the specified operating range and at the lowest value supported by the host controller.
- Reduce the load capacitance on the SDO output.
- Run the device at the optimum throughput. Power consumption reduces proportionally with the throughput.

10.2.1 Estimating Digital Power Consumption

The current consumption from the DVDD supply depends on the DVDD voltage, the load capacitance on the SDO pin ($C_{\text{LOAD-SDO}}$), and the output code, and can be calculated as:

$$I_{\text{DVDD}} = C_{\text{LOAD-SDO}} \times V \times f$$

where:

- $C_{\text{LOAD-SDO}}$ = Load capacitance on the SDO pin
 - V = DVDD supply voltage
 - f = Frequency of transitions on the SDO output
- (2)

The number of transitions on the SDO output depends on the output code, and thus changes with the analog input. The maximum value of f occurs when data output on the SDO change on every SCLK (that is, for output codes of AAAh or 555h). With an output code of AAAh or 555h, $f = 18$ MHz and when $C_{\text{LOAD-SDO}} = 20$ pF and $\text{DVDD} = 1.8$ V, $I_{\text{DVDD}} = 650$ μ A.

11 Layout

11.1 Layout Guidelines

Figure 50 shows a typical connection diagram for the ADS7046.

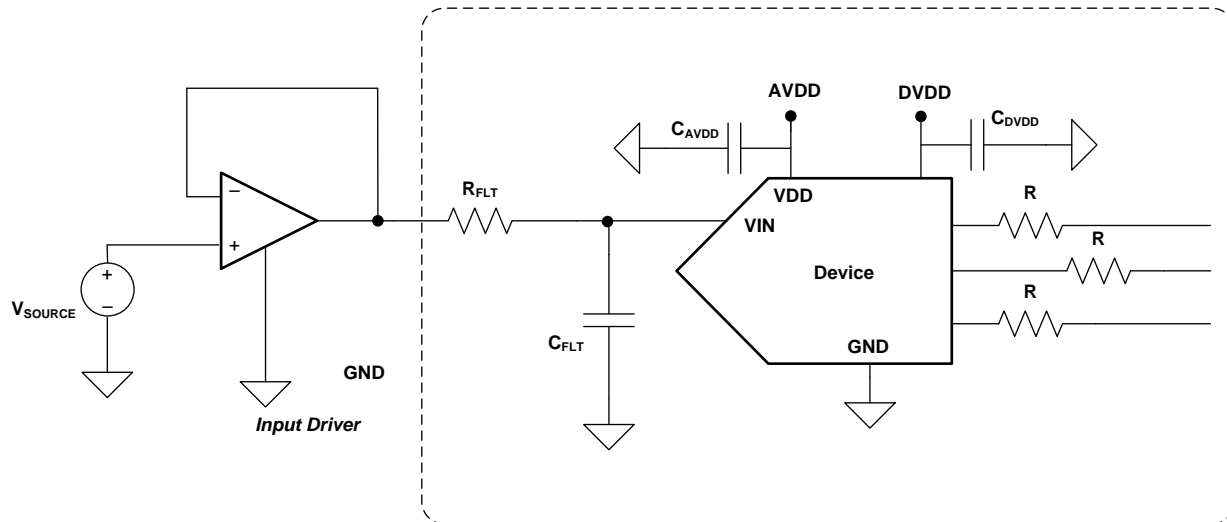


Figure 50. Typical Connection Diagram

Figure 51 depicts a board layout example for the device for the typical connection diagram in Figure 50. The key considerations for layout are:

- Use a solid ground plane underneath the device and partition the PCB into analog and digital sections
- Avoid crossing digital lines with the analog signal path and keep the analog input signals and the reference input signals away from noise sources.
- The power sources to the device must be clean and well-bypassed. Use C_{AVDD} decoupling capacitors in close proximity to the analog (AVDD) power-supply pin.
- Use a C_{DVDD} decoupling capacitor close to the digital (DVDD) power-supply pin.
- Avoid placing vias between the AVDD and DVDD pins and the bypass capacitors.
- Connect the ground pin to the ground plane using a short, low-impedance path.
- Place the charge kickback filter components close to the device.

Among ceramic surface-mount capacitors, COG (NPO) ceramic capacitors are recommended because these components provide the most stable electrical properties over voltage, frequency, and temperature changes.

11.2 Layout Example

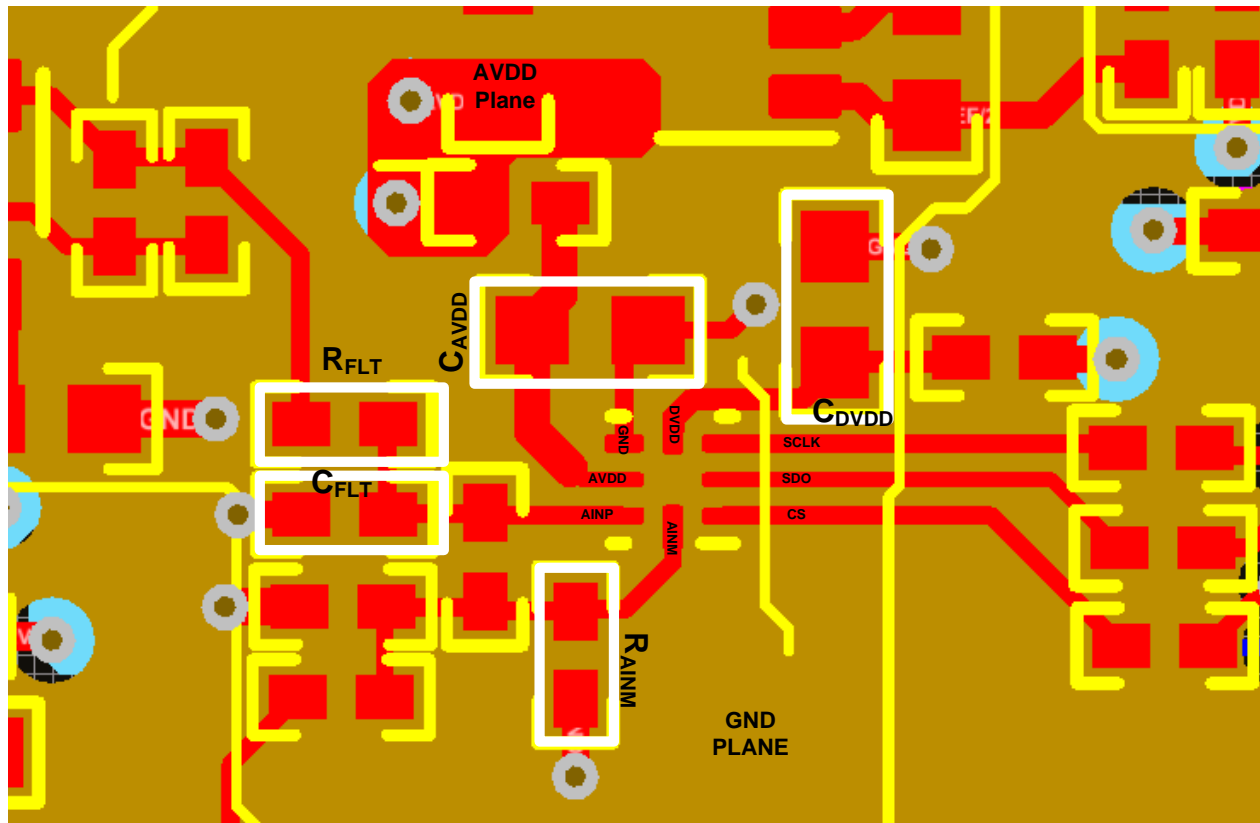


Figure 51. Example Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

[TI Precision Labs Training Video Series](#)

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

Input Driver Amplifier (Single-Ended Inputs):

- [OPAx836 Very-Low-Power, Rail-to-Rail Out, Negative-Rail In, Voltage-Feedback Operational Amplifiers](#)
- [THS403x 100-MHz Low-Noise High-Speed Amplifiers](#)
- [OPAx365 50-MHz, Zero-Crossover, Low-Distortion, High CMRR, RRI/O, Single-Supply Operational Amplifier](#)

Input Driver Amplifier (Fully-Differential Inputs):

- [THS4551 Low-Noise, Precision, 150-MHz, Fully Differential Amplifier](#)
- [OPAx836 Very-Low-Power, Rail-to-Rail Out, Negative-Rail In, Voltage-Feedback Operational Amplifiers](#)

Reference Driver:

- [REF19xx Low-Drift, Low-Power, Dual-Output, \$V_{REF}\$ and \$V_{REF} / 2\$ Voltage References](#)
- [REF61xx High-Precision Voltage Reference With Integrated ADC Drive Buffer](#)

Similar Devices:

- [ADS7042 Ultra-Low Power, Ultra-Small Size, 12-Bit, 1-MSPS, SAR ADC](#)
- [ADS7049-Q1 Small-Size, Low-Power, 12-Bit, 2-MSPS, SAR ADC](#)

Reference Designs:

- [TI Design: Analog Front-End Reference Design for Imaging Using Time-Interleaved SAR ADCs With 73-dB SNR, 7.5 MSPS](#)
- [Single-Ended to Differential Using an Op Amp and FDA for Bipolar Signals](#)

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

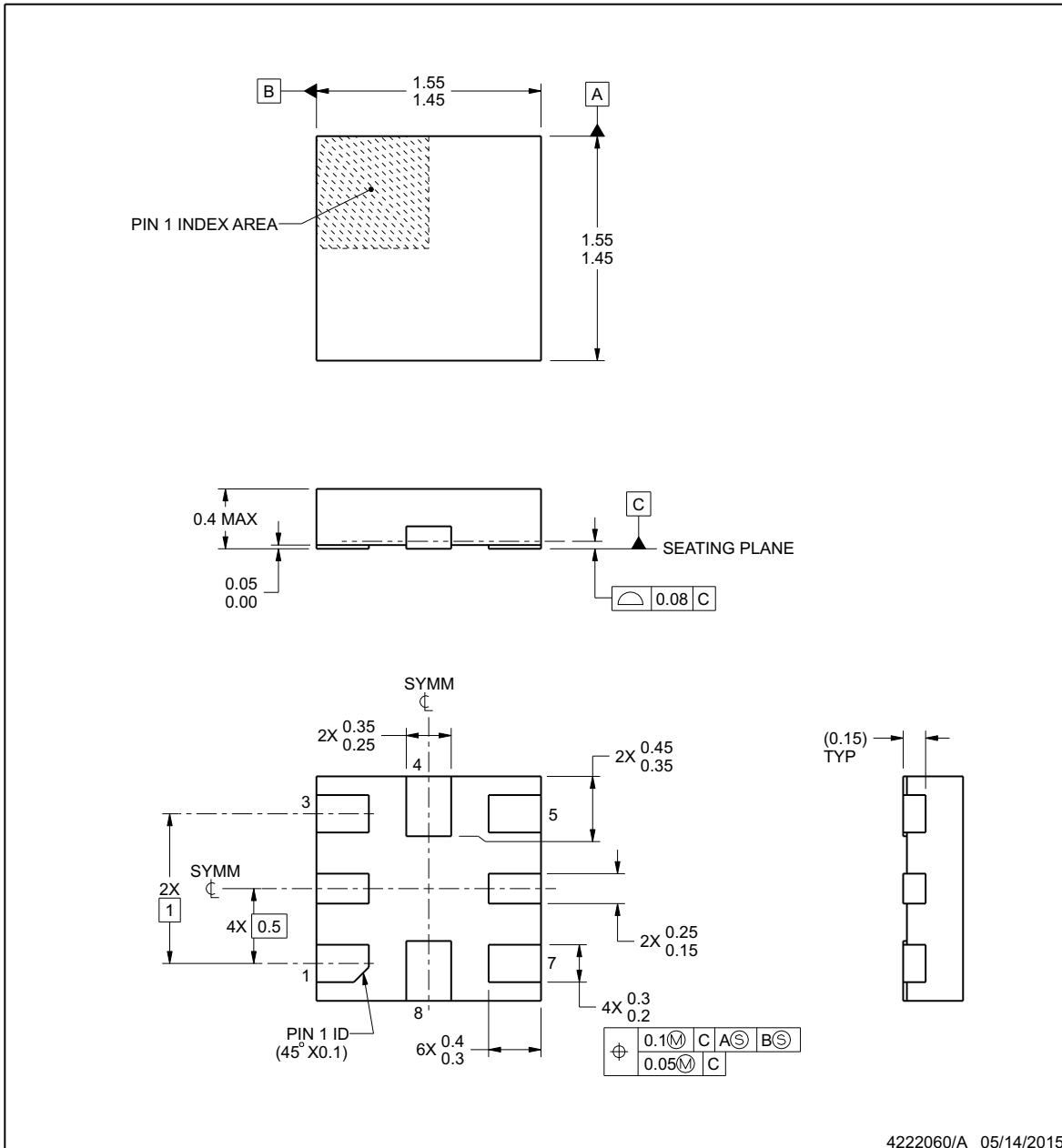
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



RUG0008A

PACKAGE OUTLINE
X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

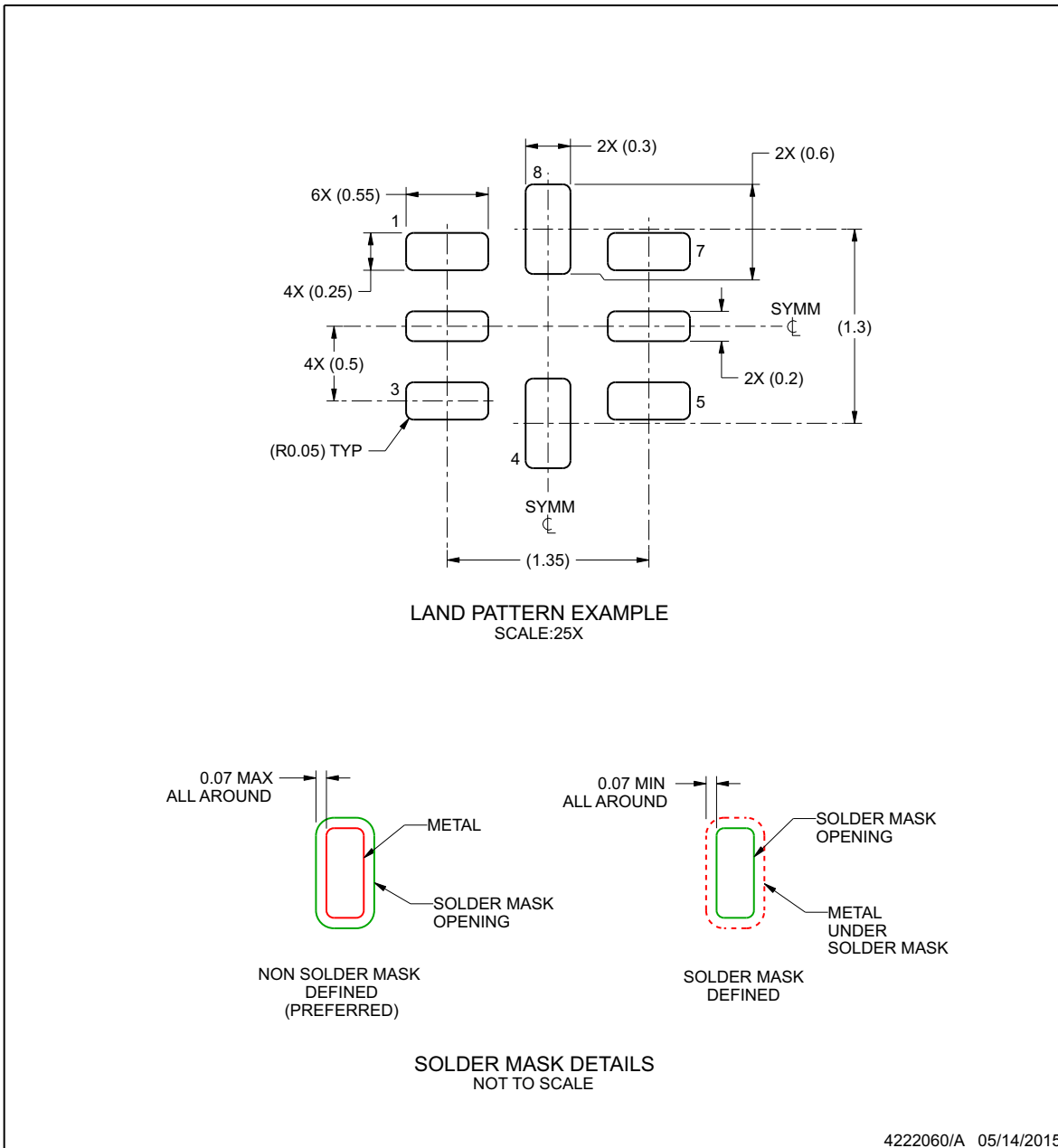
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

RUG0008A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

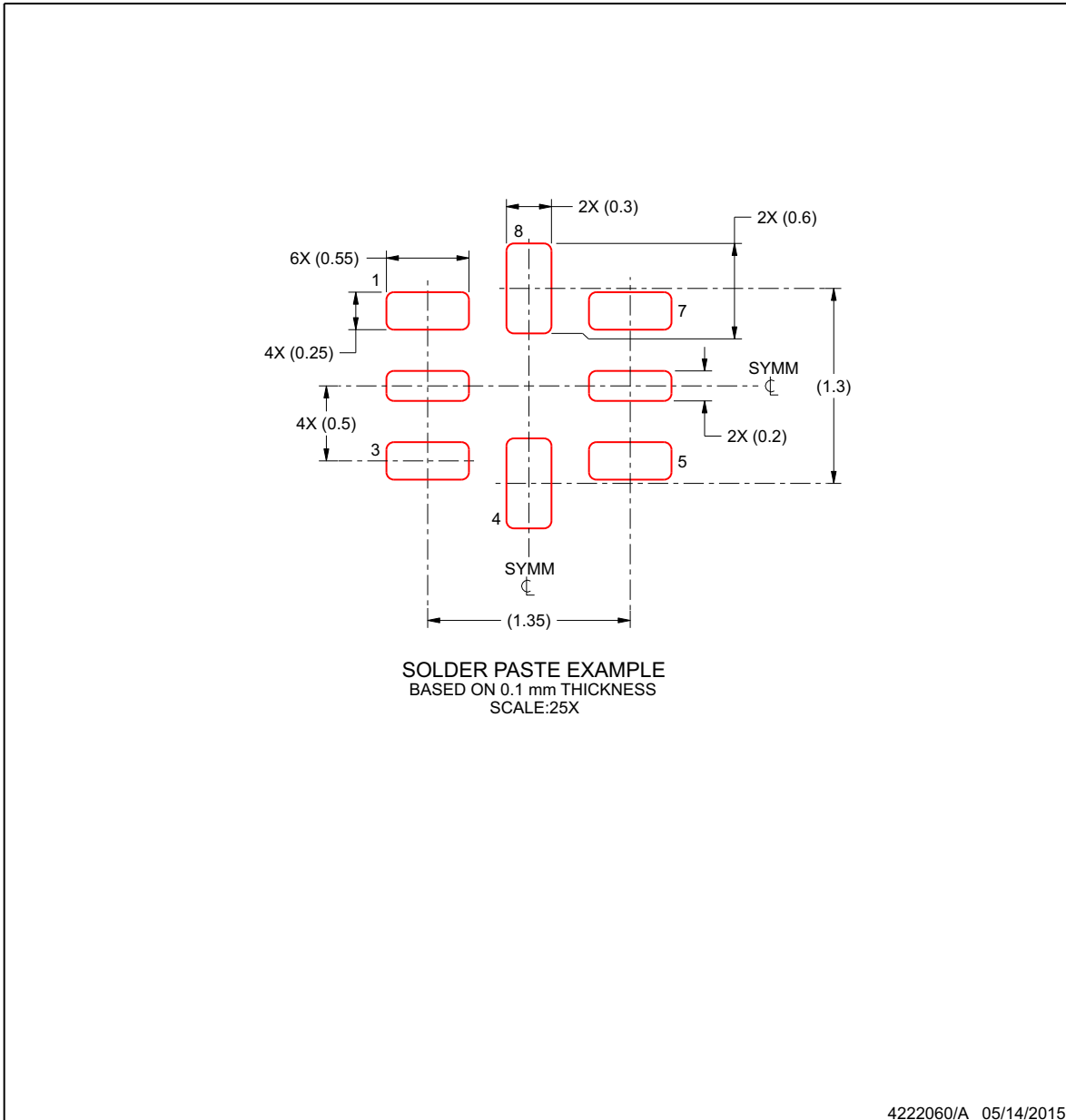
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RUG0008A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

- 4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS7046IRUGR	Active	Production	X2QFN (RUG) 8	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	9R
ADS7046IRUGR.A	Active	Production	X2QFN (RUG) 8	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	9R

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7046IRUGR	X2QFN	RUG	8	3000	180.0	8.4	1.6	1.6	0.66	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

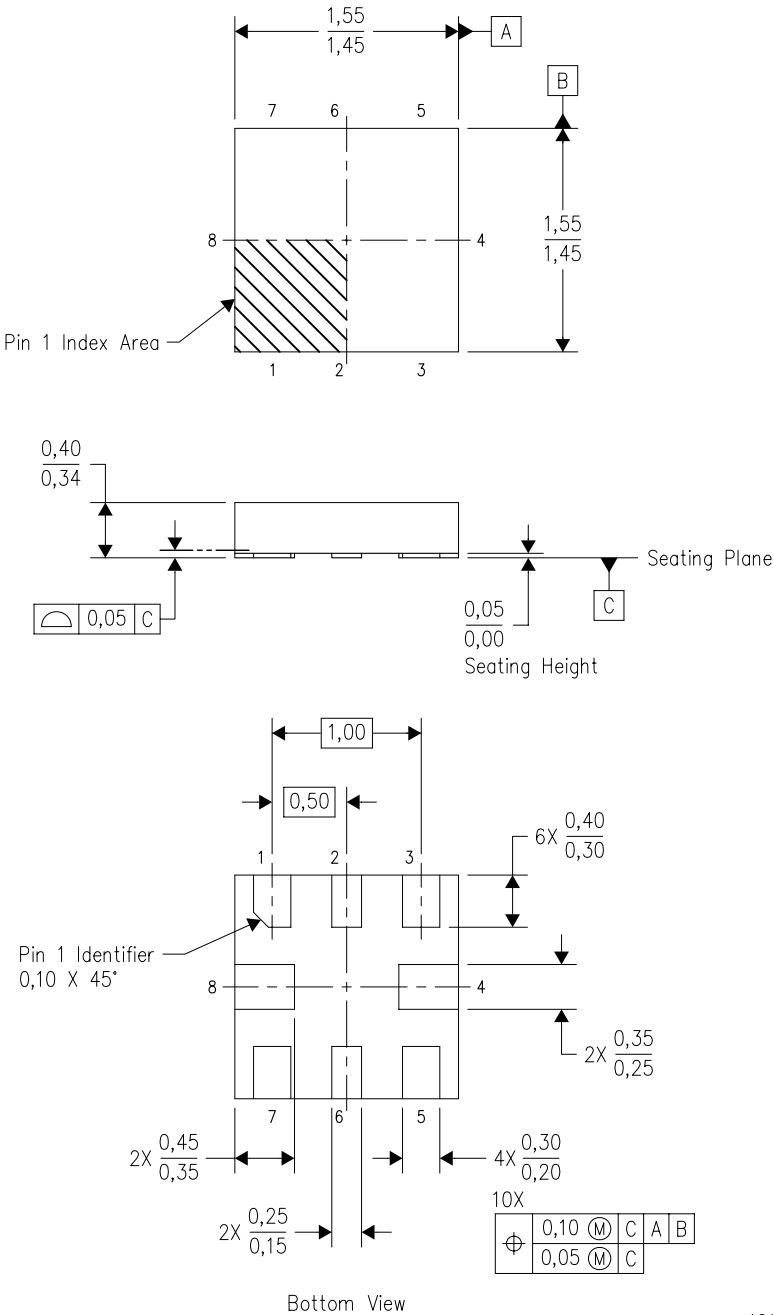


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7046IRUGR	X2QFN	RUG	8	3000	183.0	183.0	20.0

RUG (S-PQFP-N8)

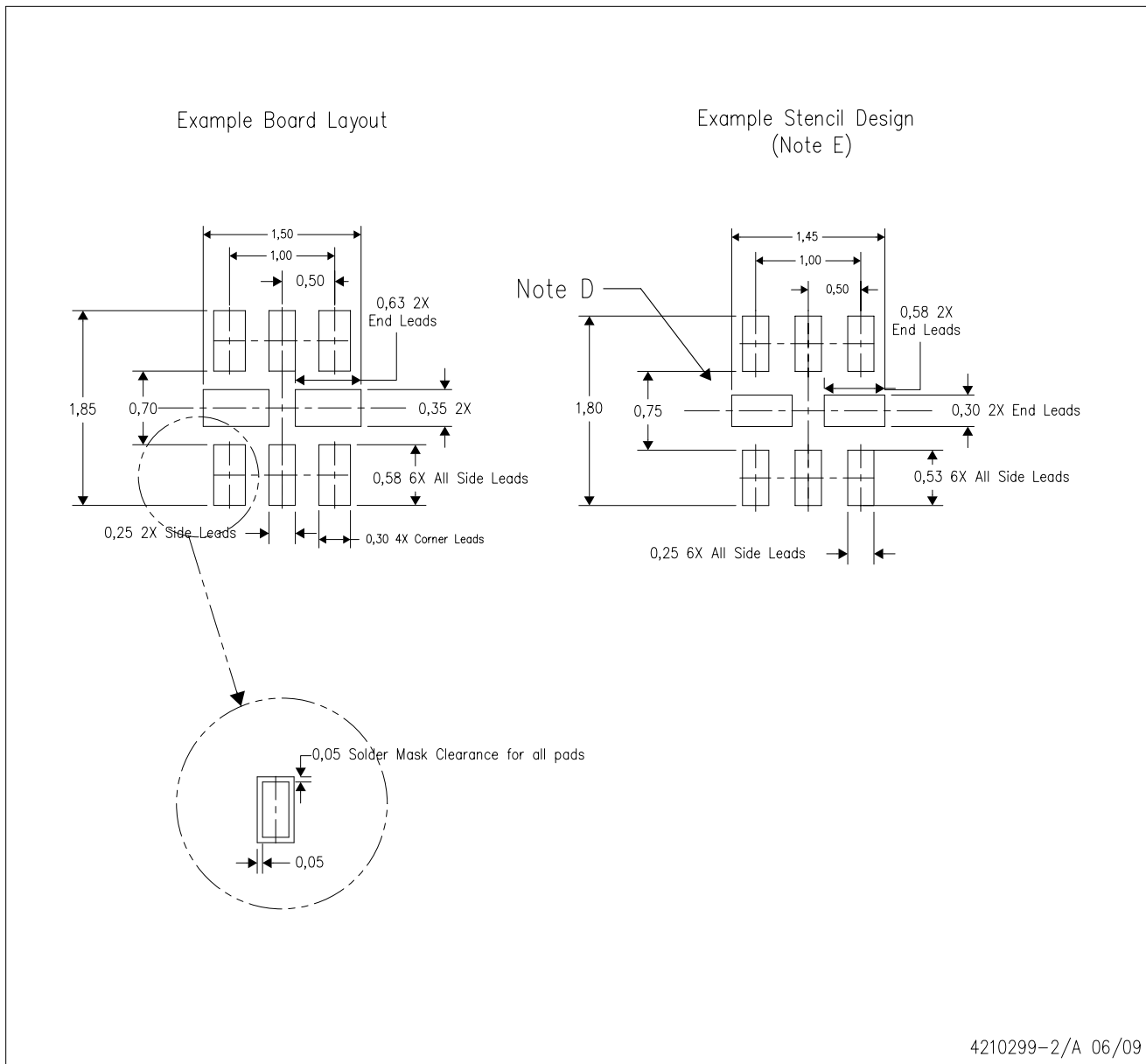
PLASTIC QUAD FLATPACK



4208528-2/B 04/2008

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - D. This package complies to JEDEC MO-288 variation X2ECD.

RUG (R-PQFP-N8)



4210299-2/A 06/09

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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