Dual Channel 14-/12-Bit, 250-/210-MSPS ADC With DDR LVDS and Parallel CMOS Outputs

Check for Samples: ADS62P49 / ADS62P29, ADS62P48 / ADS62P28

FEATURES

- **Maximum Sample Rate: 250 MSPS**
- **14-Bit Resolution – ADS62P49/ADS62P48**
- **12-Bit Resolution – ADS62P29/ADS62P28**
- **Total Power: 1.25 W at 250 MSPS**
- **Double Data Rate (DDR) LVDS and Parallel CMOS Output Options**
- **Programmable Gain up to 6dB for SNR/SFDR Trade-Off**
- **DC Offset Correction**
- **90dB Cross-Talk**
- **Supports Input Clock Amplitude Down to 400 mV_{PP} Differential**
- **Internal and External Reference Support**
- **64-QFN Package (9 mm × 9 mm)**

ADS62Pxx High Speed Family

	250 MSPS	210 MSPS	200 MSPS
14-Bit Family	ADS62P49	ADS62P48	
12-Bit Family	ADS62P29	ADS62P28	
11-Bit Family			ADS62C17

DESCRIPTION

The ADS62Px9/x8 is a family of dual channel 14-bit and 12-bit A/D converters with sampling rates up to 250 MSPS. It combines high dynamic performance and low power consumption in a compact 64 QFN package. This makes it well-suited for multi-carrier, wide band-width communications applications.

The ADS62Px9/x8 has gain options that can be used to improve SFDR performance at lower full-scale input ranges. It includes a dc offset correction loop that can be used to cancel the ADC offset. Both DDR LVDS (Double Data Rate) and parallel CMOS digital output interfaces are available.

It includes internal references while the traditional reference pins and associated decoupling capacitors have been eliminated. Nevertheless, the device can also be driven with an external reference. The device is specified over the industrial temperature range (–40°C to 85°C).

Table 1. Performance Summary

AT 170MHZ INPUT		ADS62P49	ADS62P48	ADS62P29	ADS62P28
SFDR, dBc	0 dB gain	75	78	75	78
	6 dB gain	82	84	82	84
SINAD, dBFS	0 dB gain	69.8	70.1	68.3	68.7
	6 dB gain	66.5	66.3	65.8	65.8
Analog Power, W		1	0.92	1	0.92

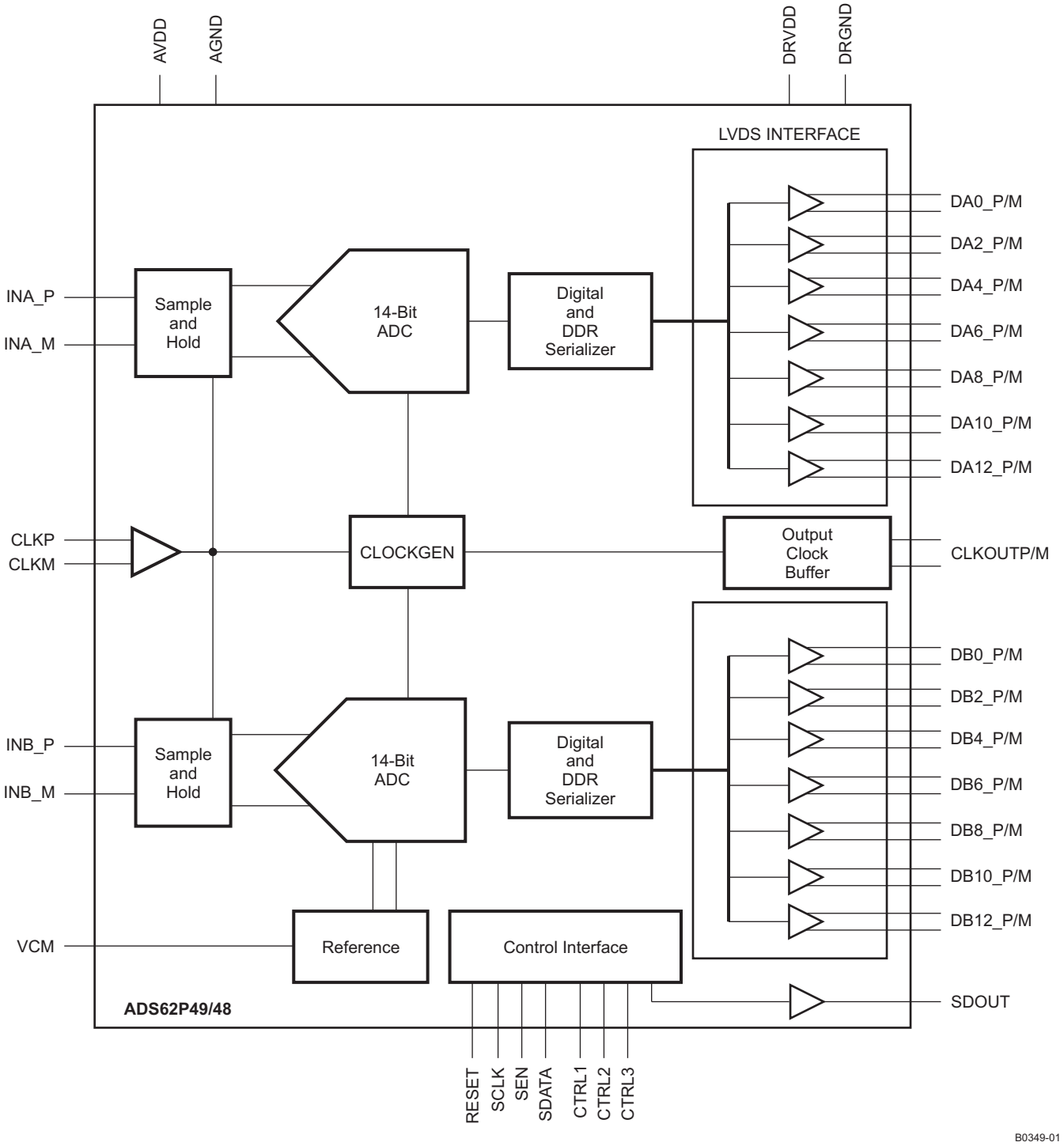


Figure 1. ADS62P49/48 Block Diagram

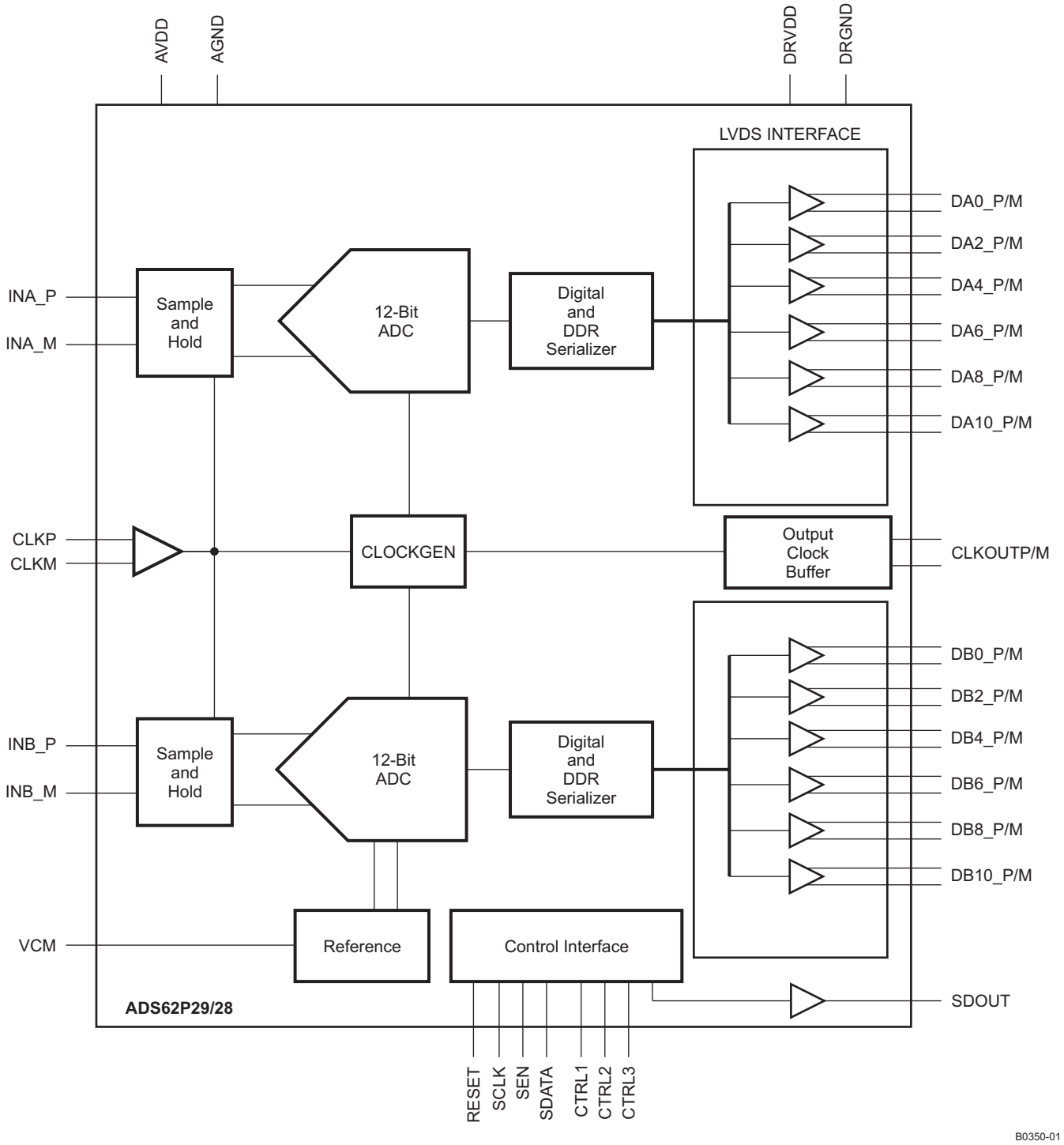


Figure 2. ADS62P29/28 Block Diagram

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	ECO PLAN(2)	LEAD/BALL FINISH	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA,QUANTITY
ADS62P49	QFN-64	RGC	–40°C to 85°C	GREEN (RoHS and no Sb/Br)	Cu NiPdAu	AZ62P49	ADS62P49IRGCT, ADS62P49IRGCR	Tape and Reel
ADS62P48						AZ62P48	ADS62P48IRGCT, ADS62P48IRGCR	
ADS62P29						AZ62P29	ADS62P29IRGCT, ADS62P29IRGCR	Tape and Reel
ADS62P28						AZ62P28	ADS62P28IRGCT, ADS62P28IRGCR	

(1) For the most current product and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Eco Plan – The planned eco-friendly classification: Green (RoHS and no Sb/Br): TI defines “Green” to mean Pb-Free (RoHS compatible) and free of Bromine (Br) and Antimony (Sb) based flame retardants.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
	Supply voltage range, AVDD	–0.3 V to 3.9	V
	Supply voltage range, DRVDD	–0.3 V to 2.2	V
	Voltage between AGND and DRGND	–0.3 to 0.3	V
	Voltage between AVDD to DRVDD (AVDD leads DRVDD during power up/DRVDD leads AVDD during power down)	–0.3 to 4.2	V
	Voltage between DRVDD to AVDD (DRVDD leads AVDD during power up/AVDD leads DRVDD during power down)	–2.5 to 1.7	V
	Voltage applied to external pin, VCM (in external reference mode)	–0.3 to 2.0	V
	Voltage applied to analog input pins – INP_A, INM_A, INP_B, INM_B	–0.3V to minimum (3.6, AVDD + 0.3V)	V
	Voltage applied to input pins - CLKP, CLKM(2), RESET, SCLK, SDATA, SEN, CTRL1, CTRL2, CTRL3	–0.3V to AVDD + 0.3V	V
T_A	Operating free-air temperature range	–40 to 85	°C
T_J	Operating junction temperature range	125	°C
T_{stg}	Storage temperature range	–65 to 150	°C
	ESD, human body model	2	kV

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) When AVDD is turned off, it is recommended to switch off the input clock (or ensure the voltage on CLKP, CLKM is < |0.3V|). This prevents the ESD protection diodes at the clock input pins from turning on.

THERMAL INFORMATION

THERMAL METRIC(1)		ADS62Pxx RGC PACKAGE 64 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	23.0	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	10.5	
θ_{JB}	Junction-to-board thermal resistance(4)	4.2	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.1	
ψ_{JB}	Junction-to-board characterization parameter(6)	4.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	0.57	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNIT
SUPPLIES						
AVDD	Analog supply voltage		3.15	3.3	3.6	V
DRVDD	Digital supply voltage		1.7	1.8	1.9	V
ANALOG INPUTS						
	Differential input voltage range			2		V_{PP}
	Input common-mode voltage			1.5 ±0.1		V
	Voltage applied on CM in external reference mode			1.5±0.05		V
	Maximum analog input frequency with 2 V_{pp} input amplitude(1)			500		MHz
	Maximum analog input frequency with 1 V_{pp} input amplitude(1)			800		MHz
CLOCK INPUT						
	Input clock sample rate					
	ADS62P49 / ADS62P29	Enable low speed mode(2)	1		80	MSPS
		Low speed mode disabled (default mode after reset)	>80		250(3)	MSPS
	ADS62P48 / ADS62P28	Enable low speed mode(2)	1		80	MSPS
		Low speed mode disabled (default mode after reset)	>80		210	MSPS
		With multiplexed mode enabled(4)	1		65	MSPS
	Input clock amplitude differential (V_{CLKP}–V_{CLKM}) (5)(6)					
		Sine wave, ac-coupled	0.2	1.5		V_{PP}
		LVPECL, ac-coupled		1.6		V_{PP}
		LVDS, ac-coupled		0.7		V_{PP}
		LVCMOS, single-ended, ac-coupled		3.3		V
	Input clock duty cycle		40%	50%	60%	
DIGITAL OUTPUTS						
C_{LOAD}	Maximum external load capacitance from each output pin to DRGND			5		pF
R_{LOAD}	Differential load resistance between the LVDS output pairs (LVDS mode)			100		Ω
T_A	Operating free-air temperature		–40		85	°C

(1) See the Theory of Operation section for information.
(2) Use register bit <ENABLE LOW SPEED MODE>, refer to the Serial Register Map section for information.
(3) With LVDS interface only; maximum recommended sample rate with CMOS interface is 210 MSPS.
(4) See the Multiplexed Output Mode section for information.
(5) Refer to Performance vs Input Clock Amplitude Chart on Figure 35, Figure 52, Figure 69, and Figure 86.
(6) Refer to Figure 3 for the definition of clock amplitude.

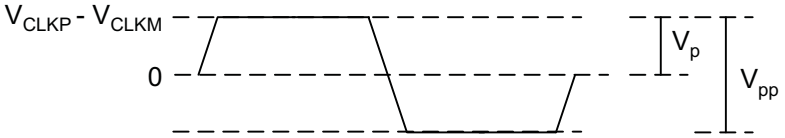


Figure 3. Clock Amplitude Definition Diagram

ELECTRICAL CHARACTERISTICS – ADS62P49/48 and ADS62P29/28

Typical values are at 25°C, AVDD = 3.3V, DRVDD = 1.8V, 50% clock duty cycle, –1dBFS differential analog input, internal reference mode (unless otherwise noted).

Min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 3.3V, DRVDD = 1.8V

PARAMETER			ADS62P49/ADS62P29 250 MSPS			ADS62P48/ADS62P28 210 MSPS			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUT									
	Differential input voltage range (0 dB gain)			2			2		Vpp
	Differential input resistance (at dc), See Figure 100			> 1			> 1		MΩ
	Differential input capacitance, See Figure 101			3.5			3.5		pF
	Analog input bandwidth (with 25Ω source impedance)			700			700		MHz
	Analog Input common mode current (per channel)			3.6			3.6		µA/MSPS
VCM	Common mode output voltage			1.5			1.5		V
VCM	Output current capability			±4			±4		mA
DC ACCURACY									
	Offset error		–20	±2	20	–20	±2	20	mV
	Temperature coefficient of offset error			0.02			0.02		mV/ °C
	Variation of offset error with supply			0.5			0.5		mV/V
	There are two sources of gain error – internal reference inaccuracy and channel gain error.								
E_{GREF}	Gain error due to internal reference inaccuracy alone		–1	±0.2	1	–1	±0.2	1	% FS
E_{GCHAN}	Gain error of channel alone (1)		–1	±0.2	1	–1	±0.2	1	% FS
	Temperature coefficient of E_{GCHAN}			0.002			0.002		Δ% /°C
	Gain matching (2)	Difference in gain errors between two channels within the same device	–2		2	–2		2	% FS
		Difference in gain errors between two channels across two devices	–4		4	–4		4	
POWER SUPPLY									
IAVDD	Analog supply current			305	350		280	320	mA
IDRVDD	Output buffer supply current, LVDS interface with 100 Ω external termination			133	175		122	165	mA
IDRVDD	Output buffer supply current, CMOS interface, Fin = 2MHz, No external load capacitance (3) (4)			–			91		mA
	Analog power			1.01	1.15		0.92	1.05	W
	Digital power, LVDS interface			0.24	0.315		0.22	0.3	W
	Global power down			45	100		45	100	mW

(1) This is specified by design and characterization; it is not tested in production.
(2) For two channels within the same device, only the channel gain error matters, as the reference is common for both channels.
(3) In CMOS mode, the DRVDD current scales with the sampling frequency, the load capacitance on output pins, input frequency and the supply voltage (see Figure 92 and CMOS interface power dissipation in application section).
(4) The maximum DRVDD current with CMOS interface depends on the actual load capacitance on the digital output lines. Note that the maximum recommended load capacitance on each digital output line is 10 pF.

ELECTRICAL CHARACTERISTICS – ADS62P49/48

Typical values are at 25°C, AVDD = 3.3V, DRVDD = 1.8V, 50% clock duty cycle, –1dBFS differential analog input, 0 dB gain, internal reference mode (unless otherwise noted).
Min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 3.3V, DRVDD = 1.8V

PARAMETER	TEST CONDITIONS		ADS62P49 250 MSPS			ADS62P48 210 MSPS			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SNR Signal to noise ratio, **LVDS**	Fin= 20 MHz			73.4			73.4		dBFS
	Fin = 60 MHz			73			73		
	Fin = 100 MHz			72			72		
	Fin = 170 MHz	0 dB gain	68	71		68	71		
		6 dB gain		66.6			66.4		
	Fin = 230 MHz			69.8			69.7		
SINAD Signal to noise and distortion ratio, **LVDS**	Fin= 20 MHz			73.2			73		dBFS
	Fin = 60 MHz			72.7			72.8		
	Fin = 100 MHz			71.2			71.5		
	Fin = 170 MHz	0 dB gain	66.5	69.8		66.5	70.1		
		6 dB gain		66.5			66.3		
	Fin = 230 MHz			69			68		
ENOB, Effective number of bits	Fin = 170 MHz			11.3			11.4		LSB
DNL Differential non-linearity	Fin = 170 MHz		–0.95	±0.6	1.3	–0.95	±0.6	1.3	LSB
INL Integrated non-linearity	Fin = 170 MHz		–5	±2.5	5	–5	±2.5	5	LSB

ELECTRICAL CHARACTERISTICS – ADS62P29/28

Typical values are at 25°C, AVDD = 3.3V, DRVDD = 1.8V, 50% clock duty cycle, –1dBFS differential analog input, 0 dB gain, internal reference mode (unless otherwise noted).
Min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 3.3V, DRVDD = 1.8V

PARAMETER	TEST CONDITIONS		ADS62P29 250 MSPS			ADS62P28 210 MSPS			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SNR Signal to noise ratio, **LVDS**	Fin= 20 MHz			70.7			70.8		dBFS
	Fin = 60 MHz			70.5			70.6		
	Fin = 100 MHz			69.8			70		
	Fin = 170 MHz	0 dB gain	66.5	69.4		66.5	69.4		
		6 dB gain		66			65.9		
	Fin = 230 MHz			68.4			68.4		
SINAD Signal to noise and distortion ratio, **LVDS**	Fin= 20 MHz			70.6			70.6		dBFS
	Fin = 60 MHz			70.3			70.5		
	Fin = 100 MHz			69.3			69.7		
	Fin = 170 MHz	0 dB gain	66	68.3		66	68.7		
		6 dB gain		65.9			65.8		
	Fin = 230 MHz			67.9			67.1		
ENOB, Effective number of bits	Fin = 170 MHz			11			11.1		LSB
DNL Differential non-linearity			–0.9	±0.2	1.3	–0.9	±0.2	1.3	LSB
INL Integrated non-linearity			–5	±1	5	–5	±1	5	LSB

ELECTRICAL CHARACTERISTICS – ADS62P49/48

Typical values are at 25°C, AVDD = 3.3V, DRVDD = 1.8V, 50% clock duty cycle, –1dBFS differential analog input, 0 dB gain, internal reference mode (unless otherwise noted).

Min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 3.3V, DRVDD = 1.8V

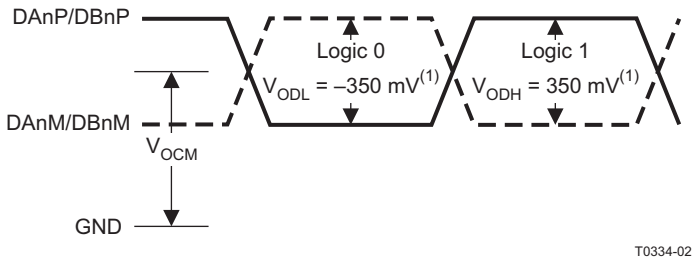
PARAMETER	TEST CONDITIONS	ADS62P49/ADS62P29 250 MSPS			ADS62P48/ADS62P28 210 MSPS			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
SFDR Spurious Free Dynamic Range	Fin= 20 MHz		89			85		dBc
	Fin = 60 MHz		85			85		
	Fin = 100 MHz		78			80		
	Fin = 170 MHz	71	75		71	77		
	Fin = 230 MHz		77			72		
SFDR Spurious Free Dynamic Range, excluding HD2,HD3	Fin= 20 MHz		98			98		dBc
	Fin = 60 MHz		95			95		
	Fin = 100 MHz		92			92		
	Fin = 170 MHz	77	90		78	91		
	Fin = 230 MHz		90			90		
HD2 Second Harmonic Distortion	Fin= 20 MHz		93			95		dBc
	Fin = 60 MHz		90			94		
	Fin = 100 MHz		90			90		
	Fin = 170 MHz	71	85		71	88		
	Fin = 230 MHz		85			80		
HD3 Third Harmonic Distortion	Fin= 20 MHz		89			85		dBc
	Fin = 60 MHz		85			85		
	Fin = 100 MHz		78			80		
	Fin = 170 MHz	71	75		71	77		
	Fin = 230 MHz		77			72		
THD Total harmonic distortion	Fin= 20 MHz		87			83.5		dBc
	Fin = 60 MHz		83.5			84.6		
	Fin = 100 MHz		77.5			79.7		
	Fin = 170 MHz	70	74		70.5	76.5		
	Fin = 230 MHz		75			71		
IMD 2-Tone Inter-modulation Distortion	F1 = 46 MHz, F2 = 50 MHz, each tone at –7 dBFS		87			91		dBFS
	F1 = 185 MHz, F2 = 190 MHz, each tone at –7 dBFS		85			84.5		
Cross-talk	Up to 200-MHz cross-talk frequency		90			90		dB
Input overload recovery	Recovery to within 1% (of final value) for 6-dB overload with sine wave input		1			1		Clock Cycles
PSRR AC Power supply rejection ratio	For 100-mV pp signal on AVDD supply		25			25		dB

DIGITAL CHARACTERISTICS — ADS62Px9/x8

The DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1. AVDD = 3.3V, DRVDD = 1.8V

PARAMETER		TEST CONDITIONS	ADS62P49/ADS62P48/ ADS62P29/ADS62P28			UNIT
			MIN	TYP	MAX	
DIGITAL INPUTS – CTRL1, CTRL2, CTRL3, RESET, SCLK, SDATA, SEN(1)						
High-level input voltage		All digital inputs support 1.8V and 3.3V CMOS logic levels.	1.3			V
Low-level input voltage					0.4	V
High-level input current	SDATA, SCLK(2)	V_{HIGH} = 3.3 V		16		µA
	SEN(3)			10		
Low-level input current	SDATA, SCLK	V_{LOW} = 0 V		0		µA
	SEN			–20		
Input capacitance				4		pF
DIGITAL OUTPUTS – CMOS INTERFACE (DA0-DA13, DB0-DB13, CLKOUT, SDOUT)						
High-level output voltage		I_{OH} = 1mA	DRVDD –0.1	DRVDD		V
Low-level output voltage		I_{OL} = 1mA		0	0.1	V
Output capacitance (internal to device)				2		pF
DIGITAL OUTPUTS – LVDS INTERFACE						
V_{ODH} High-level output differential voltage		With external 100 Ω termination.	275	350	425	mV
V_{ODL} Low-level output differential voltage		With external 100 Ω termination.	–425	–350	–275	mV
V_{OCM} Output common-mode voltage			1	1.15	1.4	V
Output Capacitance		Capacitance inside the device from each output to ground		2		pF

(1) SCLK, SDATA, SEN function as digital input pins in serial configuration mode.
(2) SDATA, SCLK, RESET, CTRL1, CTRL2, and CTRL3 have an internal 100-kΩ pull-down resistor.
(3) SEN has internal 100 kΩ pull-up resistor to AVDD. Since the pull-up is weak, SEN can also be driven by 1.8V or 3.3V CMOS buffers.



(1) With external 100-Ω termination

Figure 4. LVDS Output Voltage Levels

TIMING REQUIREMENTS – LVDS AND CMOS MODES(1)

Typical values are at 25°C, AVDD = 3.3V, DRVDD = 1.8V, sampling frequency = 250 MSPS, sine wave input clock, 1.5 Vpp clock amplitude, C_{LOAD} = 5pF(2) , R_{LOAD} = 100Ω(3) , (unless otherwise noted).
Min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 3.3V, DRVDD = 1.7V to 1.9V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_a	Aperture delay		0.7	1.2	1.7	ns
	Aperture delay matching	Between two channels within the same device		±50		ps
t_j	Aperture jitter			145		fs rms
	Wake-up time	Time to valid data after coming out of STANDBY mode		1	3	µs
		Time to valid data after coming out of global powerdown		20	50	µs
		Time to valid data after stopping and restarting the input clock		10		Clock cycles
	ADC latency(4)			22		Clock cycles
DDR LVDS MODE(5)						
t_{su}	Data setup time	Data valid(6) to zero-crossing of CLKOUTP	0.55	0.9		ns
t_h	Data hold time	Zero-crossing of CLKOUTP to data becoming invalid(6)	0.55	0.95		ns
t_{PDI}	Clock propagation delay	Input clock falling edge cross-over to output clock rising edge cross-over *100 MSPS ≤ Sampling frequency ≤ 250 MSPS* *Ts = 1/Sampling frequency*	$t_{PDI} = 0.69 \times Ts + t_{delay}$			
t_{delay}			4.2	5.7	7.2	ns
	t_{delay} skew	Difference in t_{delay} between two devices operating at same temperature and DRVDD supply voltage		±500		ps
	LVDS bit clock duty cycle	Duty cycle of differential clock, (CLKOUTP-CLKOUTM) *100 MSPS ≤ Sampling frequency ≤ 250 MSPS*		52%		
t_{RISE}, t_{FALL}	Data rise time, Data fall time	Rise time measured from –100mV to +100mV Fall time measured from +100mV to –100mV *1MSPS ≤ Sampling frequency ≤ 250 MSPS*		0.14		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, Output clock fall time	Rise time measured from –100mV to +100mV Fall time measured from +100mV to –100mV *1 MSPS ≤ Sampling frequency ≤ 250 MSPS*		0.14		ns
t_{OE}	Output buffer enable to data delay	Time to valid data after output buffer becomes active		100		ns
PARALLEL CMOS MODE(7) at Fs = 210 MSPS						
t_{START}	Input clock to data delay	Input clock falling edge cross-over to start of data valid(8)			2.5	ns
t_{DV}	Data valid time	Time interval of valid data(8)	1.7	2.7		ns
t_{PDI}	Clock propagation delay	Input clock falling edge cross-over to output clock rising edge cross-over *100 MSPS ≤ Sampling frequency ≤ 150 MSPS* *Ts = 1/Sampling frequency*	$t_{PDI} = 0.28 \times Ts + t_{delay}$			
t_{delay}			5.5	7.0	8.5	ns
	Output clock duty cycle	Duty cycle of output clock, CLKOUT *100 MSPS ≤ Sampling frequency ≤ 150 MSPS*		43%		
t_{RISE}, t_{FALL}	Data rise time, Data fall time	Rise time measured from 20% to 80% of DRVDD Fall time measured from 80% to 20% of DRVDD *1 ≤ Sampling frequency ≤ 210 MSPS*		1.2		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, Output clock fall time	Rise time measured from 20% to 80% of DRVDD Fall time measured from 80% to 20% of DRVDD *1 ≤ Sampling frequency ≤ 150 MSPS*		0.8		ns

(1) Timing parameters are ensured by design and characterization and not tested in production
(2) C_{LOAD} is the effective external single-ended load capacitance between each output pin and ground
(3) R_{LOAD} is the differential load resistance between the LVDS output pair.
(4) At higher clock frequencies, t_{PDI} is greater than one clock period and overall latency = ADC latency + 1.
(5) Measurements are done with a transmission line of 100Ω characteristic impedance between the device and the load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.
(6) Data valid refers to LOGIC HIGH of +100.0mV and LOGIC LOW of –100.0mV.
(7) For Fs> 150 MSPS, it is recommended to use external clock for data capture and NOT the device output clock signal (CLKOUT).
(8) Data valid refers to LOGIC HIGH of 1.26V and LOGIC LOW of 0.54V.

TIMING REQUIREMENTS – LVDS AND CMOS MODES(1) (continued)

Typical values are at 25°C, AVDD = 3.3V, DRVDD = 1.8V, sampling frequency = 250 MSPS, sine wave input clock, 1.5 Vpp clock amplitude, C_{LOAD} = 5pF(2) , R_{LOAD} = 100Ω(3) , (unless otherwise noted).

Min and max values are across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 3.3V, DRVDD = 1.7V to 1.9V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OE}	Output buffer enable (OE) to data delay (9)	Time to valid data after output buffer becomes active		100		ns

(9) Output buffer enable is controlled by Serial Interface Register 0x40. The output buffer becomes active once serial control data for output buffer is latched in on the 16th SCLK falling edge when SEN is low.

Table 2. LVDS Timings at Lower Sampling Frequencies

Sampling Frequency, MSPS	Setup Time, ns			Hold Time, ns		
	MIN	TYP	MAX	MIN	TYP	MAX
210	0.75	1.1		0.75	1.15	
185	0.9	1.25		0.85	1.25	
153	1.15	1.55		1.1	1.5	
125	1.6	2		1.45	1.85	
< 100 *(Enable LOW SPEED mode for Fs ≤ 80)* (1)	2			2		
1 ≤ Fs ≤ 100 *(Enable LOW SPEED mode for Fs ≤ 80)* (1)				t_{PDI}, ns		
				MIN	TYP	MAX
					12.6	

(1) LOW SPEED mode can be enabled with serial interface configuration only.

Table 3. CMOS Timings at Lower Sampling Frequencies

Sampling Frequency, MSPS	Timings Specified With Respect to Input Clock					
	t_{START}, ns			Data Valid time, ns		
	MIN	TYP	MAX	MIN	TYP	MAX
210			2.5	1.7	2.7	
190			1.9	2	3	
170			0.9	2.7	3.7	
150			6	3.6	4.6	

Sampling Frequency, MSPS	Timings Specified With Respect to CLKOUT					
	Setup Time, ns			Hold Time, ns		
	MIN	TYP	MAX	MIN	TYP	MAX
170	2.1	3.7		0.35	1.0	
150	2.8	4.4		0.5	1.2	
125	3.8	5.4		0.8	1.5	
<100 *(Enable LOW SPEED mode for Fs ≤ 80)* (1)	5			1.2		
1 ≤ Fs ≤ 100 *Enable LOW SPEED mode for Fs ≤ 80)* (1)				t_{PDI}, ns		
				MIN	TYP	MAX
					9	

(1) LOW SPEED mode can be enabled with serial interface configuration only.

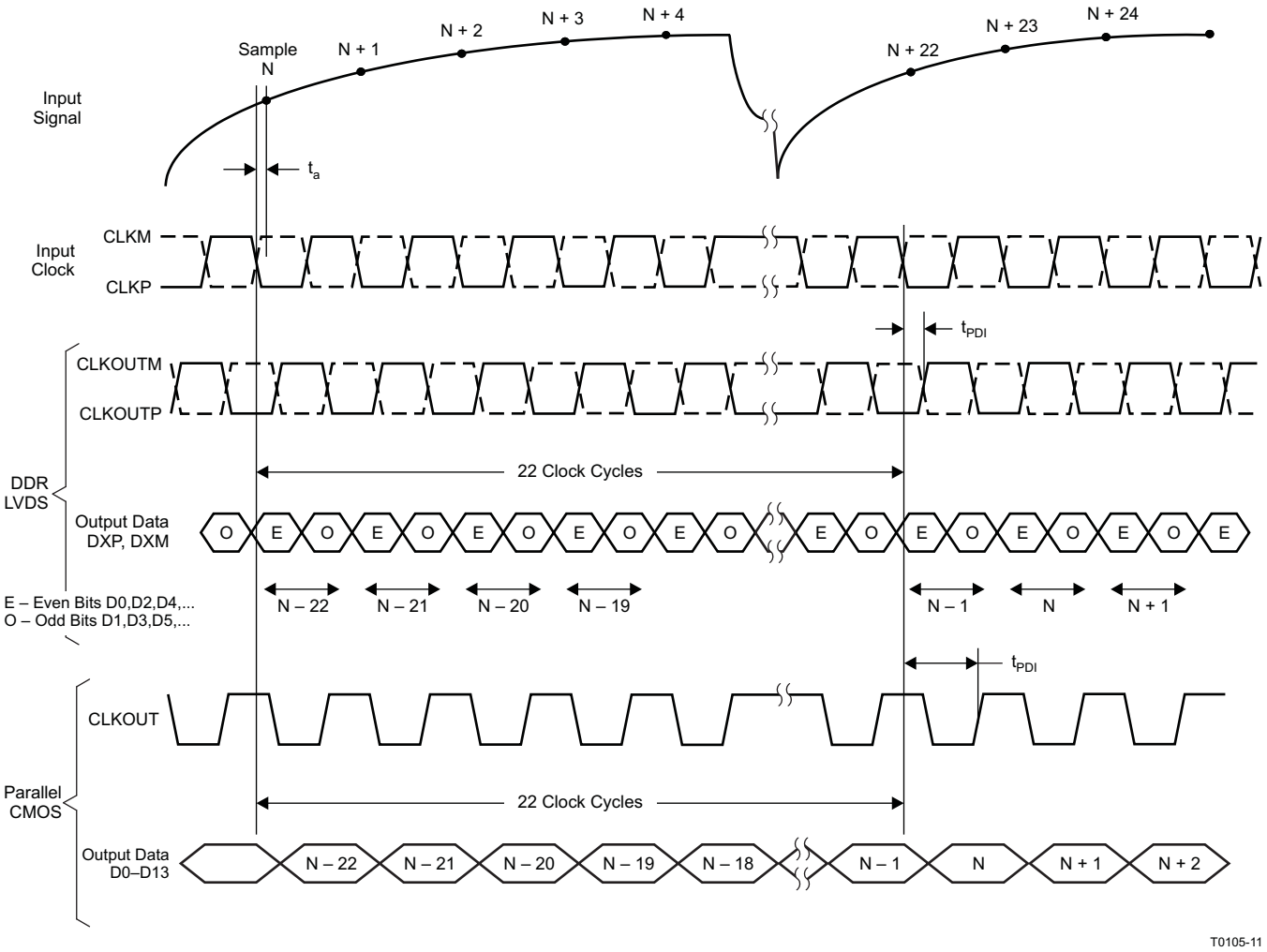
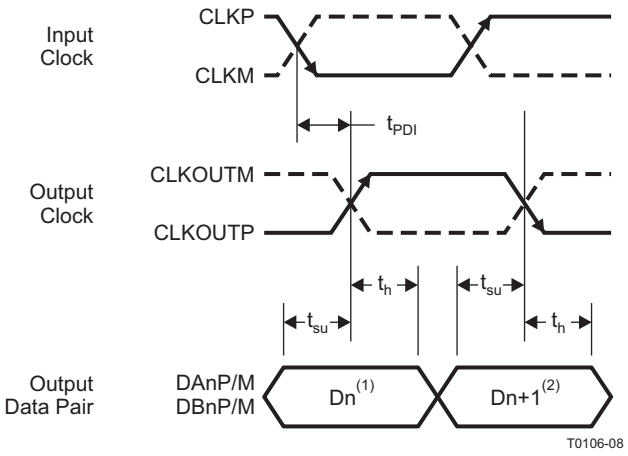


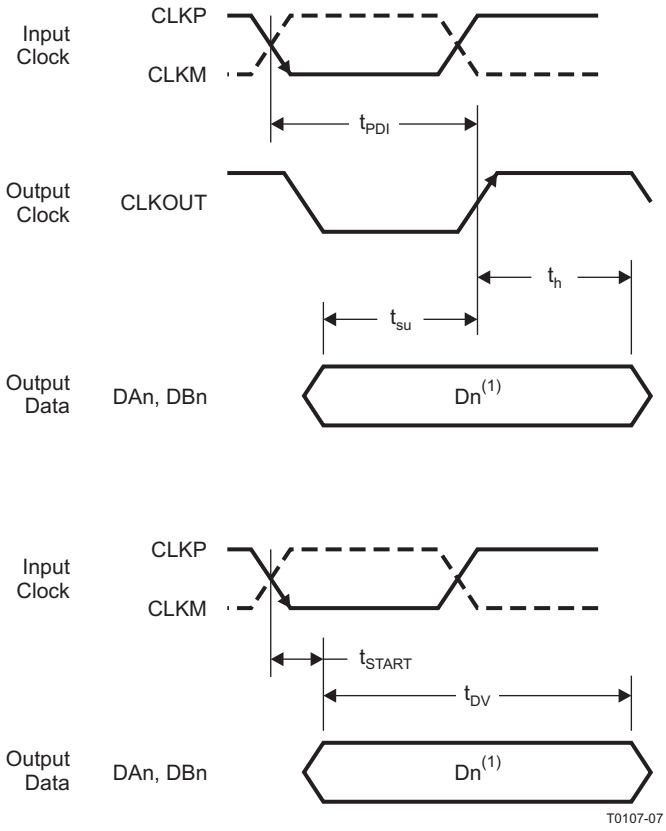
Figure 5. Latency Diagram



(1) Dn - Bits D0, D2, D4, ...

(2) Dn + 1 - Bits D1, D3, D5, ...

Figure 6. LVDS Interface Timing



(1) Dn - Bits D0, D1, D2, ... of Channel A and B

Figure 7. CMOS Interface Timing

DEVICE CONFIGURATION

ADS62Px9/x8 can be configured independently using either parallel interface control or serial interface programming.

PARALLEL CONFIGURATION ONLY

To put the device in parallel configuration mode, keep RESET tied to ***high*** (AVDD or DRVDD).

Now, pins SEN, SCLK, CTRL1, CTRL2 and CTRL3 can be used to directly control certain modes of the ADC. The device can be easily configured by connecting the parallel pins to the correct voltage levels (as described in Table 4 to Table 7). There is no need to apply reset and SDATA pin can be connected to ground.

In this mode, SEN and SCLK function as parallel interface control pins. Frequently used functions can be controlled in this mode – power down modes, internal/external reference, selection between LVDS/CMOS interface and output data format.

Table 4 has a brief description of the modes controlled by the four parallel pins.

Table 4. Parallel Pin Definition

PIN	TYPE OF PIN	CONTROLS MODES
SCLK	Analog control pins (controlled by analog voltage levels, see Figure 8)	Internal/external reference
SEN		LVDS/CMOS interface and output data format
CTRL1	Digital control pins (controlled by digital logic levels)	Controls power down modes
CTRL2		
CTRL3		

SERIAL INTERFACE CONFIGURATION ONLY

To exercise this mode, first the serial registers have to be reset to their default values and RESET pin has to be kept ***low***.

SEN, SDATA and SCLK function as serial interface pins in this mode and can be used to access the internal registers of the ADC.

The registers can be reset either by applying a pulse on RESET pin or by setting the **<RESET>** bit ***high***. The serial interface section describes the register programming and register reset in more detail

DETAILS OF PARALLEL CONFIGURATION ONLY

The functions controlled by each parallel pin are described below. A simple way of configuring the parallel pins is shown in Figure 8.

Table 5. SCLK CONTROL PIN

VOLTAGE APPLIED ON SCLK	DESCRIPTION
0 +200mV/-0mV	Internal reference
(3/8)AVDD +/- 200mV	External reference
(5/8) AVDD +/- 200mV	External reference
AVDD +0mV/-200mV	Internal reference

Table 6. SEN CONTROL PIN

VOLTAGE APPLIED ON SEN	DESCRIPTION
0 (+200mV/–0mV)	2's complement, DDR LVDS output
(3/8)AVDD (±200mV)	Offset binary, DDR LVDS output
(5/8)AVDD (±200mV)	Offset binary, parallel CMOS output
AVDD (+0mV/–200mV)	2's compliment, parallel CMOS output

Table 7. CTRL1, CTRL2 and CTRL3 PINS (1)

CTRL1	CTRL2	CTRL3	DESCRIPTION
LOW	LOW	LOW	Normal operation
LOW	LOW	HIGH	Not available
LOW	HIGH	LOW	Not available
LOW	HIGH	HIGH	Not available
HIGH	LOW	LOW	Global power down
HIGH	LOW	HIGH	Channel B standby
HIGH	HIGH	LOW	Channel A standby
HIGH	HIGH	HIGH	MUX mode of operation, Channel A and B data is multiplexed and output on ***DA13 to DA0*** pins.(2)

(1) See POWER DOWN in the APPLICATION INFORMATION section.
(2) Low Speed mode has to be enabled for Multiplexed Output mode (MUX mode). Therefore, MUX mode works with serial interface configuration only and is not supported with parallel configuration.

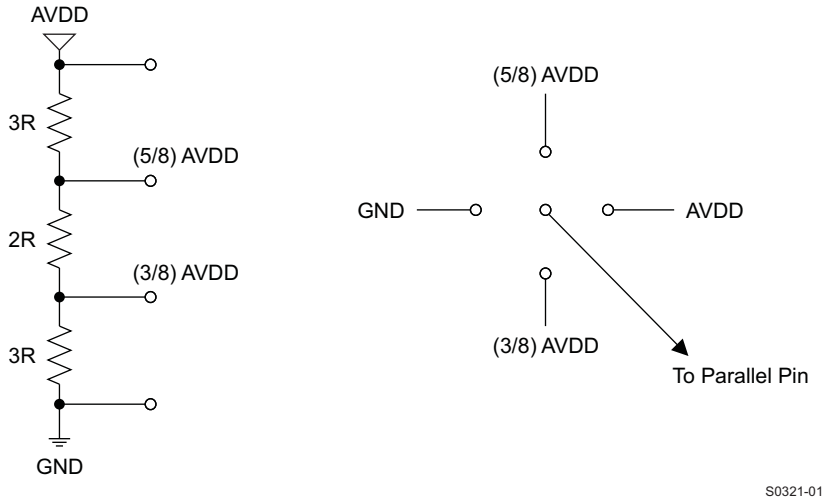


Figure 8. Simple Scheme to Configure Parallel Pins

USING BOTH SERIAL INTERFACE AND PARALLEL CONTROLS

For increased flexibility, a combination of serial interface registers and parallel pin controls (CTRL1 to CTRL3) can also be used to configure the device. To allow this, keep RESET low. The parallel interface control pins CTRL1 to CTRL3 are available. After power-up, the device is automatically configured as per the voltage settings on these pins (see Table 6). SEN, SDATA, and SCLK function as serial interface digital pins and are used to access the internal registers of ADC. The registers must first be reset to their default values either by applying a pulse on RESET pin or by setting bit <RST> = 1. After reset, the RESET pin must be kept low. The Serial Interface section describes register programming and register reset in more detail.

SERIAL INTERFACE

The ADC has a set of internal registers, which can be accessed by the serial interface formed by pins SEN (Serial interface Enable), SCLK (Serial Interface Clock) and SDATA (Serial Interface Data).

Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA is latched at every falling edge of SCLK when SEN is active (low). The serial data is loaded into the register at every 16th SCLK falling edge when SEN is low. In case the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiple of 16-bit words within a single active SEN pulse.

The first 8 bits form the register address and the remaining 8 bits are the register data. The interface can work with SCLK frequency from 20 MHz down to very low speeds (few Hertz) and also with non-50% SCLK duty cycle.

Register Initialization

After power-up, the internal registers MUST be initialized to their default values. This can be done in one of two ways:

1. Either through hardware reset by applying a high-going pulse on RESET pin (of width greater than 10ns) as shown in Figure 9

   OR

2. By applying software reset. Using the serial interface, set the **<RESET>** bit (D7 in register 0x00) to HIGH. This initializes internal registers to their default values and then self-resets the **<RESET>** bit to ***low***. In this case the RESET pin is kept ***low***.

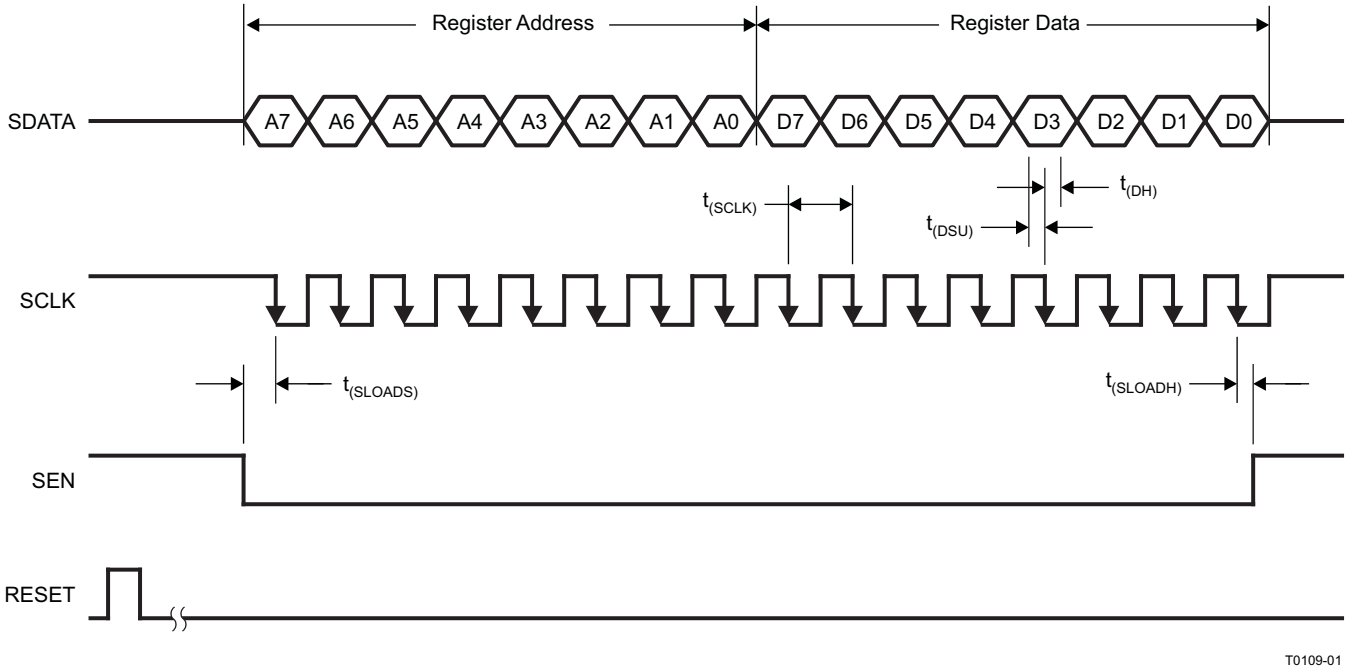


Figure 9. Serial Interface Timing

SERIAL INTERFACE TIMING CHARACTERISTICS

Typical values at 25°C, min and max values across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 3.3V, DRVDD = 1.8V (unless otherwise noted).

PARAMETER		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (= 1/ t_{SCLK})	> DC		20	MHz
t_{SLOADS}	SEN to SCLK setup time	25			ns
t_{SLOADH}	SCLK to SEN hold time	25			ns
t_{DS}	SDATA setup time	25			ns
t_{DH}	SDATA hold time	25			ns

Serial Register Readout

The device includes an option where the contents of the internal registers can be read back. This may be useful as a diagnostic check to verify the serial interface communication between the external controller AND the ADC.

a. First, set register bit <SERIAL READOUT> = 1. This also disables any further writes into the registers.
b. Initiate a serial interface cycle specifying the address of the register (A7-A0) whose content has to be read.
c. The device outputs the contents (D7-D0) of the selected register on the SDOUT pin (64).
d. The external controller can latch the contents at the falling edge of SCLK.
e. To enable register writes, reset register bit <SERIAL READOUT> = 0. SDOUT is a CMOS output pin; the readout functionality is available whether the ADC output data interface is LVDS or CMOS.

When <SERIAL READOUT> is disabled, the SDOUT pin is forced low by the device (and not put in high-impedance). If serial readout is not used, the SDOUT pin has to be floated.

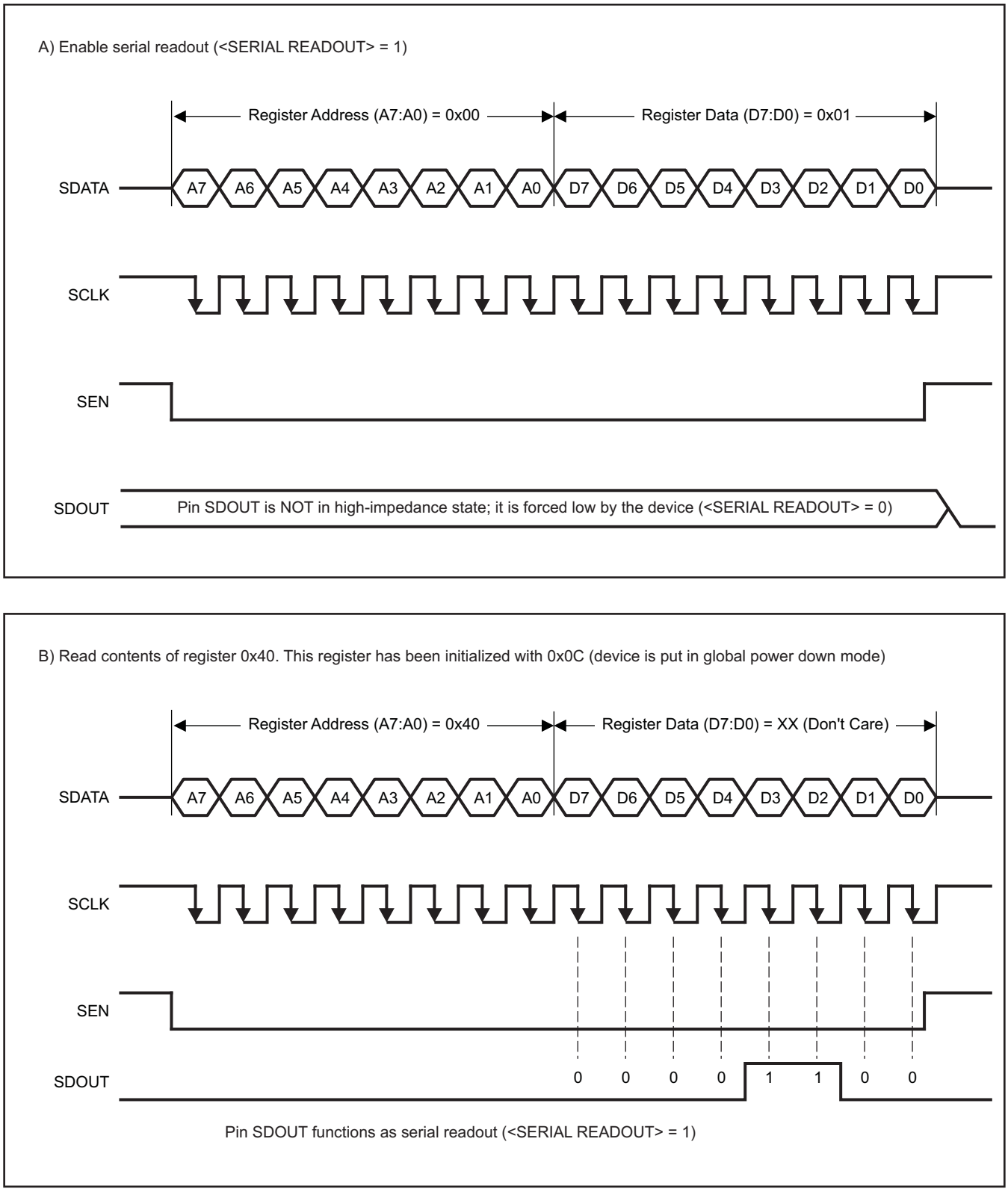


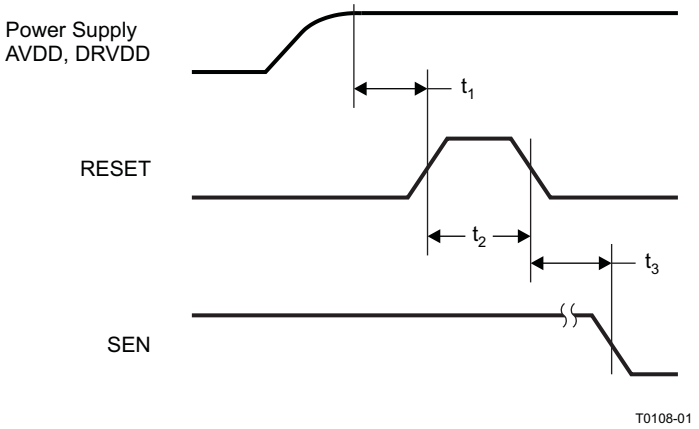
Figure 10. Serial Readout

RESET TIMING (ONLY WHEN SERIAL INTERFACE IS USED)

Typical values at 25°C, min and max values across the full temperature range T_{MIN} = –40°C to T_{MAX} = 85°C (unless otherwise noted).

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Power-on delay	Delay from power-up of AVDD and DRVDD to RESET pulse active	1			ms
t_2	Reset pulse width	Pulse width of active RESET signal	10			ns
					1 (1)	µs
t_3	Register write delay	Delay from RESET disable to SEN active	100			ns

(1) The reset pulse is needed only when using the serial interface configuration. If the pulse width is greater than 1µsec, the device could enter the parallel configuration mode briefly and then return back to serial interface mode.



NOTE: A high-going pulse on RESET pin is required in serial interface mode in case of initialization through hardware reset. For parallel interface operation, RESET has to be tied permanently HIGH.

Figure 11. Reset Timing Diagram

SERIAL REGISTER MAP

Table 8. Summary of Functions Supported by Serial Interface (1)

REGISTER ADDRESS	REGISTER FUNCTIONS							
A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
00	**<RESET>** *Software Reset*	0	0	0	0	0	0	**<SERIAL READOUT>**
20	0	0	0	0	0	**<ENABLE LOW SPEED MODE>**	0	0
3F	0	**<REF>** *Internal or external reference*	0	0	0	0	**<STANDBY>**	0
40	0	0	0	0	**<POWER DOWN MODES>**			
41	**<LVDS CMOS>** *Output interface*	0	0	0	0	0	0	0
44	**<CLKOUT EDGE CONTROL>**						0	0
50	0	**<ENABLE INDIVIDUAL CHANNEL CONTROL>**	0	0	0	**<DATA FORMAT>** *2s comp or offset binary*		0
51	**<CUSTOM PATTERN LOW>**							
52	0	0	**<CUSTOM PATTERN HIGH>**					
53	0	**<ENABLE OFFSET CORRECTION – CH A>**	0					
55	**<GAIN PROGRAMMABILITY – CH A>** *0 to 6 dB in 0.5 dB steps*				**<OFFSET CORRECTION TIME CONSTANT – CH A>**			
57	0	**<FINE GAIN ADJUST – CH A>** *+0.001 dB to +0.134 dB, in 128 steps*						
62	0	0	0	0	0	**<TEST PATTERNS – CH A>**		
63	0	0	**<OFFSET PEDESTAL – CH A>**					
66	0	**<ENABLE OFFSET CORRECTION – CH B>**	0	0	0	0	0	0
68	**<GAIN PROGRAMMABILITY – CH B>** *0 to 6 dB in 0.5 dB steps*				**<OFFSET CORRECTION TIME CONSTANT – CH B>**			
6A	0	**<FINE GAIN ADJUST – CH B>** *+0.001 dB to +0.134 dB, in 128 steps*						
75	0	0	0	0	0	**<TEST PATTERNS – CH B>**		
76	0	0	**<OFFSET PEDESTAL – CH B>**					

(1) Multiple functions in a register can be programmed in a single write operation.

DESCRIPTION OF SERIAL REGISTERS

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
00	**<RESET>** *Software Reset*	0	0	0	0	0		**<SERIAL READOUT>**

D7 <RESET>

1 Software reset applied – resets all internal registers and self-clears to 0.

D0 <SERIAL READOUT>

0 Serial readout disabled. SDOUT is forced low by the device (and not put in high impedance state).

1 Serial readout enabled, Pin SDOUT functions as serial data readout.

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
20	0	0	0	0	0	**<ENABLE LOW SPEED MODE>**	0	0

D2 <ENABLE LOW SPEED MODE>

0 LOW SPEED mode disabled. Use for sampling frequency > 80 MSPS

1 Enable LOW SPEED mode for sampling frequencies ≤ 80 MSPS.

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
3F	0	**<REF>**		0	0	0	**<STANDBY>**	0

D6-D5 <REF> Internal or external reference selection

00 Internal reference enabled
01
10

11 External reference enabled

D1 <STANDBY>

0 Normal operation

1 Both ADC channels are put in standby. Internal references, output buffers are active. This results in quick wake-up time from standby.

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
40	0	0	0	0	**POWER DOWN MODES**			

D3-D0 <POWER DOWN MODES>

0000 Pins CTRL1, CTRL2, and CTRL3 determine power down modes.

1000 Normal operation

1001 Output buffer disabled for channel B

1010 Output buffer disabled for channel A

1011 Output buffer disabled for channel A and B

1100 Global power down

1101 Channel B standby

1110 Channel A standby

1111 Multiplexed mode, **MUX-** (only with CMOS interface)
Channel A and B data is multiplexed and output on ***DA13 to DA0*** pins. Refer to the Multiplexed Output Mode section in the APPLICATION INFORMATION for additional information.

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
41	<LVDS CMOS>	0	0	0	0	0	0	0

D7 <LVDS CMOS>

0 Parallel CMOS interface

1 DDR LVDS interface

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
44	<CLKOUT EDGE CONTROL> *Output clock edge control*						0	0

LVDS interface

D7-D5 <CLKOUT POSN> Output clock rising edge position (2)

000, 100 Default output clock position (refer to timing specification table)

101 Falling edge shifted (delayed) by + (4/26)×Ts(1)

110 Falling edge shifted (advanced) by – (7/26)×Ts

111 Falling edge shifted (advanced) by – (4/26)×Ts

D4-D2 <CLKOUT POSN> Output clock falling edge position (2)

000, 100 Default output clock position (refer to timing specification table)

101 Rising edge shifted (delayed) by + (4/26)×Ts

110 Rising edge shifted (advanced) by – (7/26)×Ts

111 Rising edge shifted (advanced) by – (4/26)×Ts

CMOS interface

D7-D5 <CLKOUT POSN> Output clock rising edge position (2)

000, 100 Default output clock position (refer to timing specification table)

101 Rising edge shifted (delayed) by + (4/26)×Ts

110 Rising edge shifted (advanced) by – (7/26)×Ts

111 Rising edge shifted (advanced) by – (4/26)×Ts

D4-D2 <CLKOUT POSN> Output clock falling edge position (2)

000, 100 Default output clock position (refer to timing specification table)

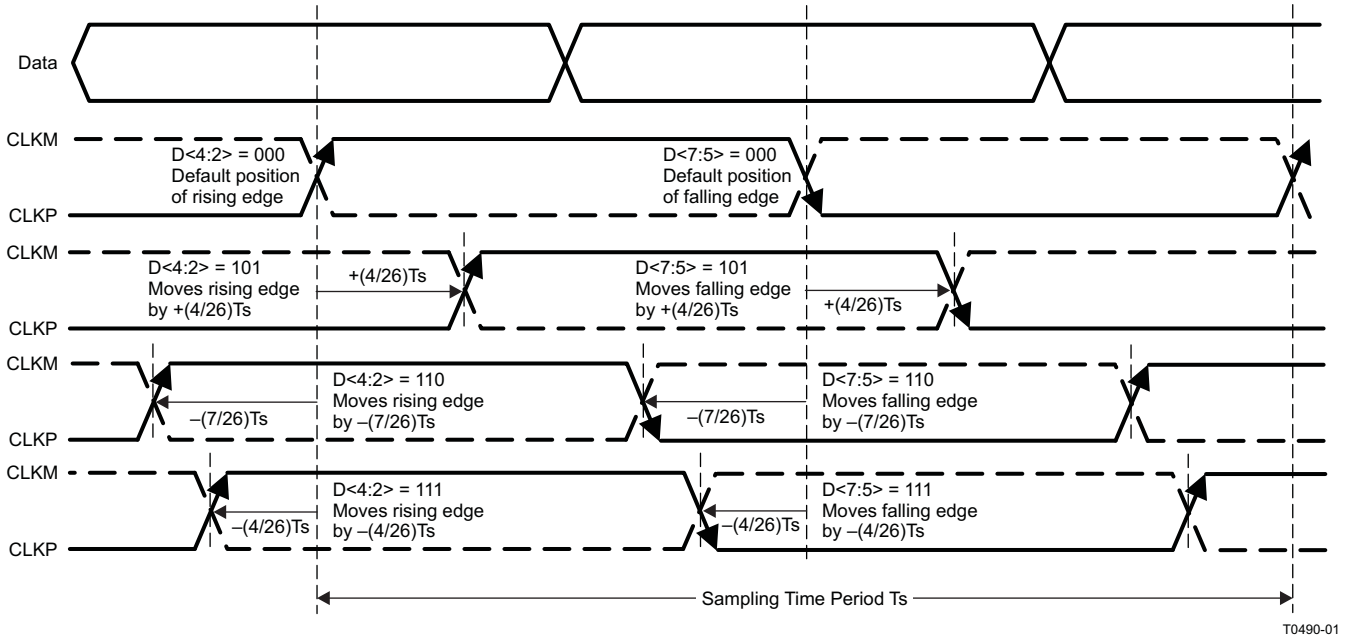
101 Falling edge shifted (delayed) by + (4/26)×Ts

110 Falling edge shifted (advanced) by – (7/26)×Ts

111 Falling edge shifted (advanced) by – (4/26)×Ts

(1) Ts = 1 / sampling frequency

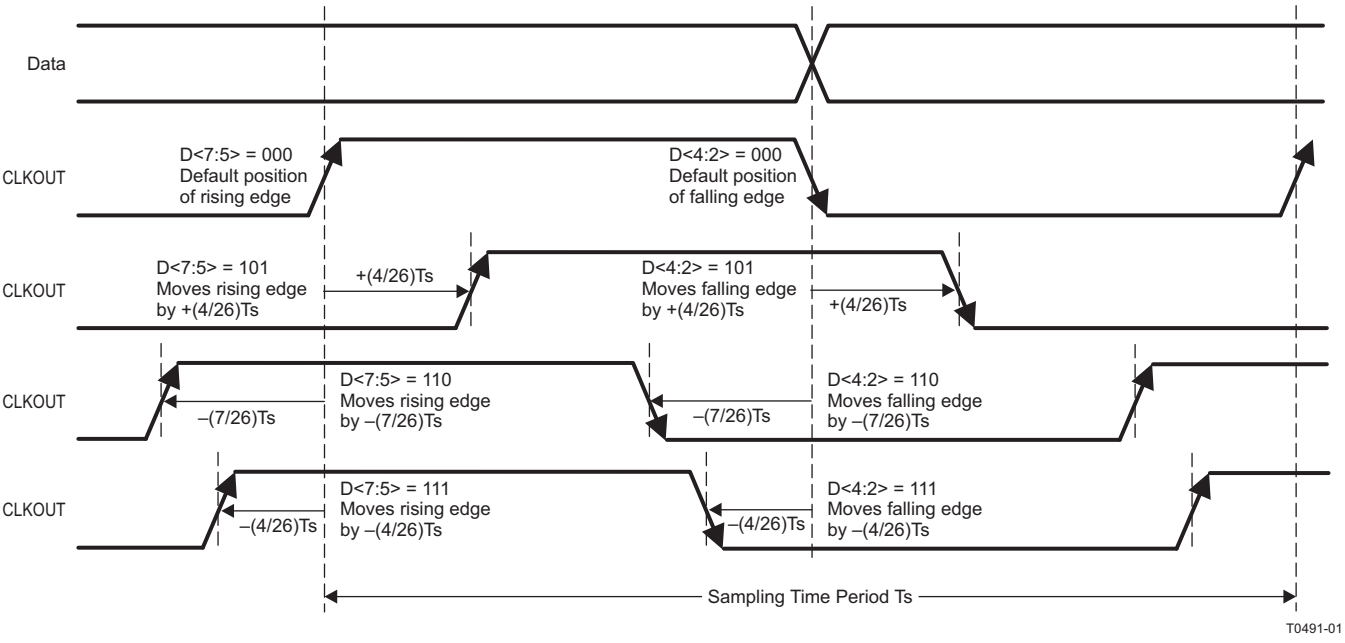
(2) Keep the same duty cycle, move both edges by the same amount (i.e., write both D<4:2> and D<7:5> to be the same value).



NOTES: 1. Keep the same duty cycle, move both edges by same amount (i.e. write both D<4:2> and D<7:5> to be the same value).

2. Refer to timing specification table for default output clock position.

Figure 12. LVDS Interface Output Clock Edge Movement (Serial Register 0x44)



NOTES: 1. Keep the same duty cycle, move both edges by same amount (i.e. write both D<4:2> and D<7:5> to be the same value).

2. Refer to timing specification table for default output clock position.

Figure 13. CMOS Interface Output Clock Edge Movement (Serial Register 0x44)

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
50	0	**<ENABLE INDEPENDENT CHANNEL CONTROL>**	0	0	0	**<DATA FORMAT>** *2s complement or offset binary*		0

D6 <ENABLE INDEPENDENT CHANNEL CONTROL>

0 ***Common control –*** both channels use common control settings for test patterns, offset correction, fine gain, gain correction and SNR Boost functions. These settings can be specified in a single set of registers.

1 ***Independent control –*** both channels can be programmed with independent control settings for test patterns, offset correction and SNR Boost functions. Separate registers are available for each channel.

D2-D1 <DATA FORMAT>

10 2s complement

11 Offset binary

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
51	**<Custom Pattern Low>**							
52	0	0	**<Custom Pattern High>**					

D7-D0 <CUSTOM PATTERN LOW>

8 lower bits of custom pattern available at the output instead of ADC data.

D5-D0 <CUSTOM PATTERN HIGH>

6 upper bits of custom pattern available at the output instead of ADC data

Use this mode along with “Test Patterns” (register 0x62).

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
53	0	**<ENABLE OFFSET CORRECTION – Common/Ch A>** *Offset correction enable*	0	0	0	0	0	0

D6 <ENABLE OFFSET CORRECTION – Common/Ch A>

Offset correction enable control for both channels (*with common control*) or for channel A only (*with independent control*).

0 Offset correction disabled

1 Offset correction enabled

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
55	<GAIN – Common/Ch A>				<OFFSET CORR TIME CONSTANT – Common/Ch A> *Offset correction time constant*			

D7-D4 <GAIN – Common/Ch A>

Gain control for both channels (with common control) or for channel A only (with independent control).

0000 0 dB gain, default after reset
0001 0.5 dB gain
0010 1.0 dB gain
0011 1.5 dB gain
0100 2.0 dB gain
0101 2.5 dB gain
0110 3.0 dB gain
0111 3.5 dB gain
1000 4.0 dB gain
1001 4.5 dB gain
1010 5.0 dB gain
1011 5.5 dB gain
1100 6.0 dB gain

D3-D0 <OFFSET CORR TIME CONSTANT – Common/Ch A>

Correction loop time constant in number of clock cycles.
Applies to both channels (with common control) or for channel A only (with independent control).

0000 256 k
0001 512 k
0010 1 M
0011 2 M
0100 4 M
0101 8 M
0110 16 M
0111 32 M
1000 64 M
1001 128 M
1010 256 M
1011 512 M

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
57	0	**<FINE GAIN ADJUST – Common/Ch A>** *+0.001 dB to +0.134 dB, in 128 steps*						

Using the FINE GAIN ADJUST register bits, the channel gain can be trimmed in fine steps. The trim is only additive, has 128 steps and a range of 0.134dB. The relation between the FINE GAIN ADJUST bits and the trimmed channel gain is:

$$\Delta \text{ Channel gain} = 20*\log10[1 + (\text{FINE GAIN ADJUST}/8192)]$$

Note that the total device gain = ADC gain + Δ Channel gain. The ADC gain is determined by register bits <GAIN PROGRAMMABILITY>

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
62	0	0	0	0	0	**<TEST PATTERNS>**		

D2-D0 **<TEST PATTERNS>** Test Patterns to verify data capture.

Applies to both channels (*with common control*) or for channel A only (*with independent control*).

000 Normal operation

001 Outputs all zeros

010 Outputs all ones

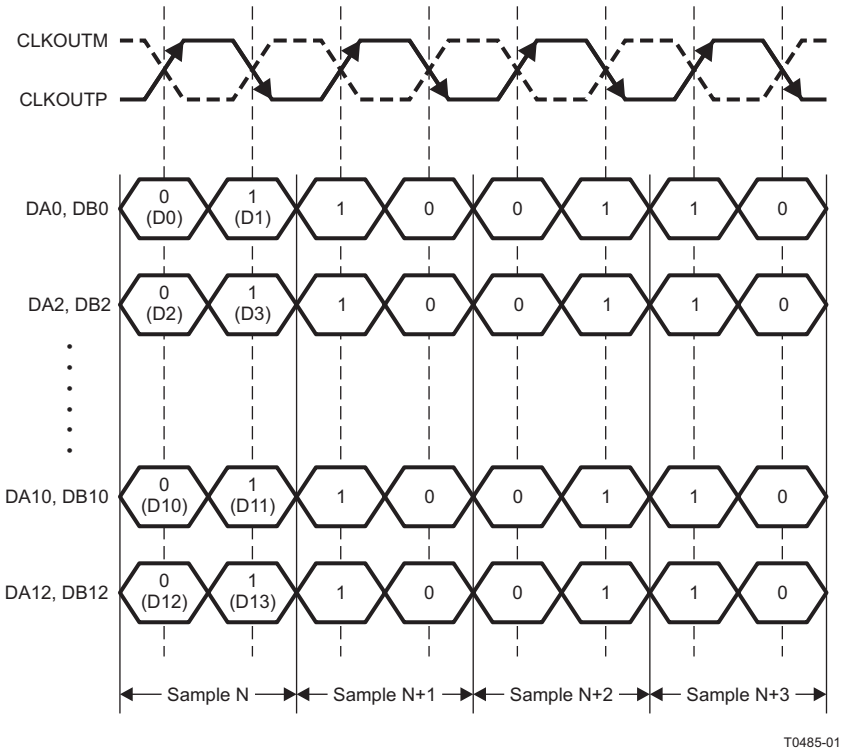
011 Outputs toggle pattern – see Figure 14 and Figure 15 for test pattern timing diagrams for LVDS and CMOS modes.
In ADS62P49/48, output data <D13:D0> alternates between 01010101010101 and 10101010101010 every clock cycle.
In ADS62P29/28, output data <D11:D0> alternates between 010101010101 and 101010101010 every clock cycle.

100 Outputs digital ramp
In ADS62P49/48, output data increments by one LSB (14-bit) every clock cycle from code 0 to code 16383
In ADS62P29/28, output data increments by one LSB (12-bit) every 4th clock cycle from code 0 to code 4095

101 Outputs custom pattern (use registers 0x51, 0x52 for setting the custom pattern), see Figure 16 for an example of a custom pattern.

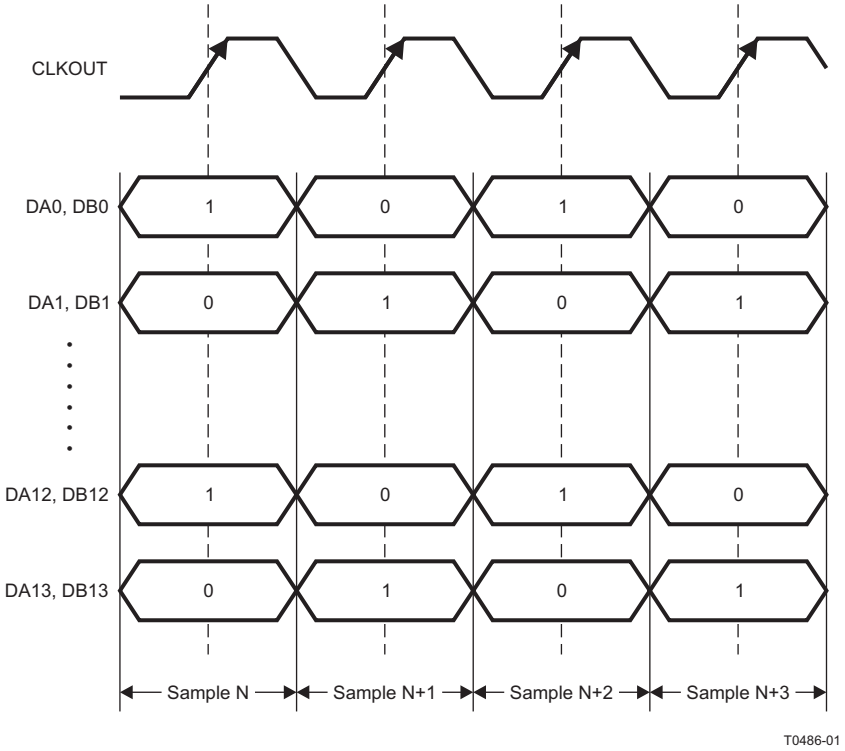
110 Unused

111 Unused



NOTES: 1. Even bits output at the rising edge of CLKOUTP, and odd bits output at falling edge of CLKOUTP.
2. Output toggles at half the sampling rate (Fs/2) in this test mode.

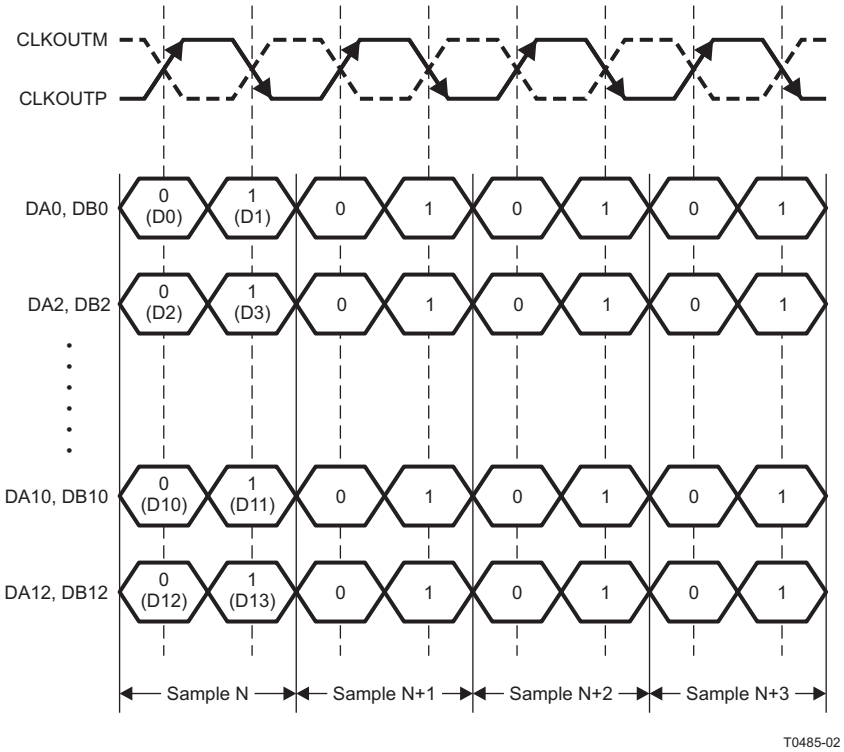
Figure 14. Output Toggle Pattern (Serial Register 0x62, D<2:0> = 011) in LVDS Mode



NOTE: Output toggles at half the sampling rate (Fs/2) in this test mode.

Figure 15. Output Toggle Pattern (Serial Register 0x62, D<2:0> = 011) in CMOS Mode

Example: Register 0x51 = 0xAA and Register 0x52 = 0x2A to toggle output at Fs



NOTES: 1. Even bits output at the rising edge of CLKOUTP, and odd bits output at falling edge of CLKOUTP.

2. Output toggles at the sampling rate (Fs) in this test mode.

Figure 16. Output Custom Pattern (Serial Register 0x62, D<2:0> = 101) in LVDS Mode

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
63	0	0	<OFFSET PEDESTAL – Common/Ch A>					

D5-D0 <OFFSET PEDESTAL – Common/Ch A>

When the offset correction is enabled, the final converged value (after the offset is corrected) will be the ideal ADC mid-code value (=8192 for P49/48, = 2048 for P29/28). A pedestal can be added to the final converged value by programming these bits. So, the final converged value will be = ideal mid-code + PEDESTAL.
See "Offset Correction" in application section.

Applies to both channels (*with common control*) or for channel A only (*with independent control*).

011111 PEDESTAL = 31 LSB

011110 PEDESTAL = 30 LSB

011101 PEDESTAL = 29 LSB

….

000000 PEDESTAL = 0

….

111111 PEDESTAL = –1 LSB

111110 PEDESTAL = –2 LSB

….

100000 PEDESTAL = –32 LSB

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
66	0	**<ENABLE OFFSET CORRECTION – CH B>** *Offset correction enable*	0	0	0	0	0	0

D6 <ENABLE OFFSET CORRECTION – CH B>

Offset correction enable control for channel B (only with independent control).

0 offset correction disabled

1 offset correction enabled

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
68	<GAIN – CH B>				<OFFSET CORR TIME CONSTANT – CH B> *Offset correction time constant*			

D7-D4 **<GAIN – CH B>** Gain programmability to 0.5 dB steps.

Applies to channel B (*only with independent control*).

0000 0 dB gain, default after reset
0001 0.5 dB gain
0010 1.0 dB gain
0011 1.5 dB gain
0100 2.0 dB gain
0101 2.5 dB gain
0110 3.0 dB gain
0111 3.5 dB gain
1000 4.0 dB gain
1001 4.5 dB gain
1010 5.0 dB gain
1011 5.5 dB gain
1100 6.0 dB gain

D3-D0 **OFFSET CORR TIME CONSTANT – CH B>** Time constant of correction loop in number of clock cycles.

Applies to channel B (*only with independent control*)

0000 256 k
0001 512 k
0010 1 M
0011 2 M
0100 4 M
0101 8 M
0110 16 M
0111 32 M
1000 64 M
1001 128 M
1010 256 M
1011 512 M

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
6A		**<FINE GAIN ADJUST – CH B>** *+0.001 dB to +0.134 dB, in 128 steps*						

Using the FINE GAIN ADJUST register bits, the channel gain can be trimmed in fine steps. The trim is only additive, has 128 steps and a range of 0.134dB. The relation between the FINE GAIN ADJUST bits and the trimmed channel gain is:

$$\Delta \text{ Channel gain} = 20*\log10[1 + (\text{FINE GAIN ADJUST}/8192)]$$

Note that the total device gain = ADC gain + Δ Channel gain. The ADC gain is determined by register bits <GAIN PROGRAMMABILITY>

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
75			0	0	0	**<TEST PATTERNS – CH B>**		

D2-D0 **<TEST PATTERNS>** Test Patterns to verify data capture.

Applies to channel B (only with independent control)

000 Normal operation

001 Outputs all zeros

010 Outputs all ones

011 Outputs toggle pattern – see Figure 14 and Figure 15 for LVDS and CMOS modes.
In ADS62P49/48, output data <D13:D0> alternates between 01010101010101 and 10101010101010 every clock cycle.
In ADS62P29/28, output data <D11:D0> alternates between 010101010101 and 101010101010 every clock cycle.

100 Outputs digital ramp
In ADS62P49/48, output data increments by one LSB (14-bit) every clock cycle from code 0 to code 16383
In ADS62P29/28, output data increments by one LSB (12-bit) every 4th clock cycle from code 0 to code 4095

101 Outputs custom pattern (use registers 0x51, 0x52 for setting the custom pattern), see Figure 16 for an example of a custom pattern.

110 Unused

111 Unused

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
76	0	0	<OFFSET PEDESTAL – Common/CH B>					

D5-D0 **<OFFSET PEDESTAL – Common/CH B>**

When the offset correction is enabled, the final converged value (after the offset is corrected) will be the ideal ADC mid-code value (=8192 for P49/48, = 2048 for P29/28). A pedestal can be added to the final converged value by programming these bits. So, the final converged value will be = ideal mid-code + PEDESTAL. See "Offset Correction" in application section.

Applies to channel B (*only with independent control*).

011111 PEDESTAL = 31 LSB

011110 PEDESTAL = 30 LSB

011101 PEDESTAL = 29 LSB

….

000000 PEDESTAL = 0

….

111111 PEDESTAL = –1 LSB

111110 PEDESTAL = –2 LSB

….

100000 PEDESTAL = –32 LSB

DEVICE INFORMATION

PIN CONFIGURATION (LVDS MODE) – ADS62P49/P48

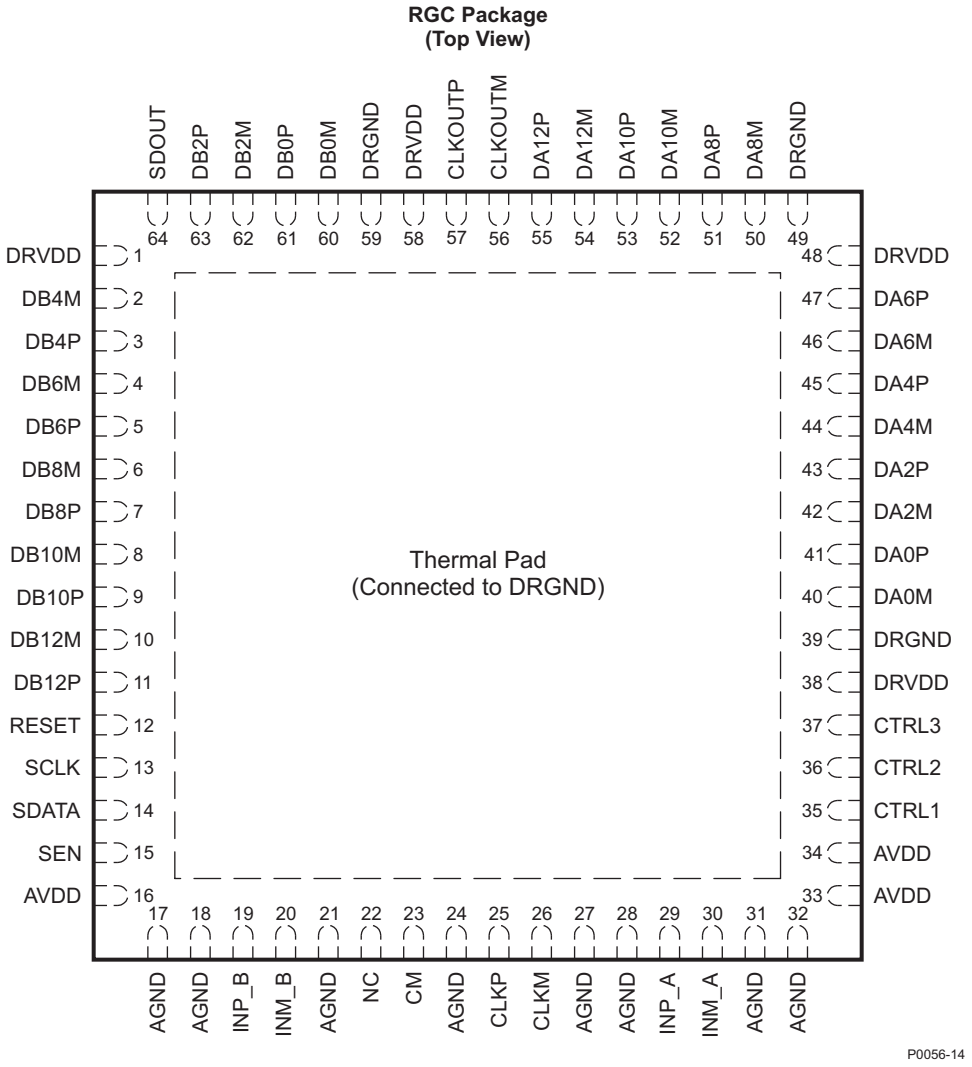


Figure 17.

PIN CONFIGURATION (LVDS MODE) – ADS62P29/P28

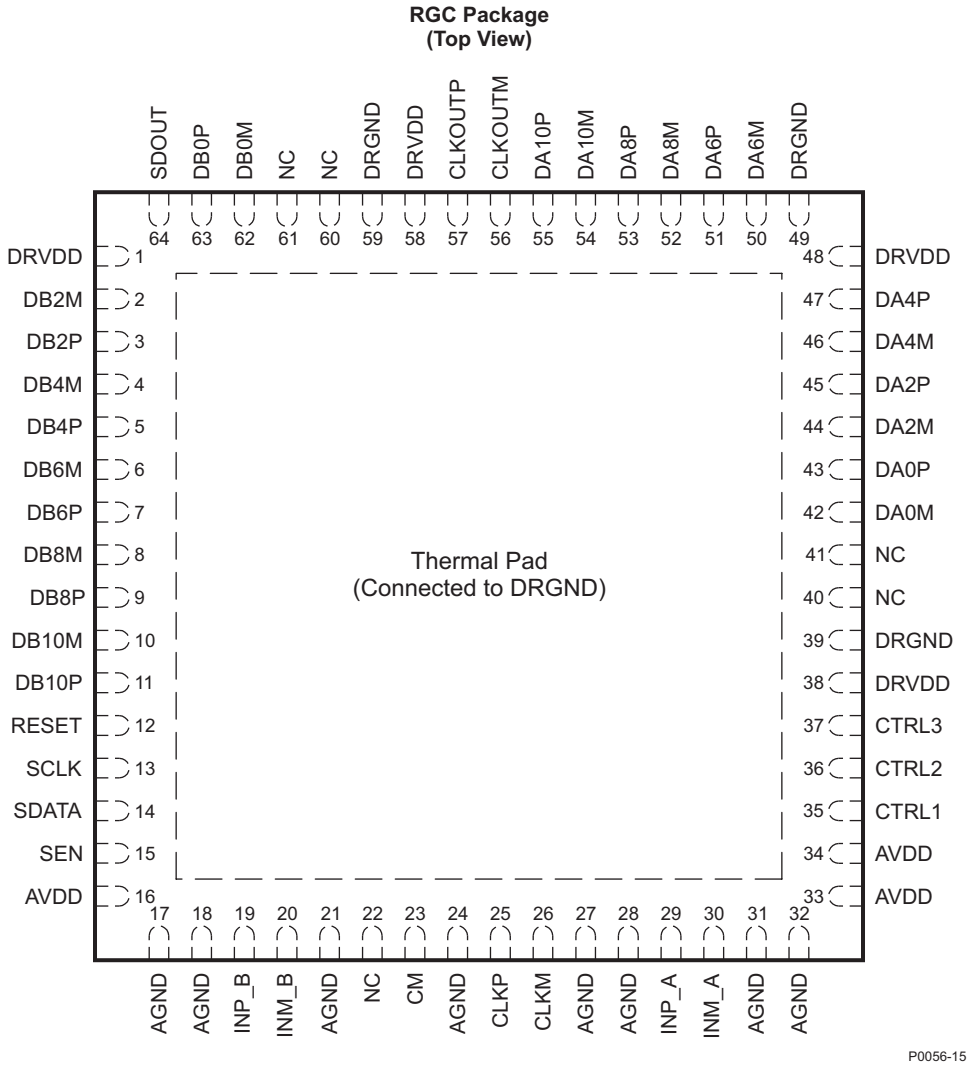


Figure 18.

PIN ASSIGNMENTS (LVDS MODE) – ADS62P49/P48 and ADS62P29/P28

PIN		NO. OF PINS	I/O	DESCRIPTION
NAME	NO.			
AVDD	16, 33, 34	3	I	Analog power supply
AGND	17, 18, 21, 24, 27, 28, 31, 32	8	I	Analog ground
CLKP, CLKM	25, 26	2	I	Differential clock input
INP_A, INM_A	29, 30	2	I	Differential analog input, Channel A
INP_B, INM_B	19, 20	2	I	Differential analog input, Channel B
VCM	23	1	IO	Internal reference mode – Common-mode voltage output. External reference mode – Reference input. The voltage forced on this pin sets the internal references.
RESET	12	1	I	Serial interface RESET input. When using the serial interface mode, the user ***must*** initialize internal registers through hardware RESET by applying a high-going pulse on this pin or by using software reset option. Refer to ***Serial Interface*** section.

PIN ASSIGNMENTS (LVDS MODE) – ADS62P49/P48 and ADS62P29/P28 (continued)

PIN		NO. OF PINS	I/O	DESCRIPTION
NAME	NO.			
				In parallel interface mode, the user has to tie RESET pin permanently ***high***. (SCLK and SEN are used as parallel control pins in this mode) The pin has an internal 100 kΩ pull-down resistor.
SCLK	13	1	I	This pin functions as serial interface clock input when RESET is ***low***. It controls selection of internal or external reference when RESET is tied ***high***. See Table 5 for detailed information. The pin has an internal 100 kΩ pull-down resistor.
SDATA	14	1	I	Serial interface data input. The pin has an internal 100KΩ pull-down resistor. It has no function in parallel interface mode and can be tied to ground.
SEN	15	1	I	This pin functions as serial interface enable input when RESET is ***low***. It controls selection of data format and interface type when RESET is tied high. See Table 6 for detailed information. The pin has an internal 100 kΩ pull-up resistor to AVDD
SDOUT	64	1	O	This pin functions as serial interface register readout, when the <SERIAL READOUT> bit is enabled. When <SERIAL READOUT> = 0, this pin forces logic LOW and is not 3-stated.
CTRL1	35	1	I	Digital control input pins. Together, they control various power down modes. The pin has an internal 100kΩ pull-down resistor.
CTRL2	36	1	I	
CTRL3	37	1	I	
CLKOUTP	57	1	O	Differential output clock, true
CLKOUTM	56	1	O	Differential output clock, complement
DA0P, DA0M	Refer to Figure 17 and Figure 18	2	O	Differential output data pair, D0 and D1 multiplexed – Channel A
DA2P, DA2M		2	O	Differential output data D2 and D3 multiplexed – Channel A
DA4P, DA4M		2	O	Differential output data D4 and D5 multiplexed – Channel A
DA6P, DA6M		2	O	Differential output data D6 and D7 multiplexed – Channel A
DA8P, DA8M		2	O	Differential output data D8 and D9 multiplexed – Channel A
DA10P, DA10M		2	O	Differential output data D10 and D11 multiplexed – Channel A
DA12P, DA12M		2	O	Differential output data D12 and D13 multiplexed – Channel A
DB0P, DB0M		2	O	Differential output data pair, D0 and D1 multiplexed – Channel B
DB2P, DB2M		2	O	Differential output data D2 and D3 multiplexed – Channel B
DB4P, DB4M		2	O	Differential output data D4 and D5 multiplexed – Channel B
DB6P, DB6M		2	O	Differential output data D6 and D7 multiplexed – Channel B
DB8P, DB8M		2	O	Differential output data D8 and D9 multiplexed – Channel B
DB10P, DB10M		2	O	Differential output data D10 and D11 multiplexed – Channel B
DB12P, DB12M		2	O	Differential output data D12 and D13 multiplexed – Channel B
DRVDD	1, 38, 48, 58	4	I	Output buffer supply
DRGND	39, 49, 59, PAD	4	I	Output buffer ground
NC	Refer to Figure 17 and Figure 18			Do not connect

PIN CONFIGURATION (CMOS MODE) – ADS62P49/P48

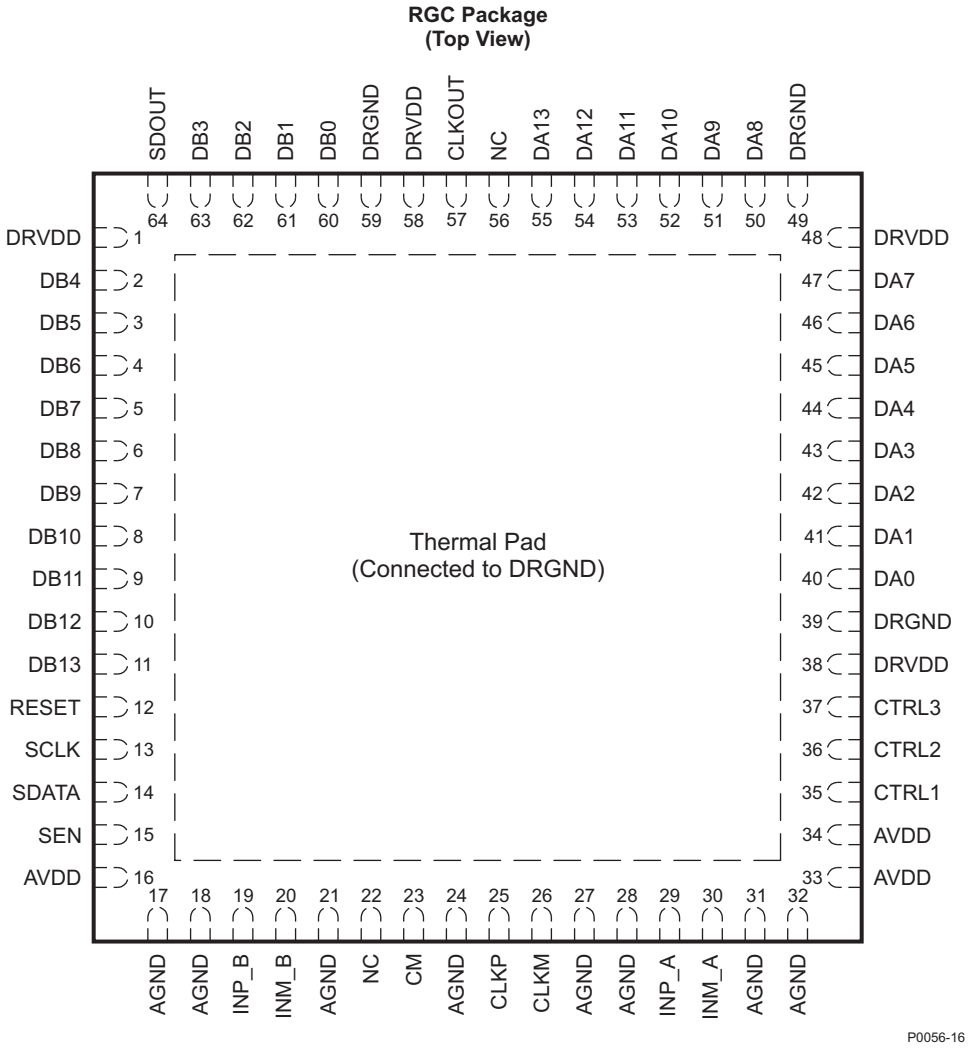


Figure 19.

PIN CONFIGURATION (CMOS MODE) – ADS62P29/P28

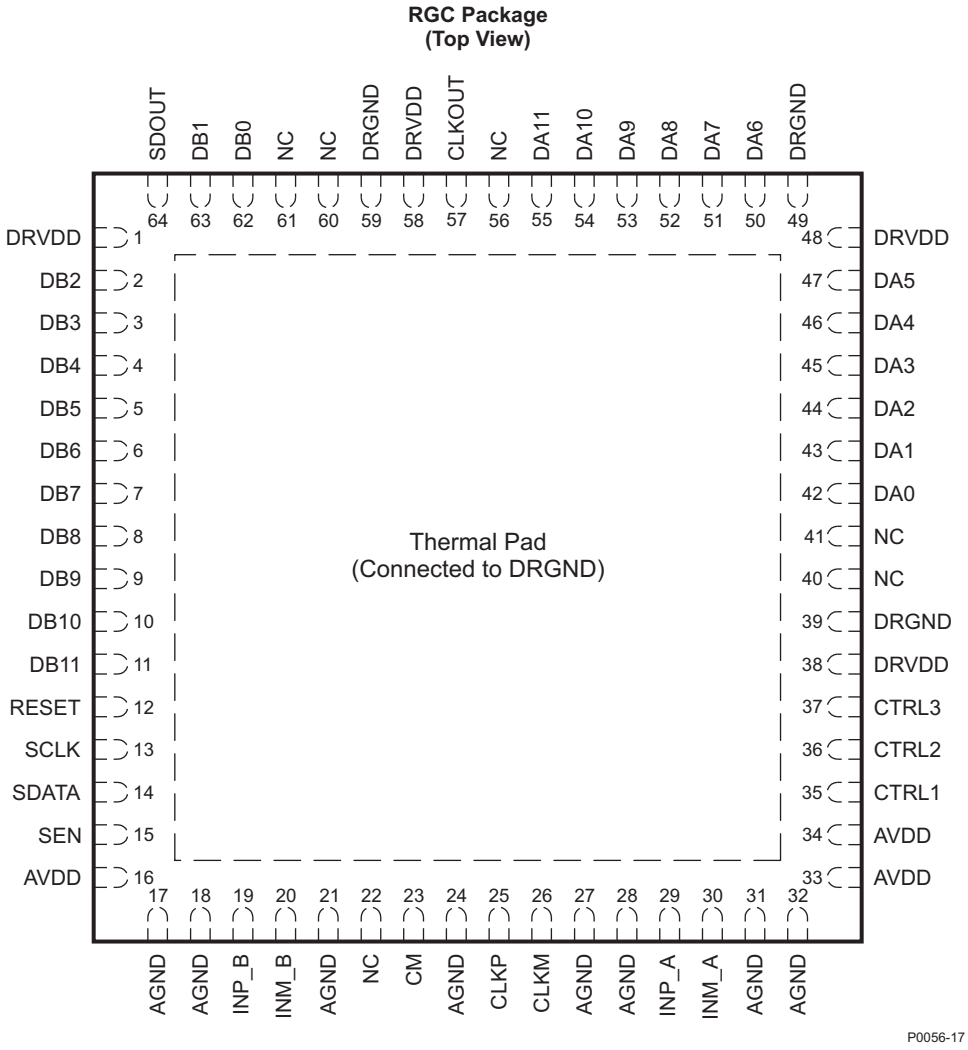


Figure 20.

PIN ASSIGNMENTS (CMOS MODE) – ADS62P49/P48 and ADS62P29/P28

PIN		NO. OF PINS	I/O	DESCRIPTION
NAME	NO.			
AVDD	16, 33, 34	3	I	Analog power supply
AGND	17, 18, 21, 24, 27, 28, 31, 32	8	I	Analog ground
CLKP, CLKM	25, 26	2	I	Differential clock input
INP_A, INM_A	29, 30	2	I	Differential analog input, Channel A
INP_B, INM_B	19, 20	2	I	Differential analog input, Channel B
VCM	23	1	IO	Internal reference mode – Common-mode voltage output. External reference mode – Reference input. The voltage forced on this pin sets the internal references.
RESET	12	1	I	Serial interface RESET input. When using the serial interface mode, the user ***MUST*** initialize internal registers through hardware RESET by applying a high-going pulse on this pin or by using software reset option. Refer to **SERIAL INTERFACE** section.

PIN ASSIGNMENTS (CMOS MODE) – ADS62P49/P48 and ADS62P29/P28 (continued)

PIN		NO. OF PINS	I/O	DESCRIPTION
NAME	NO.			
				In parallel interface mode, the user has to tie RESET pin permanently ***high***. (SCLK and SEN are used as parallel control pins in this mode.) The pin has an internal 100 kΩ pull-down resistor.
SCLK	13	1	I	This pin functions as serial interface clock input when RESET is ***low***. It controls selection of internal or external reference when RESET is tied ***high***. See Table 5 for detailed information. The pin has an internal 100-kΩ pull-down resistor.
SDATA	14	1	I	Serial interface data input. The pin has an internal 100-kΩ pull-down resistor. It has no function in parallel interface mode and can be tied to ground.
SEN	15	1	I	This pin functions as serial interface enable input when RESET is ***low***. It controls selection of data format and interface type when RESET is tied ***high***. See Table 6 for detailed information. The pin has an internal 100 kΩ pull-up resistor to AVDD.
SDOUT	64	1	O	This pin functions as serial interface register readout, when the <SERIAL READOUT> bit is enabled. When <SERIAL READOUT> = 0, this pin forces logic LOW and is not 3-stated.
CTRL1	35	1	I	Digital control input pins. Together, they control various power down modes. The pin has an internal 100 kΩ pull-down resistor.
CTRL2	36	1	I	
CTRL3	37	1	I	
CLKOUT	57	1	O	CMOS output clock
DA0-DA13	Refer to Figure 19 and Figure 20	14	O	Channel A ADC output data bits, CMOS levels
DB0-DB13		14	O	Channel B ADC output data bits, CMOS levels
DRVDD	1, 38, 48, 58	4	I	Output buffer supply
DRGND	39, 49, 59, PAD	4	I	Output buffer ground
NC	Refer to Figure 19 and Figure 20			Do not connect

TYPICAL CHARACTERISTICS – ADS62P49

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, LVDS output interface, 32K point FFT (unless otherwise noted)

FFT FOR 20 MHz INPUT SIGNAL

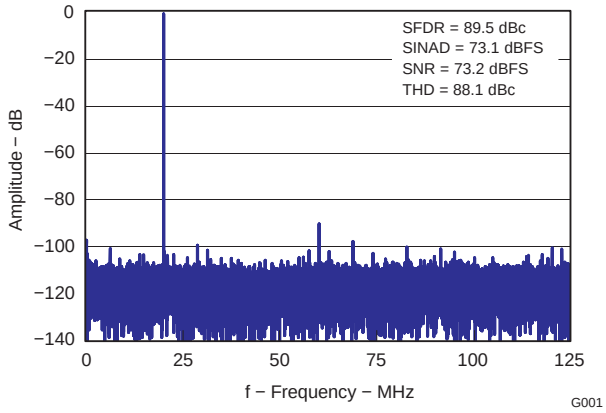


Figure 21.

FFT FOR 170 MHz INPUT SIGNAL

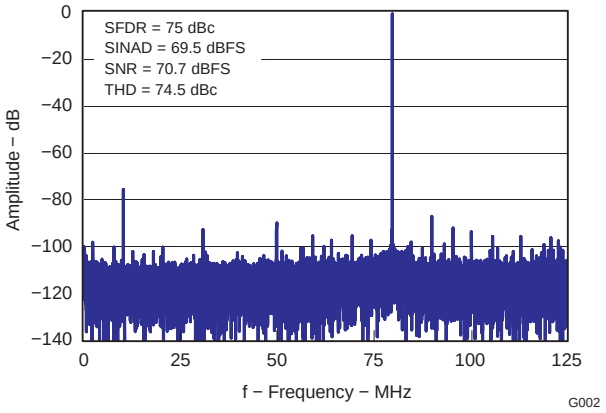


Figure 22.

FFT FOR 300 MHz INPUT SIGNAL

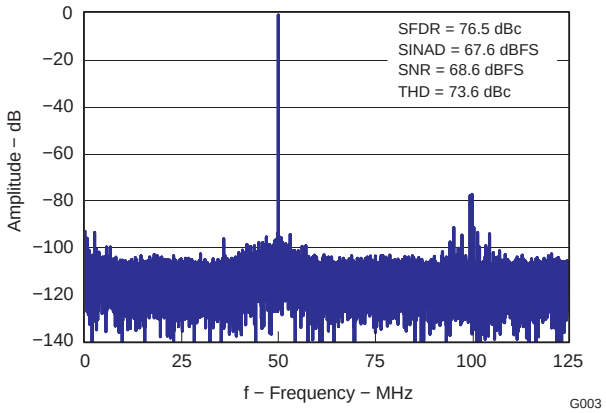


Figure 23.

FFT FOR 2-TONE INPUT SIGNAL

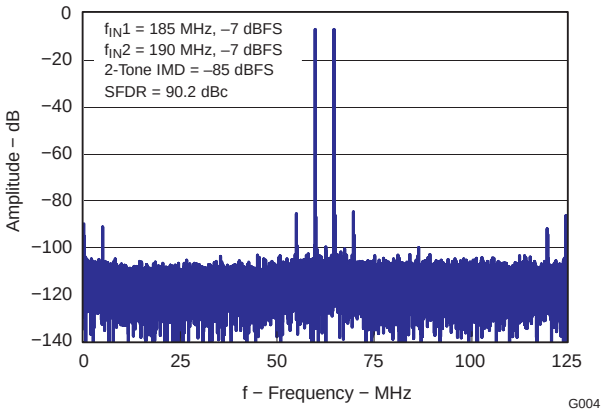


Figure 24.

FFT FOR 2-TONE INPUT SIGNAL

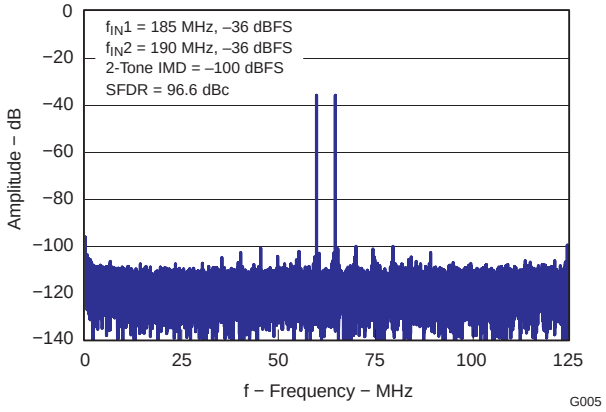


Figure 25.

SFDR vs INPUT FREQUENCY

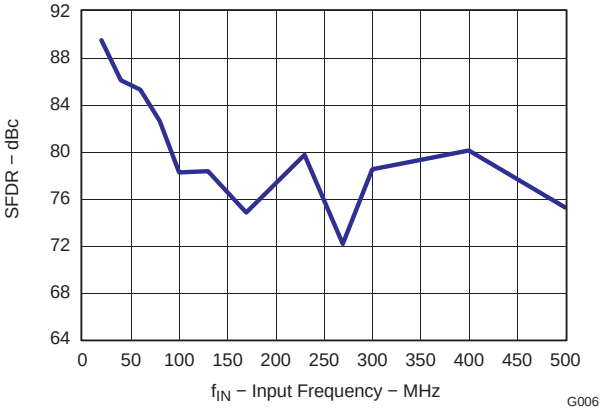


Figure 26.

TYPICAL CHARACTERISTICS – ADS62P49 (continued)

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, LVDS output interface, 32K point FFT (unless otherwise noted)

SNR vs INPUT FREQUENCY

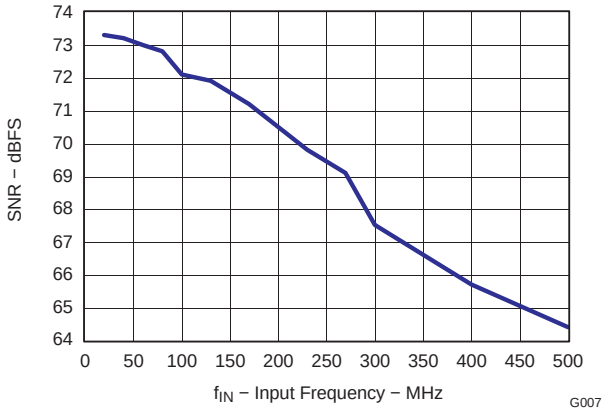


Figure 27.

SFDR vs INPUT FREQUENCY ACROSS GAIN

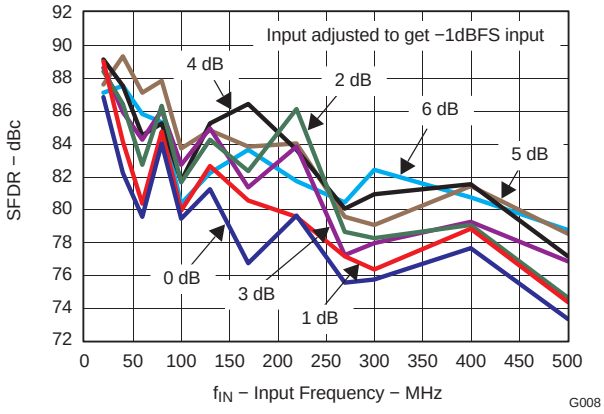


Figure 28.

SINAD vs INPUT FREQUENCY ACROSS GAIN

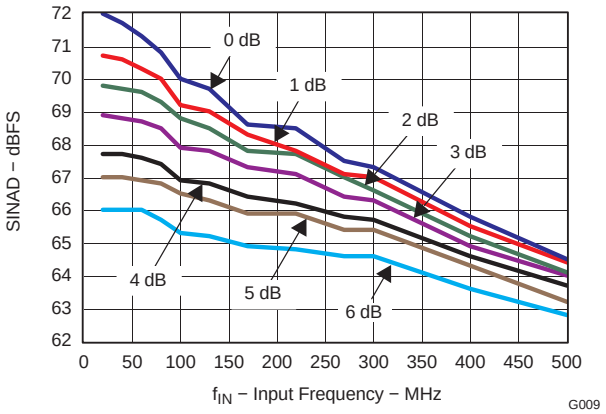


Figure 29.

PERFORMANCE vs INPUT AMPLITUDE, SINGLE TONE

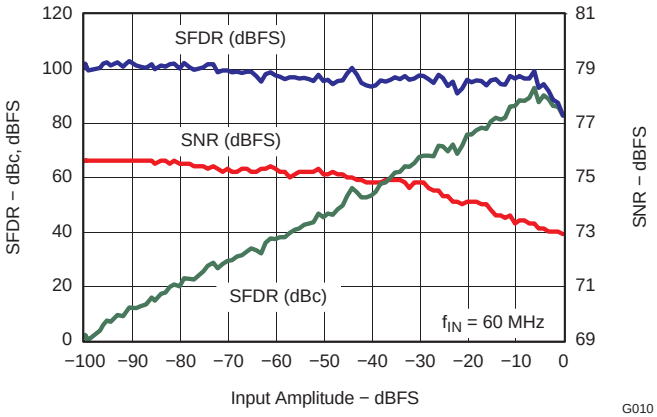


Figure 30.

PERFORMANCE vs COMMON-MODE INPUT VOLTAGE

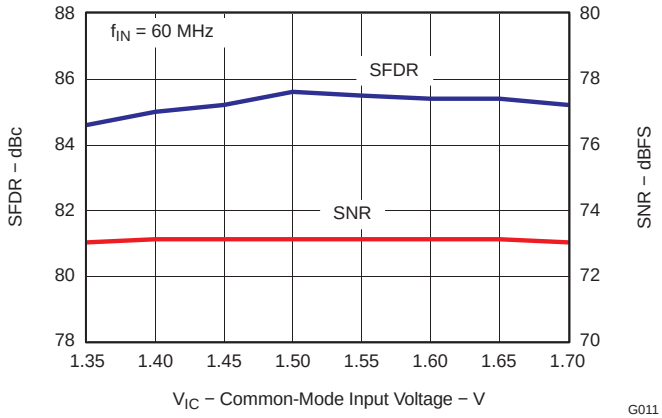


Figure 31.

SFDR vs AVDD SUPPLY VOLTAGE

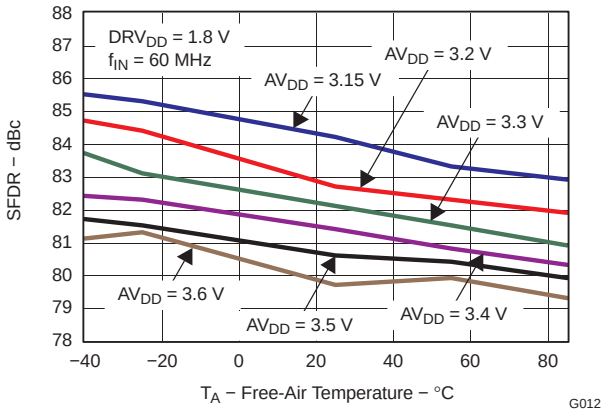


Figure 32.

TYPICAL CHARACTERISTICS – ADS62P49 (continued)

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, LVDS output interface, 32K point FFT (unless otherwise noted)

SNR vs AVDD SUPPLY VOLTAGE

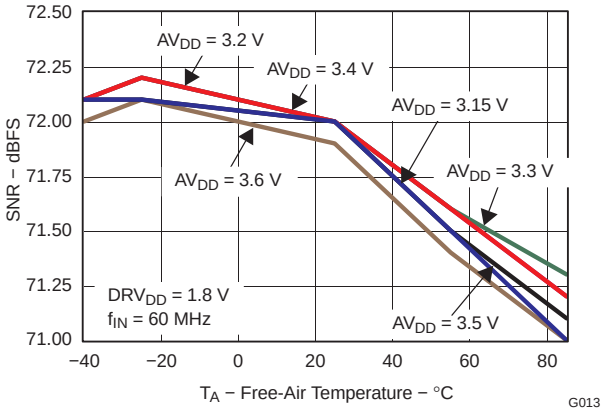


Figure 33.

PERFORMANCE vs DRVDD SUPPLY VOLTAGE

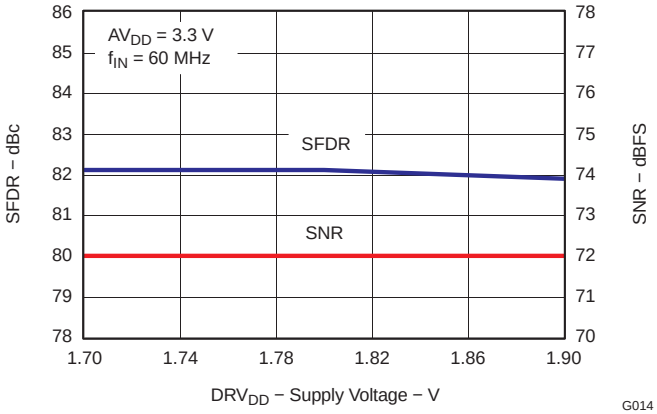


Figure 34.

PERFORMANCE vs INPUT CLOCK AMPLITUDE

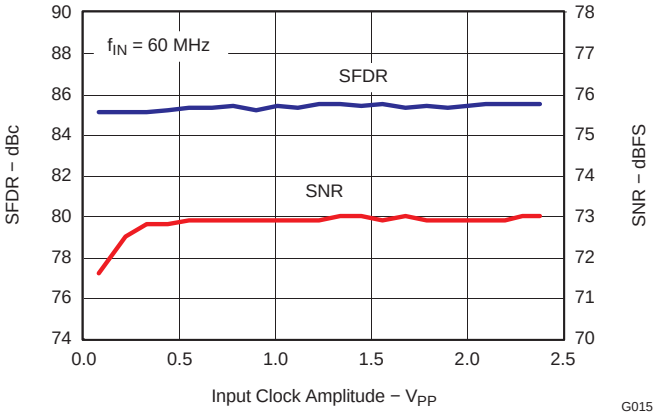


Figure 35.

PERFORMANCE vs INPUT CLOCK DUTY CYCLE

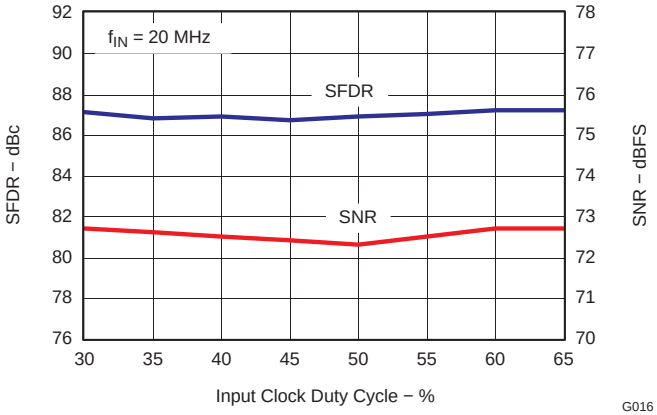


Figure 36.

PERFORMANCE IN EXTERNAL REFERENCE MODE

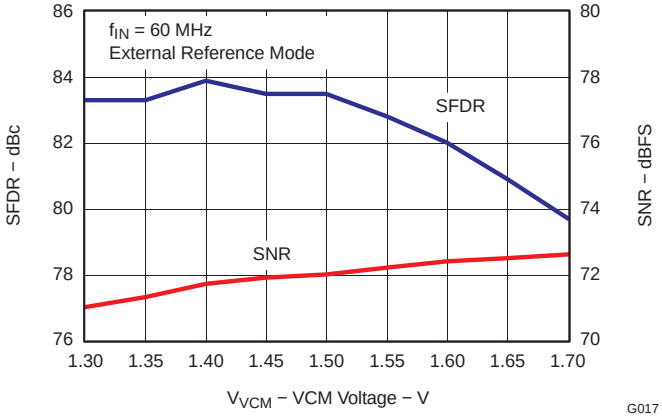


Figure 37.

TYPICAL CHARACTERISTICS – ADS62P48

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, LVDS output interface, 32K point FFT (unless otherwise noted)

FFT FOR 20 MHz INPUT SIGNAL

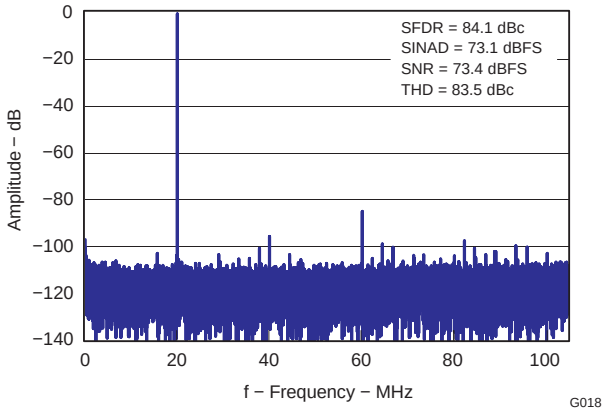


Figure 38.

FFT FOR 170 MHz INPUT SIGNAL

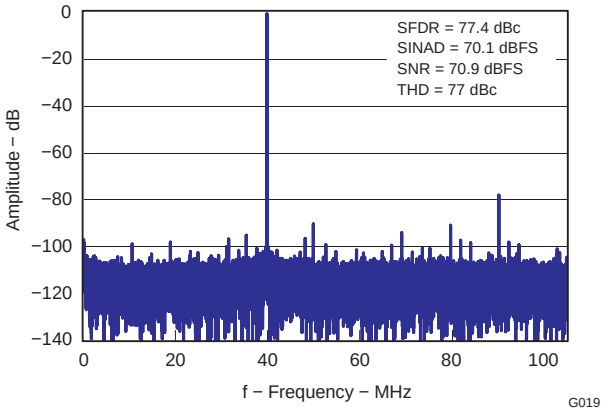


Figure 39.

FFT FOR 300 MHz INPUT SIGNAL

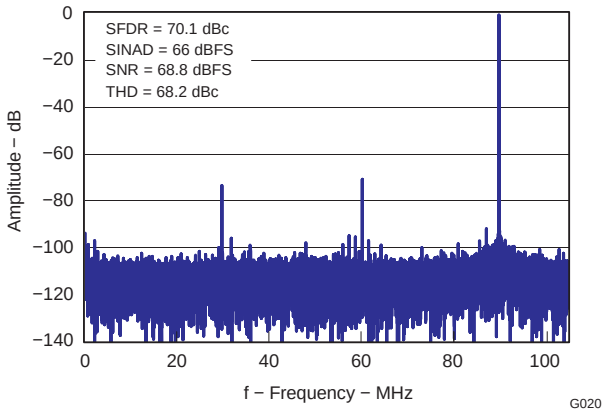


Figure 40.

FFT FOR 2-TONE INPUT SIGNAL

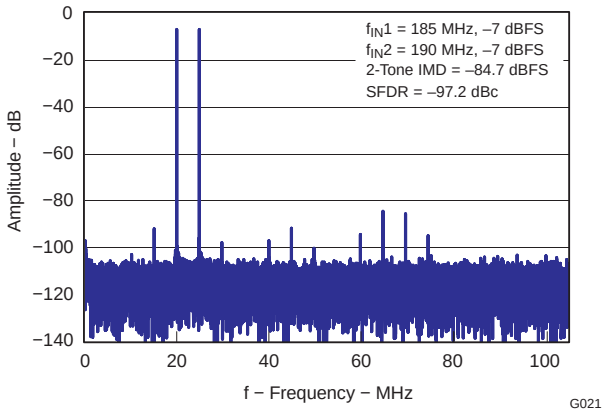


Figure 41.

FFT FOR 2-TONE INPUT SIGNAL

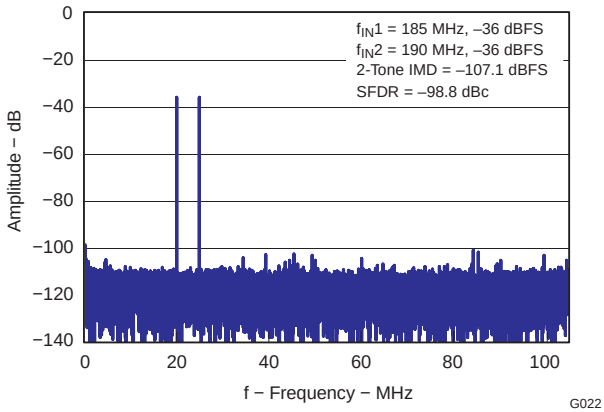


Figure 42.

SFDR vs INPUT FREQUENCY

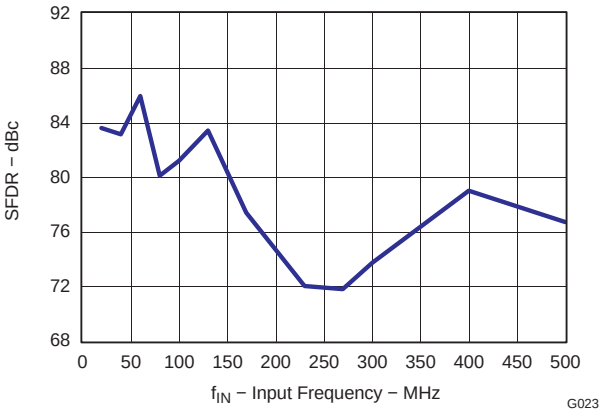


Figure 43.

TYPICAL CHARACTERISTICS – ADS62P48 (continued)

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, LVDS output interface, 32K point FFT (unless otherwise noted)

SNR vs INPUT FREQUENCY

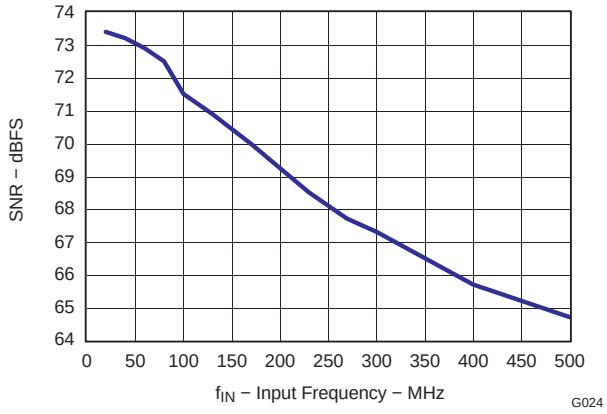


Figure 44.

SFDR vs INPUT FREQUENCY ACROSS GAIN

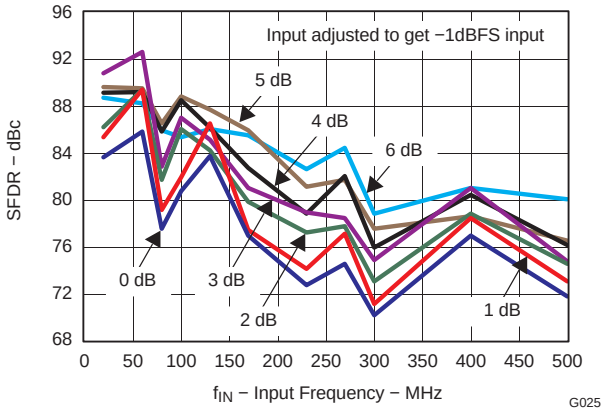


Figure 45.

SINAD vs INPUT FREQUENCY ACROSS GAIN

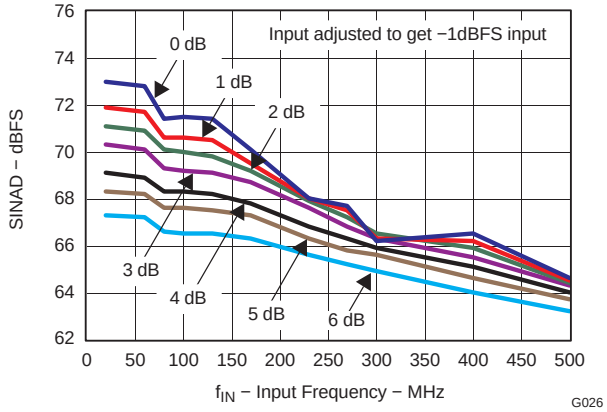


Figure 46.

PERFORMANCE vs INPUT AMPLITUDE, SINGLE TONE

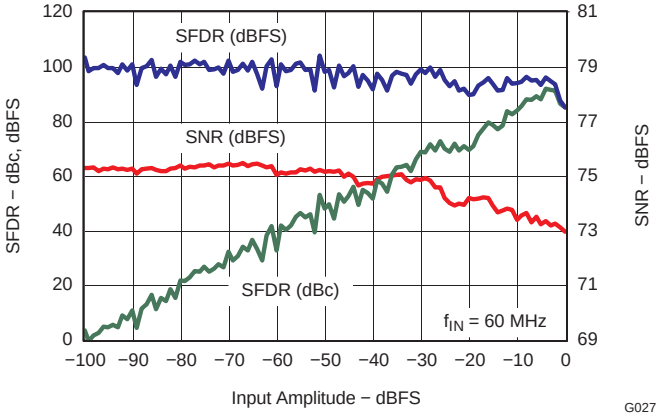


Figure 47.

PERFORMANCE vs COMMON-MODE INPUT VOLTAGE

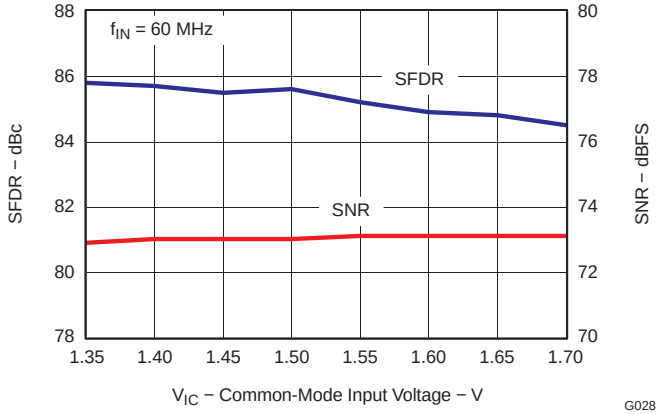


Figure 48.

SFDR vs AVDD SUPPLY VOLTAGE

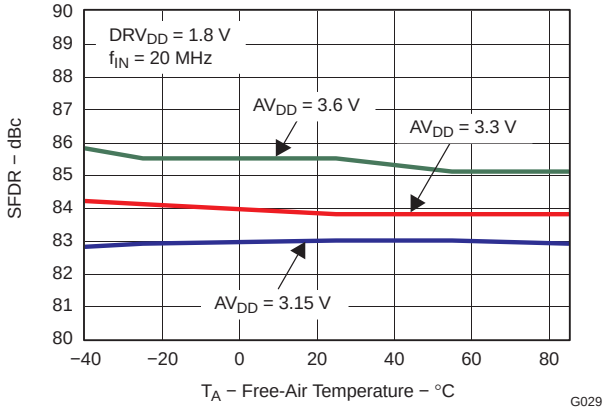


Figure 49.

TYPICAL CHARACTERISTICS – ADS62P48 (continued)

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, LVDS output interface, 32K point FFT (unless otherwise noted)

SNR vs AVDD SUPPLY VOLTAGE

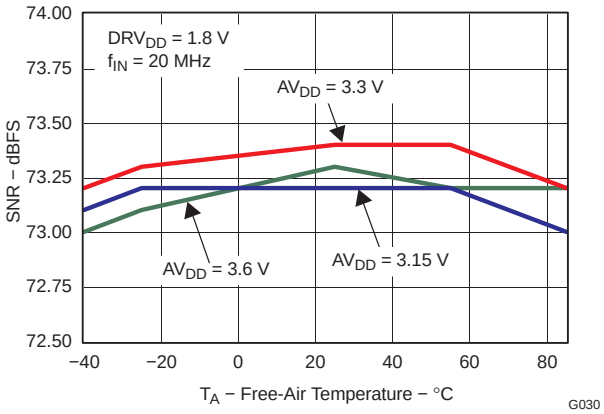


Figure 50.

PERFORMANCE vs DRVDD SUPPLY VOLTAGE

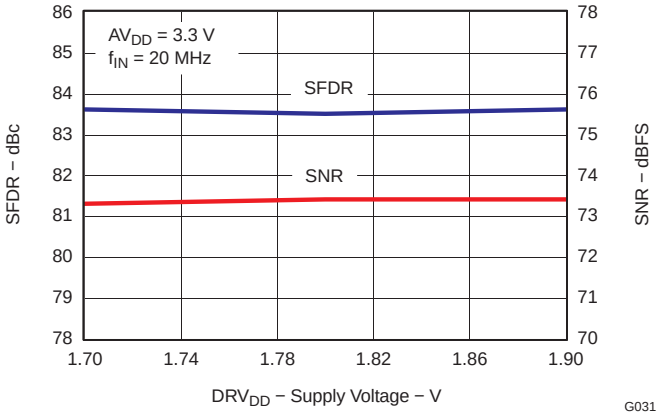


Figure 51.

PERFORMANCE vs INPUT CLOCK AMPLITUDE

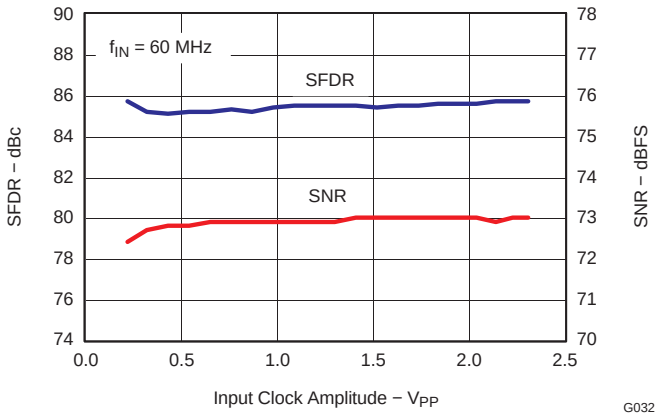


Figure 52.

PERFORMANCE vs INPUT CLOCK DUTY CYCLE

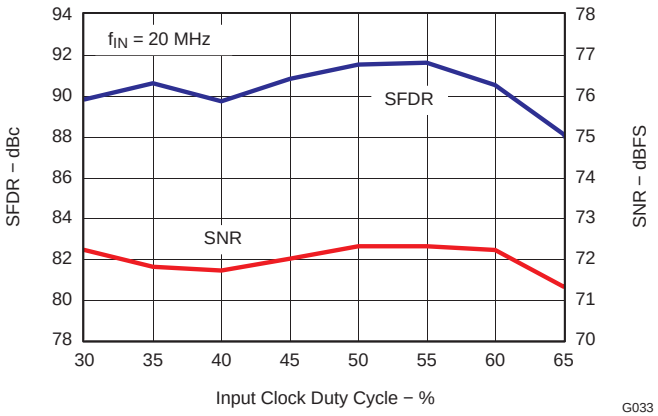


Figure 53.

PERFORMANCE IN EXTERNAL REFERENCE MODE

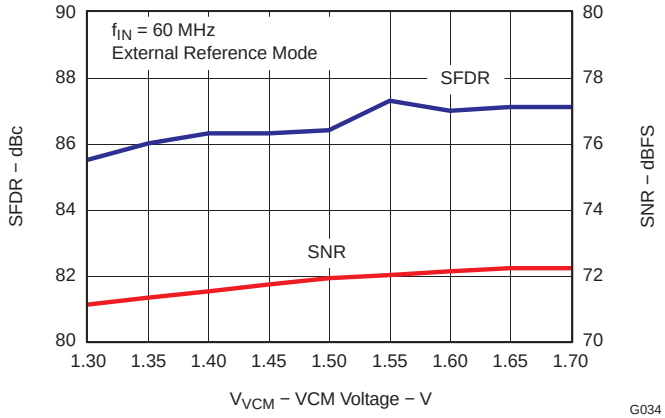


Figure 54.

TYPICAL CHARACTERISTICS – ADS62P29

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, LVDS output interface, 32K point FFT (unless otherwise noted)

FFT FOR 20 MHz INPUT SIGNAL

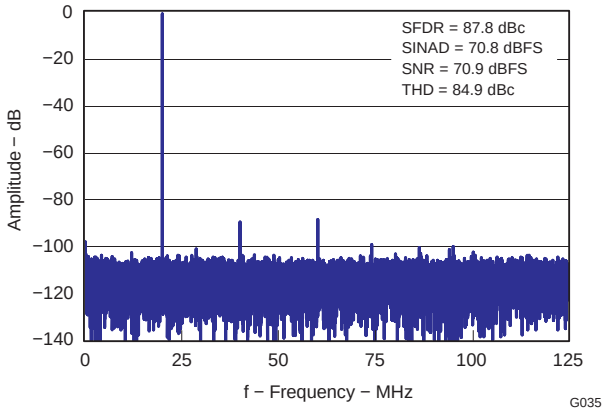


Figure 55.

FFT FOR 170 MHz INPUT SIGNAL

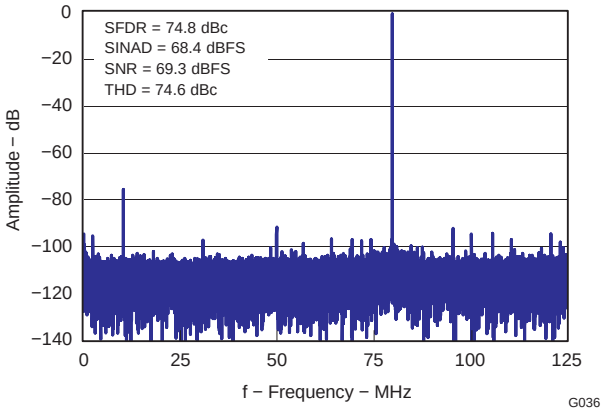


Figure 56.

FFT FOR 300 MHz INPUT SIGNAL

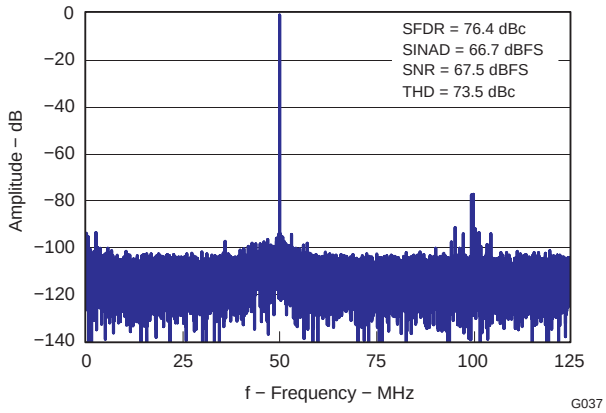


Figure 57.

FFT FOR 2-TONE INPUT SIGNAL

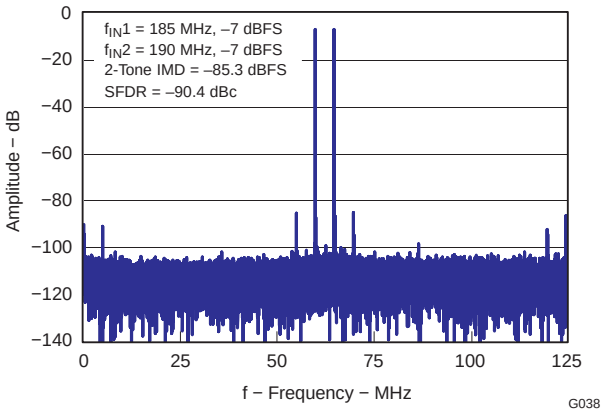


Figure 58.

FFT FOR 2-TONE INPUT SIGNAL

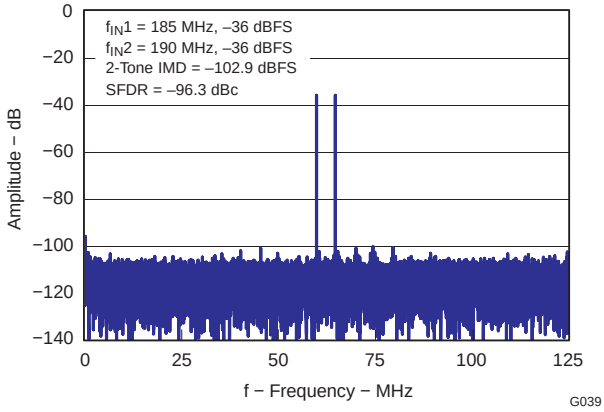


Figure 59.

SFDR vs INPUT FREQUENCY

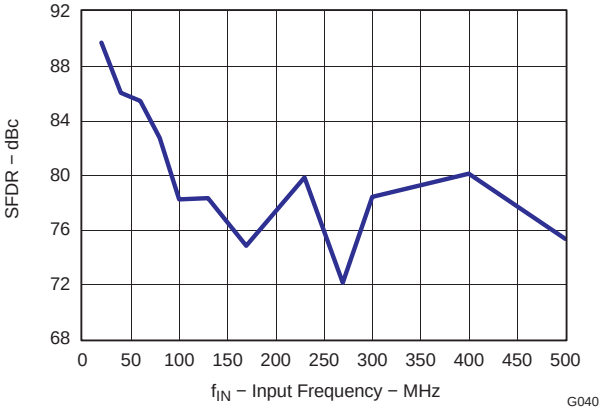


Figure 60.

TYPICAL CHARACTERISTICS – ADS62P29 (continued)

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, LVDS output interface, 32K point FFT (unless otherwise noted)

SNR vs INPUT FREQUENCY

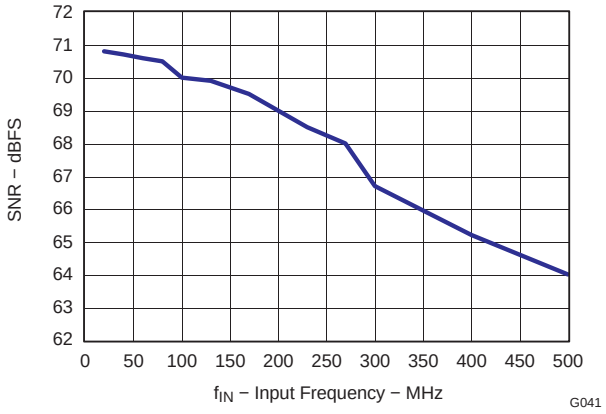


Figure 61.

SFDR vs INPUT FREQUENCY ACROSS GAIN

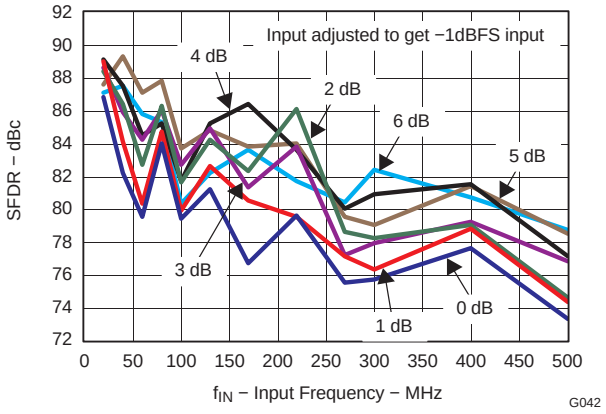


Figure 62.

SINAD vs INPUT FREQUENCY ACROSS GAIN

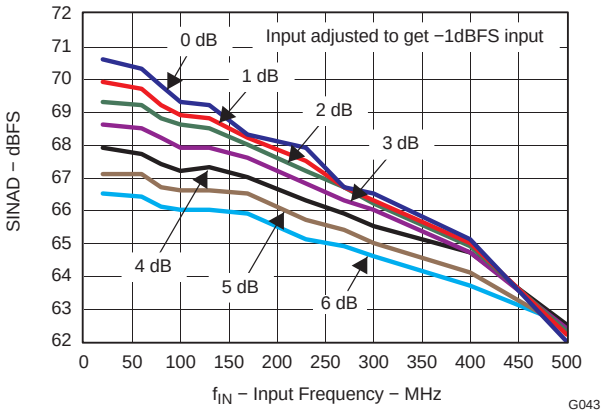


Figure 63.

PERFORMANCE vs INPUT AMPLITUDE, SINGLE TONE

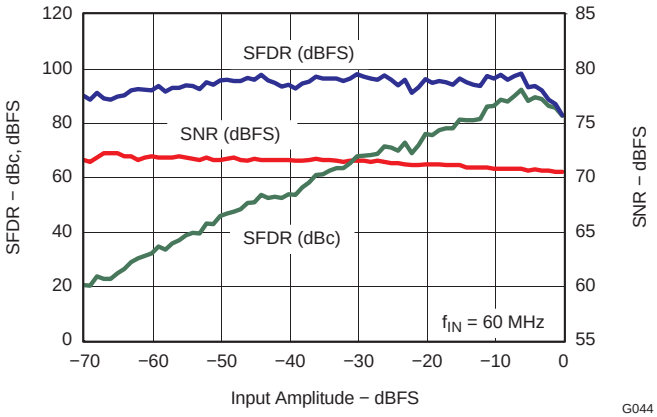


Figure 64.

PERFORMANCE vs COMMON-MODE INPUT VOLTAGE

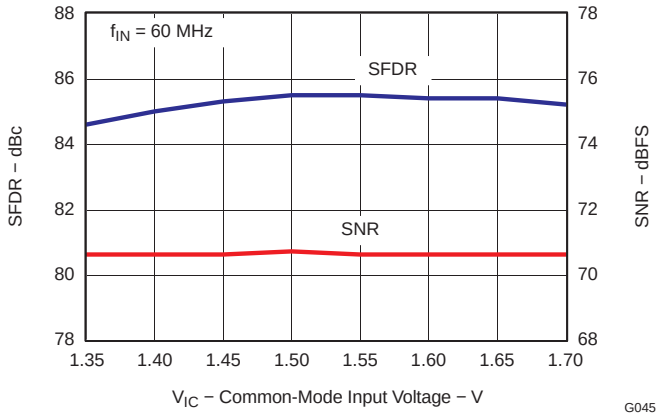


Figure 65.

SFDR vs AVDD SUPPLY VOLTAGE

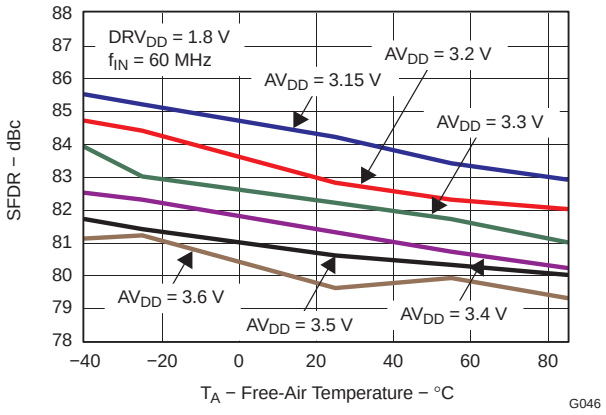


Figure 66.

TYPICAL CHARACTERISTICS – ADS62P29 (continued)

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, LVDS output interface, 32K point FFT (unless otherwise noted)

SNR vs AVDD SUPPLY VOLTAGE

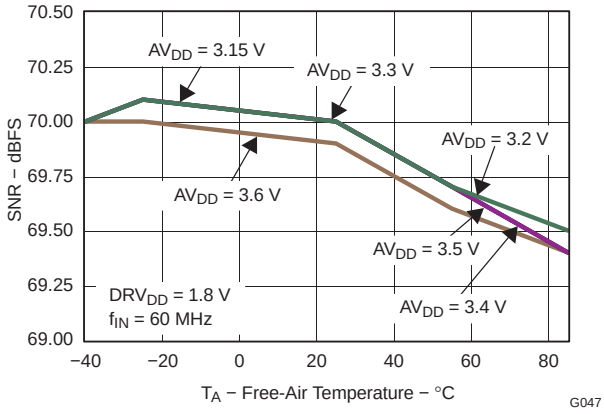


Figure 67.

PERFORMANCE vs DRVDD SUPPLY VOLTAGE

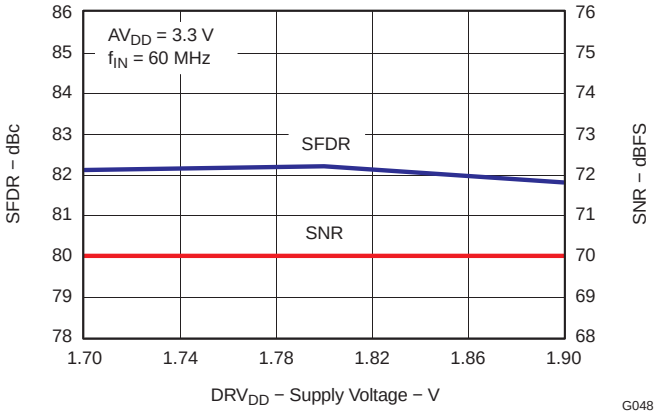


Figure 68.

PERFORMANCE vs INPUT CLOCK AMPLITUDE

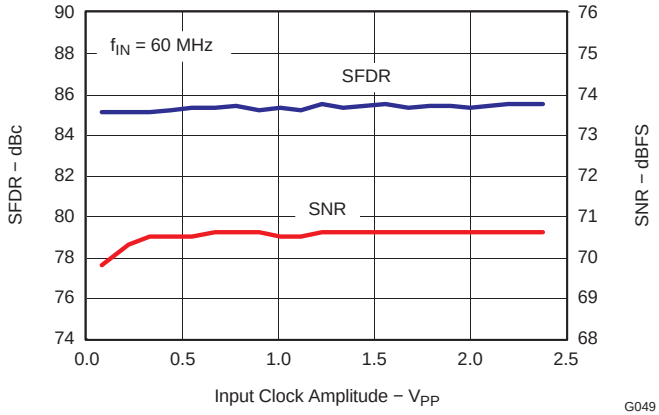


Figure 69.

PERFORMANCE vs INPUT CLOCK DUTY CYCLE

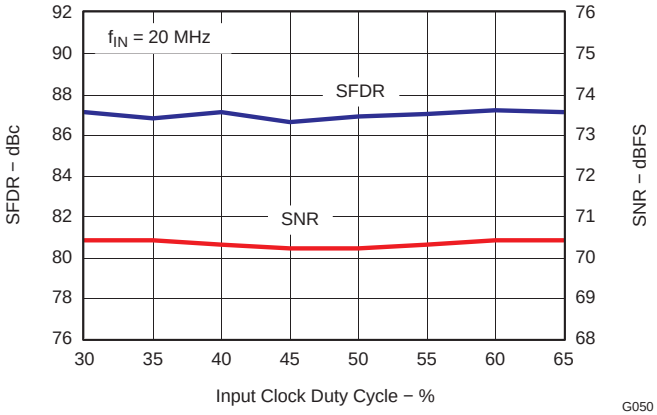


Figure 70.

PERFORMANCE IN EXTERNAL REFERENCE MODE

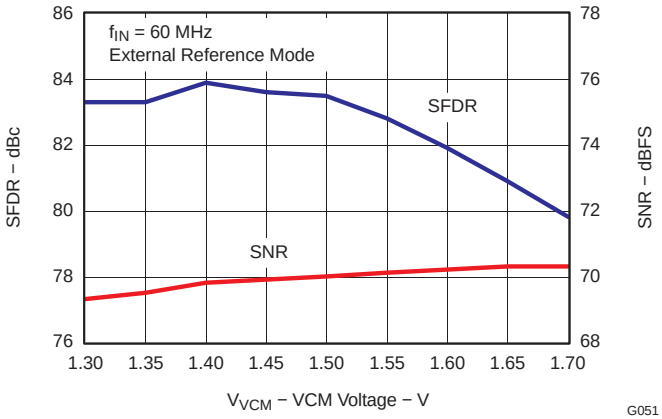


Figure 71.

TYPICAL CHARACTERISTICS – ADS62P28

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, LVDS output interface, 32K point FFT (unless otherwise noted)

FFT FOR 20 MHz INPUT SIGNAL

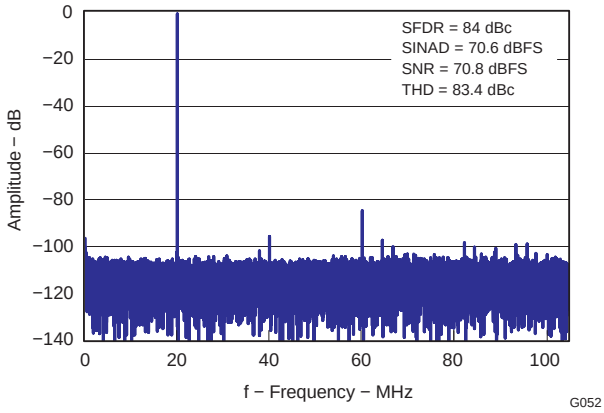


Figure 72.

FFT FOR 170 MHz INPUT SIGNAL

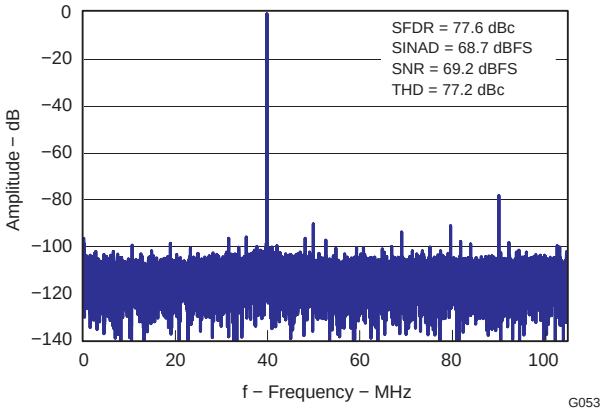


Figure 73.

FFT FOR 300 MHz INPUT SIGNAL

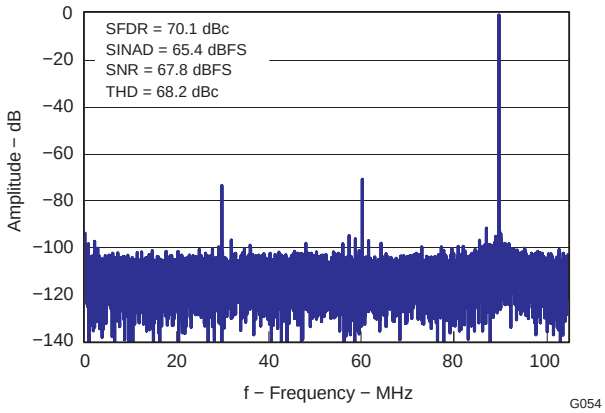


Figure 74.

FFT FOR 2-TONE INPUT SIGNAL

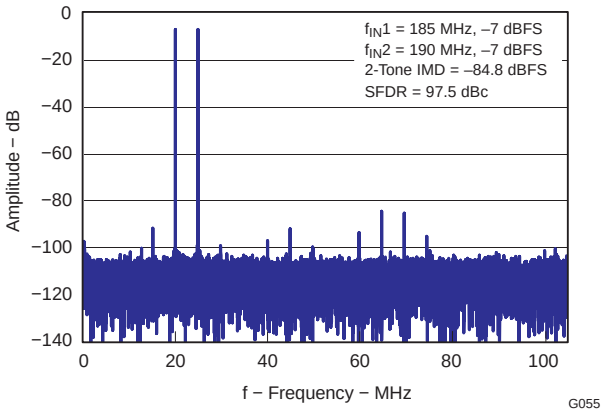


Figure 75.

FFT FOR 2-TONE INPUT SIGNAL

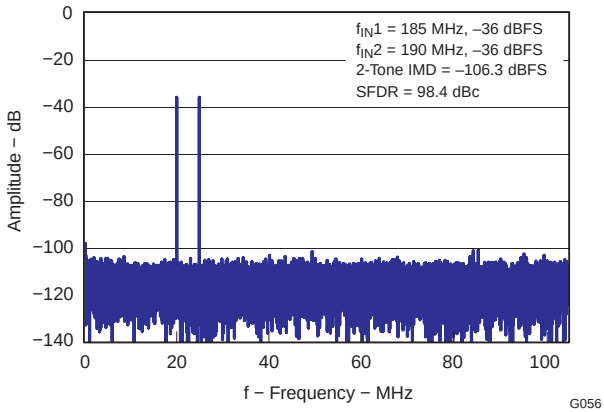


Figure 76.

SFDR vs INPUT FREQUENCY

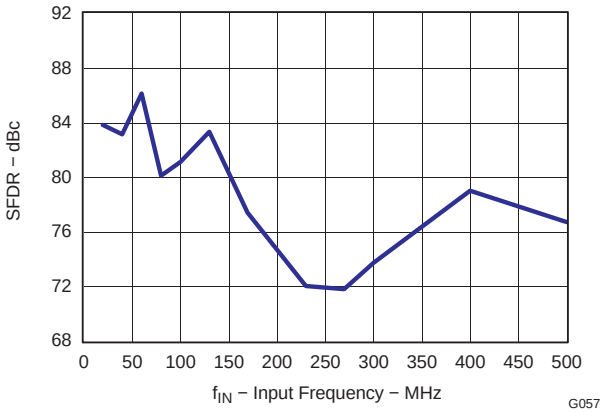


Figure 77.

TYPICAL CHARACTERISTICS – ADS62P28 (continued)

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, LVDS output interface, 32K point FFT (unless otherwise noted)

SNR vs INPUT FREQUENCY

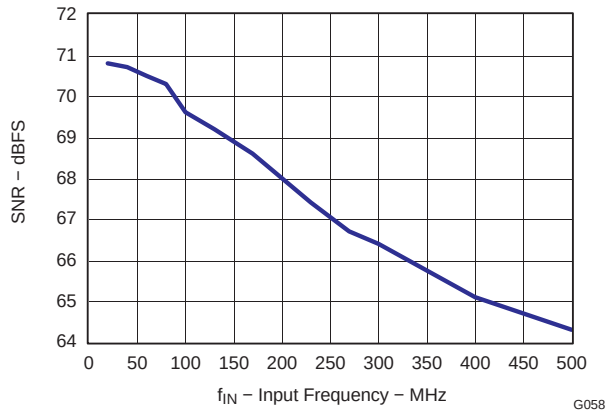


Figure 78.

SFDR vs INPUT FREQUENCY ACROSS GAIN

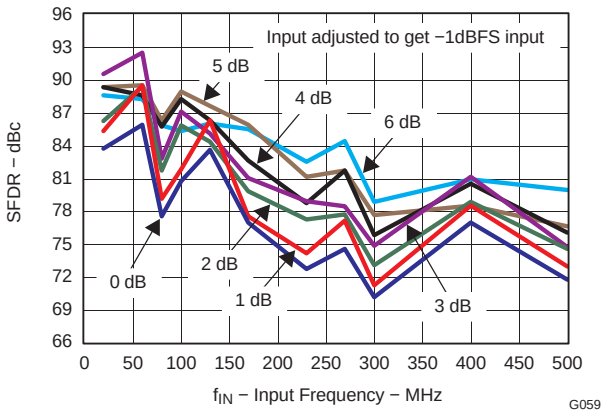


Figure 79.

SINAD vs INPUT FREQUENCY ACROSS GAIN

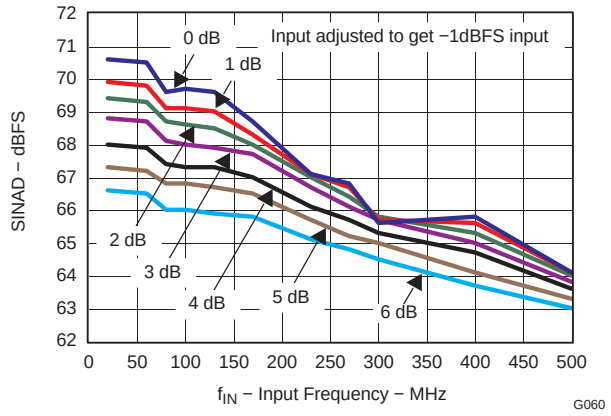


Figure 80.

PERFORMANCE vs INPUT AMPLITUDE, SINGLE TONE

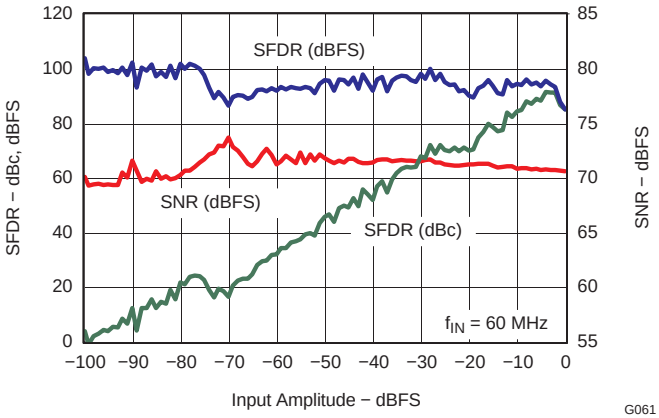


Figure 81.

PERFORMANCE vs COMMON-MODE INPUT VOLTAGE

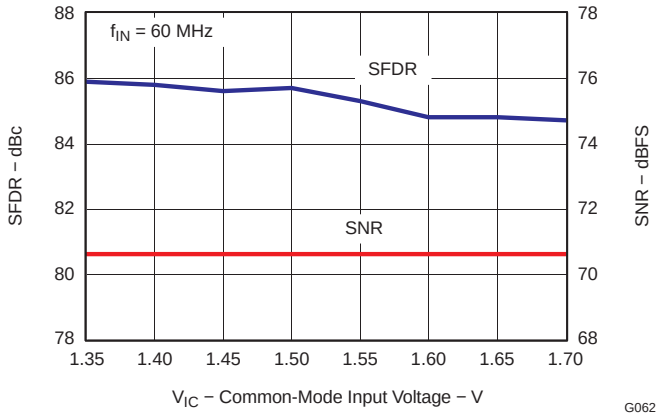


Figure 82.

SFDR vs AVDD SUPPLY VOLTAGE

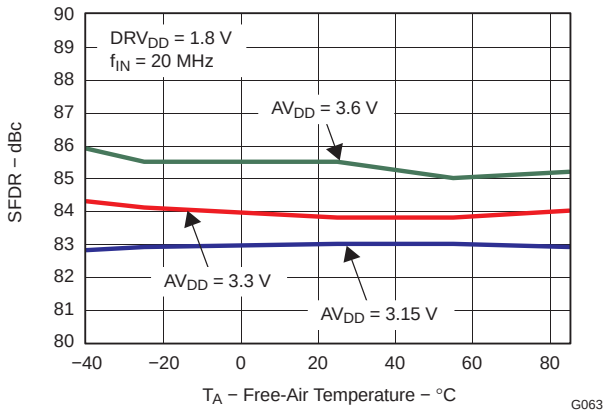


Figure 83.

TYPICAL CHARACTERISTICS – ADS62P28 (continued)

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, LVDS output interface, 32K point FFT (unless otherwise noted)

SNR vs AVDD SUPPLY VOLTAGE

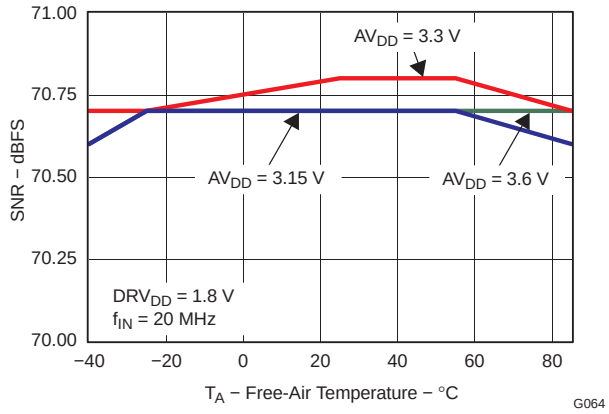


Figure 84.

PERFORMANCE vs DRVDD SUPPLY VOLTAGE

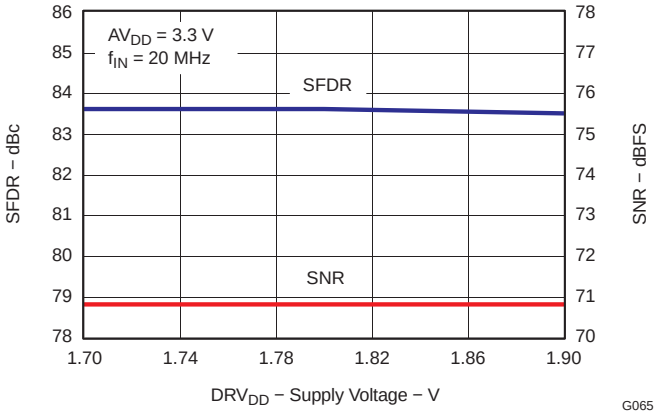


Figure 85.

PERFORMANCE vs INPUT CLOCK AMPLITUDE

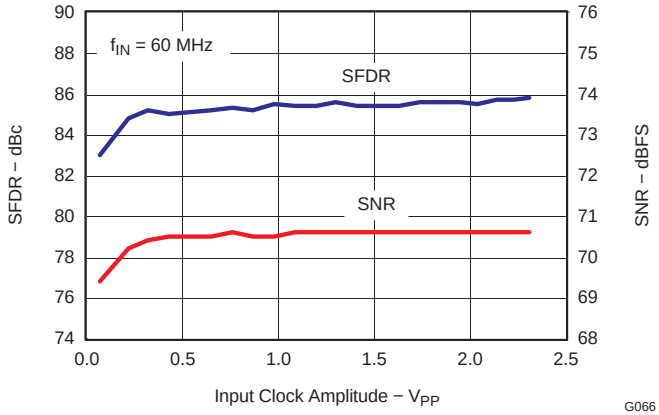


Figure 86.

PERFORMANCE vs INPUT CLOCK DUTY CYCLE

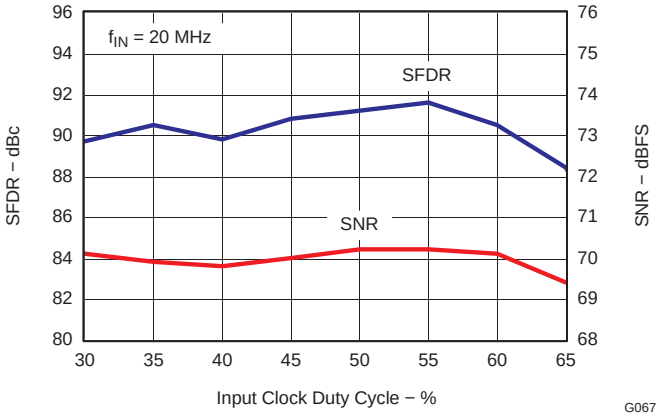


Figure 87.

PERFORMANCE IN EXTERNAL REFERENCE MODE

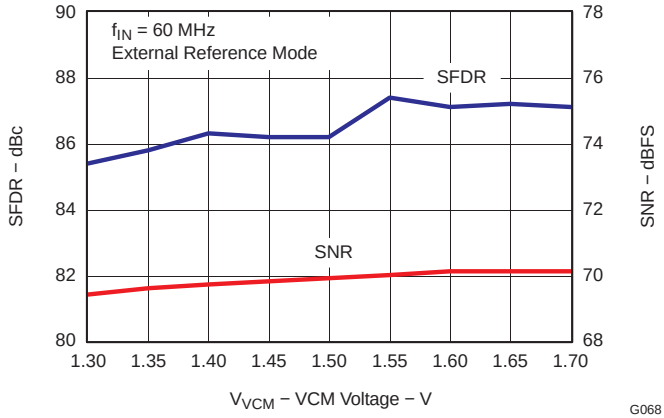


Figure 88.

TYPICAL CHARACTERISTICS – COMMON PLOTS

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, LVDS output interface, 32K point FFT (unless otherwise noted)

CROSSTALK vs FREQUENCY

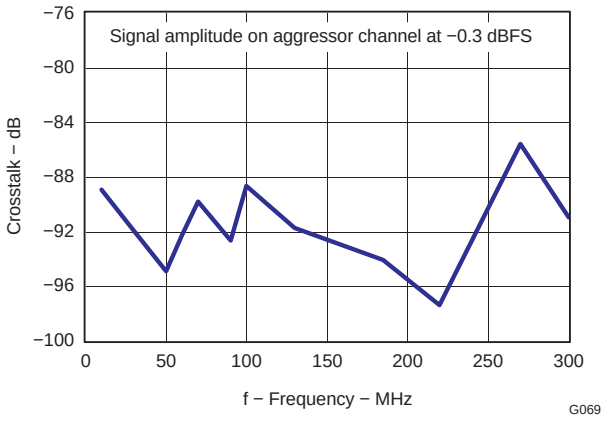


Figure 89.

CMRR vs FREQUENCY

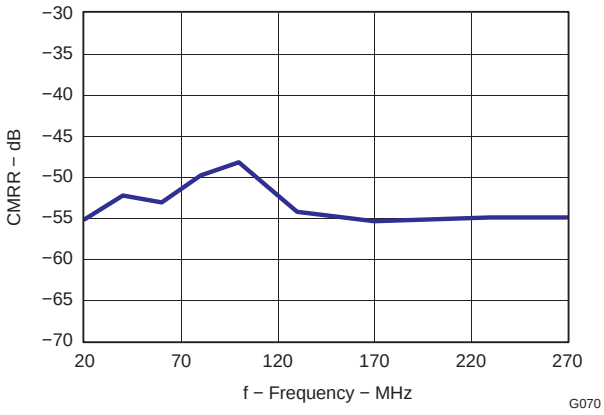


Figure 90.

POWER DISSIPATION vs SAMPLING FREQUENCY

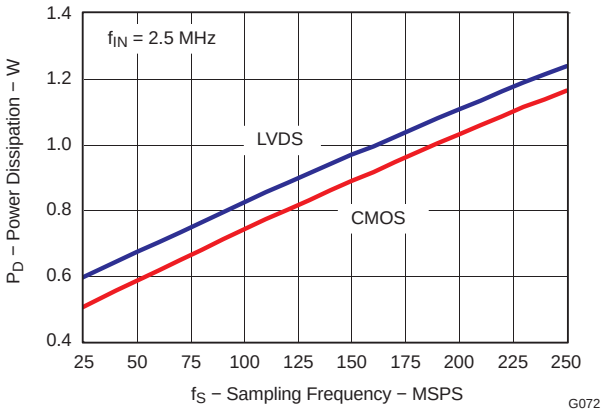


Figure 91.

DRVDD CURRENT vs SAMPLING FREQUENCY

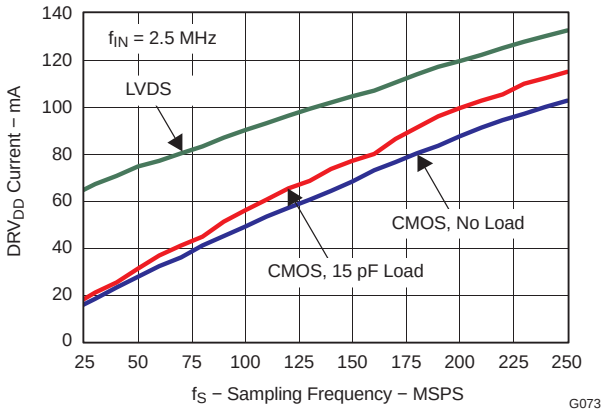


Figure 92.

TYPICAL CHARACTERISTICS – ADS62P49/48/29/28

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, LVDS output interface, 32K point FFT (unless otherwise noted)

SFDR CONTOUR, 0 dB GAIN, UP TO 500 MHz

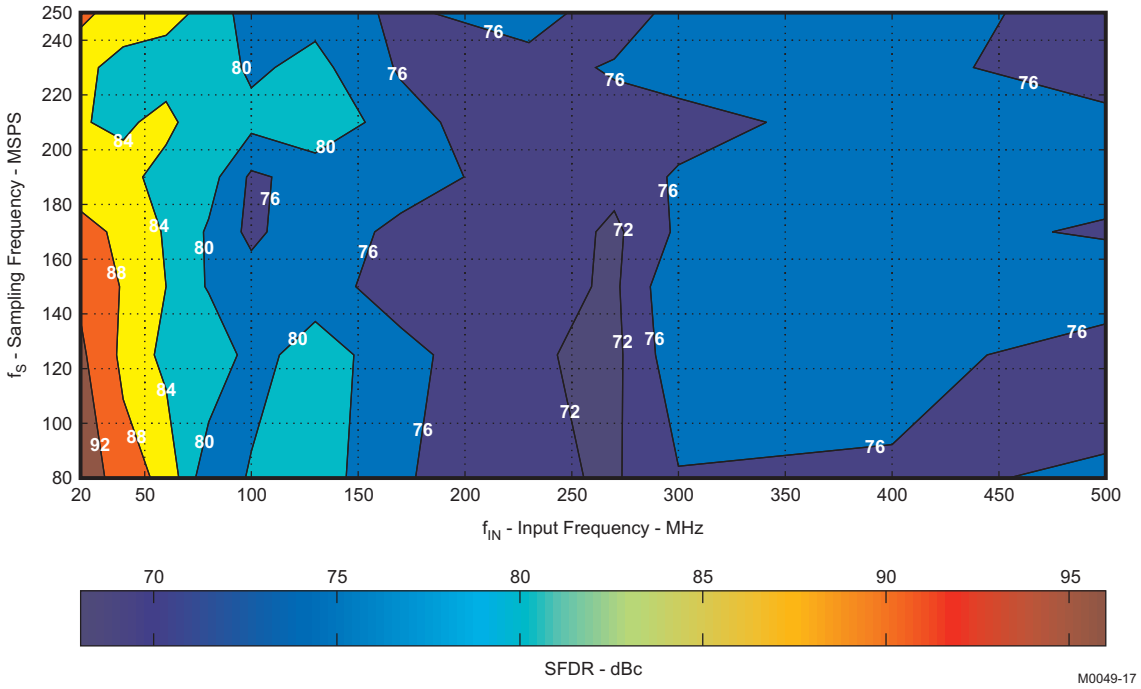


Figure 93.

SFDR CONTOUR, 6 dB GAIN, UP TO 800 MHz

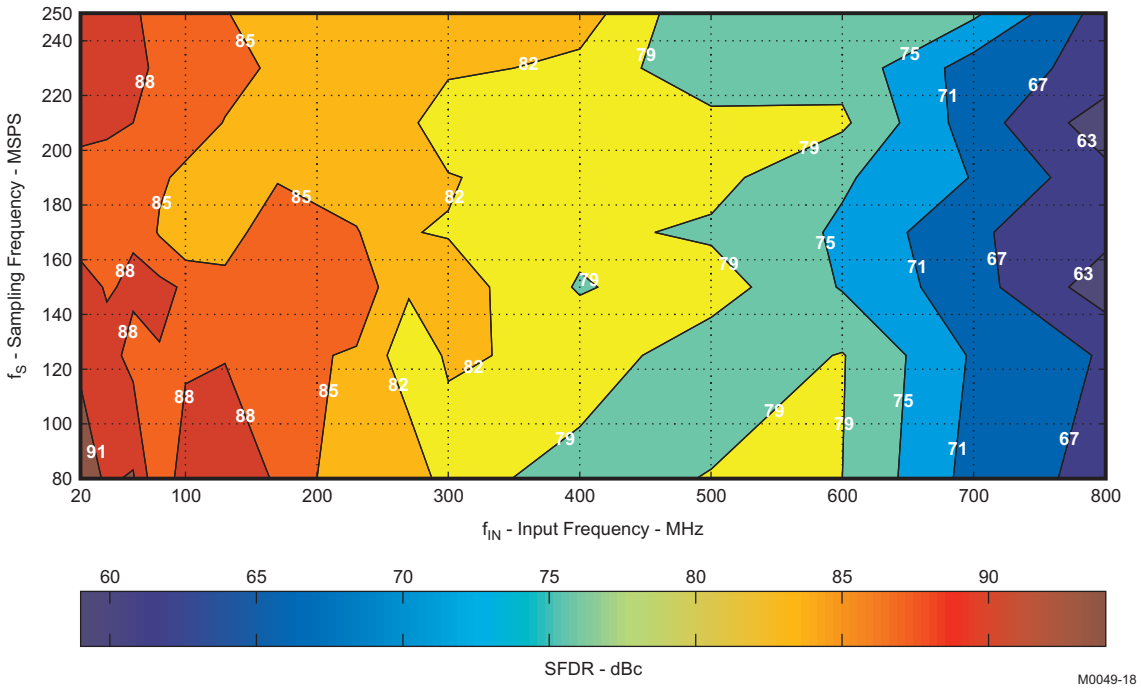


Figure 94.

TYPICAL CHARACTERISTICS – ADS62P49/48

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, LVDS output interface, 32K point FFT (unless otherwise noted)

SNR CONTOUR, 0 dB GAIN, UP TO 500 MHz

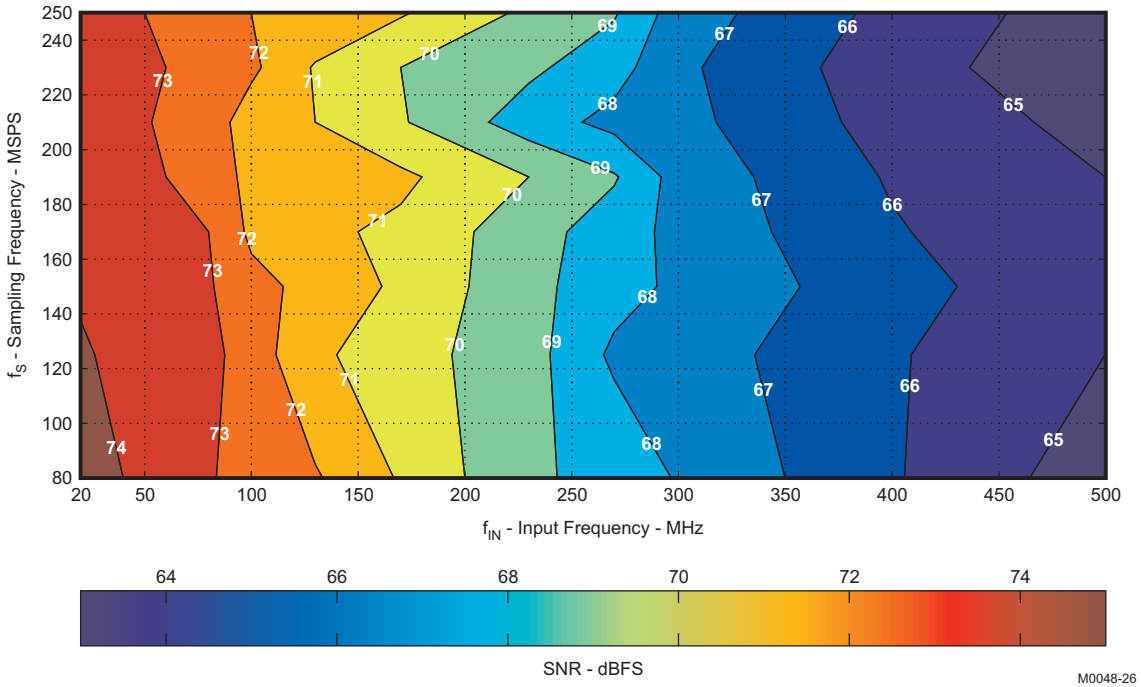


Figure 95.

SNR CONTOUR, 6 dB GAIN, UP TO 800 MHz

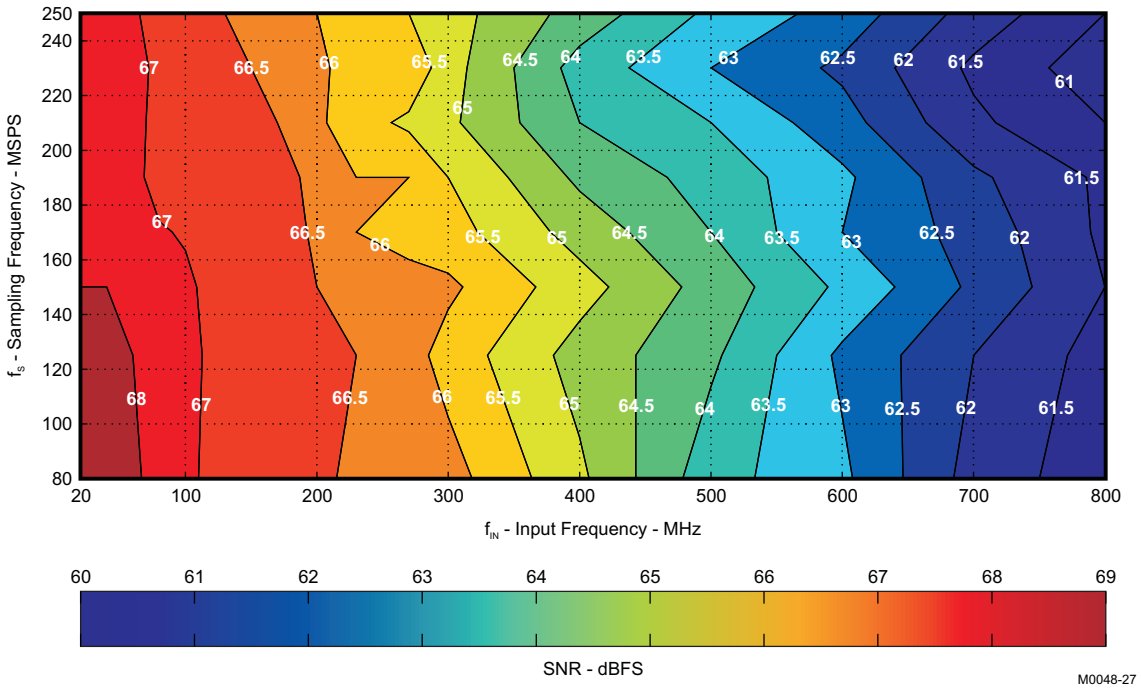


Figure 96.

TYPICAL CHARACTERISTICS – ADS62P29/28

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5 V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, LVDS output interface, 32K point FFT (unless otherwise noted)

SNR CONTOUR, 0 dB GAIN, UP TO 500 MHz

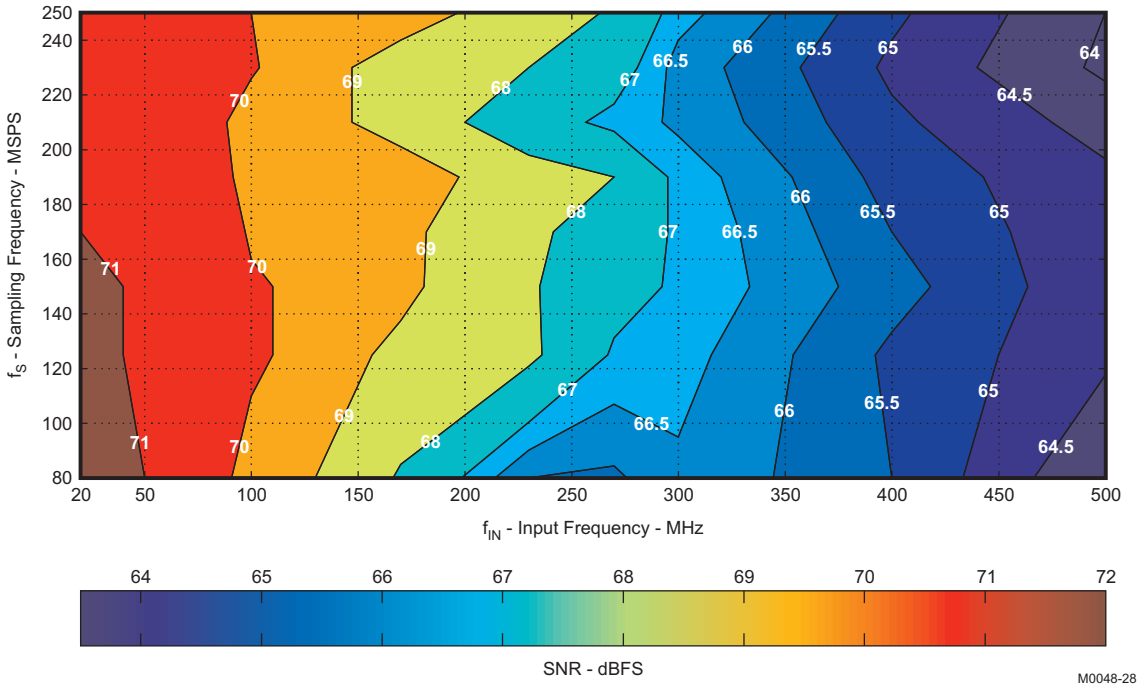


Figure 97.

SNR CONTOUR, 6 dB GAIN, UP TO 800 MHz

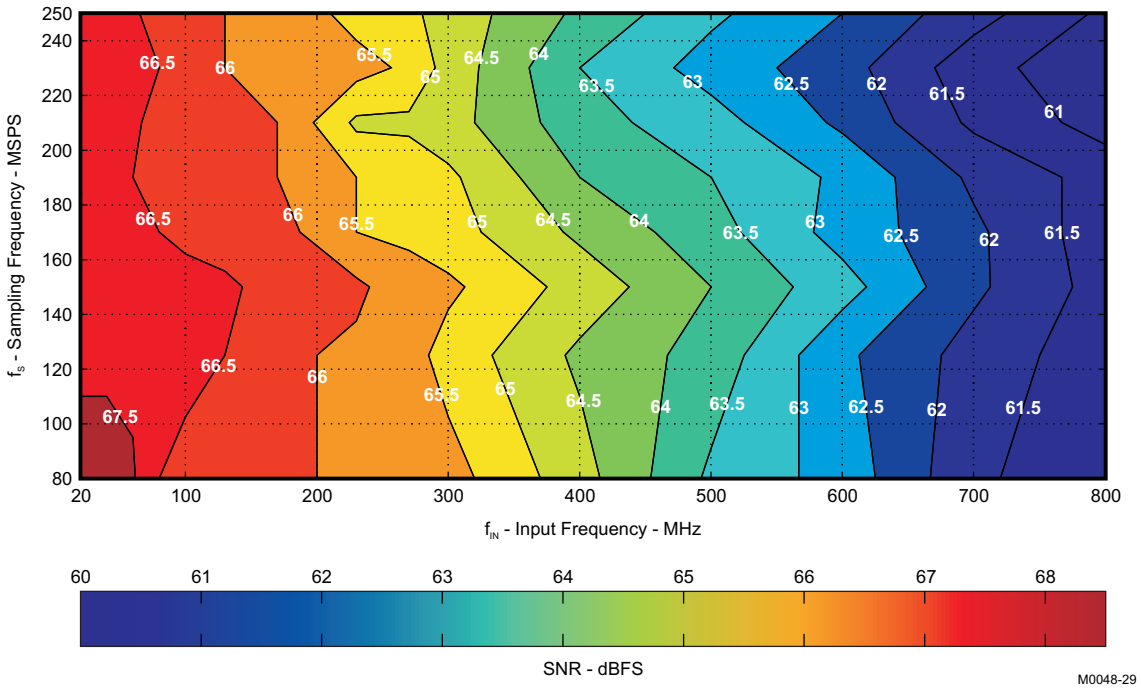


Figure 98.

APPLICATION INFORMATION

THEORY OF OPERATION

The ADS62Px9/x8 is a family of high performance and low power dual channel 14-bit/12-bit A/D converters with sampling rates up to 250 MSPS.

At every falling edge of the input clock, the analog input signal of each channel is sampled simultaneously. The sampled signal in each channel is converted by a pipeline of low resolution stages. In each stage, the sampled and held signal is converted by a high speed, low resolution flash sub-ADC. The difference (residue) between the stage input and its quantized equivalent is gained and propagates to the next stage.

At every clock, each succeeding stage resolves the sampled input with greater accuracy. The digital outputs from all stages are combined in a digital correction logic block and processed digitally to create the final code, after a data latency of 22 clock cycles.

The digital output is available as either DDR LVDS or parallel CMOS and coded in either straight offset binary or binary 2s complement format.

The dynamic offset of the first stage sub-ADC limits the maximum analog input frequency to about 500MHz (with 2V pp amplitude) and about 800MHz (with 1V pp amplitude).

ANALOG INPUT

The analog input consists of a switched-capacitor based differential sample and hold architecture. This differential topology results in very good AC performance even for high input frequencies at high sampling rates. The INP and INM pins have to be externally biased around a common-mode voltage of 1.5V, available on VCM pin. For a full-scale differential input, each input pin INP, INM has to swing symmetrically between VCM + 0.5V and VCM – 0.5V, resulting in a 2Vpp differential input swing.

The input sampling circuit has a high 3-dB bandwidth that extends up to 700 MHz (measured from the input pins to the sampled voltage).

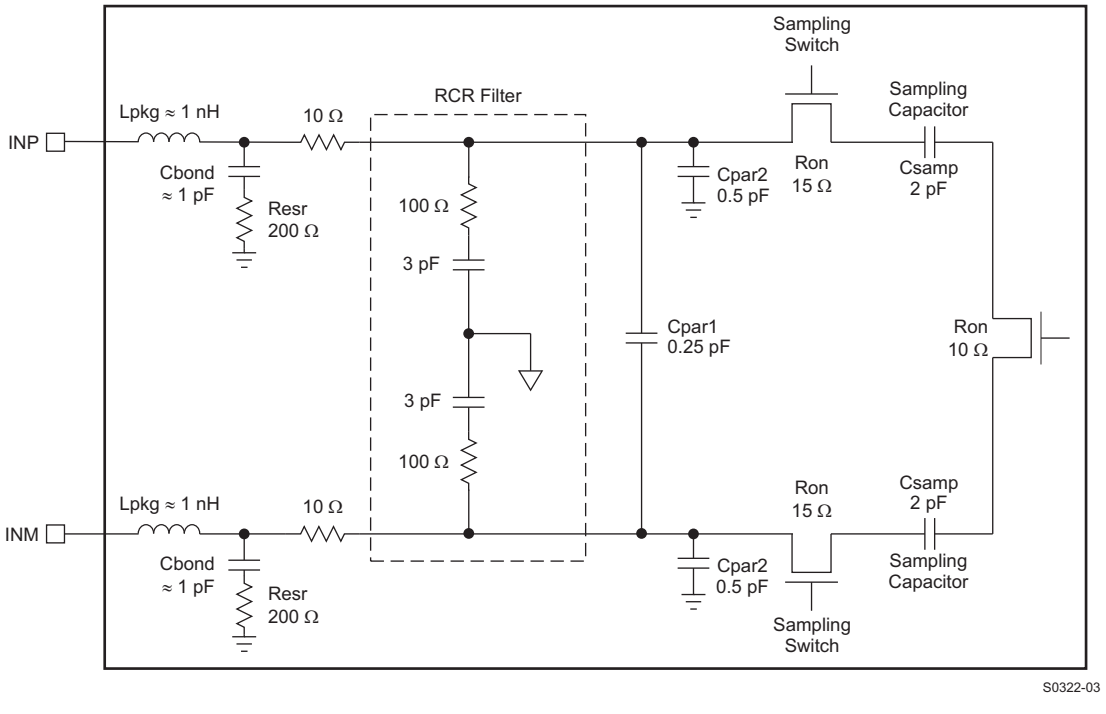


Figure 99. Analog Input Circuit

Drive Circuit Requirements

For optimum performance, the analog inputs must be driven differentially. This improves the common-mode noise immunity and even order harmonic rejection. A 5-Ω to 15-Ω resistor in series with each input pin is recommended to damp out ringing caused by package parasitic.

SFDR performance can be limited due to several reasons - the effect of sampling glitches (described below), non-linearity of the sampling circuit and non-linearity of the quantizer that follows the sampling circuit. Depending on the input frequency, sample rate and input amplitude, one of these plays a dominant part in limiting performance.

At very high input frequencies (> about 300 MHz), SFDR is determined largely by the device's sampling circuit non-linearity. At low input amplitudes, the quantizer non-linearity usually limits performance.

Glitches are caused by the opening and closing of the sampling switches. The driving circuit should present a low source impedance to absorb these glitches. Otherwise, this could limit performance, mainly at low input frequencies (up to about 200 MHz). It is also necessary to present low impedance (< 50 Ω) for the common mode switching currents. This can be achieved by using two resistors from each input terminated to the common mode voltage (VCM).

The device includes an internal R-C filter from each input to ground. The purpose of this filter is to absorb the sampling glitches inside the device itself. The cut-off frequency of the R-C filter involves a trade-off. A lower cut-off frequency (larger C) absorbs glitches better, but it reduces the input bandwidth. On the other hand, with a higher cut-off frequency (smaller C), bandwidth support is maximized. But now, the sampling glitches need to be supplied by the external drive circuit. This has limitations due to the presence of the package bond-wire inductance.

In ADS62PXX, the R-C component values have been optimized while supporting high input bandwidth (up to 700 MHz). However, in applications with input frequencies up to 200-300MHz, the filtering of the glitches can be improved further using an external R-C-R filter (as shown in Figure 102 and Figure 103).

In addition to the above, the drive circuit may have to be designed to provide a low insertion loss over the desired frequency range and matched impedance to the source. While doing this, the ADC input impedance must be considered. Figure 100 and Figure 101 show the impedance (Zin = Rin || Cin) looking into the ADC input pins.

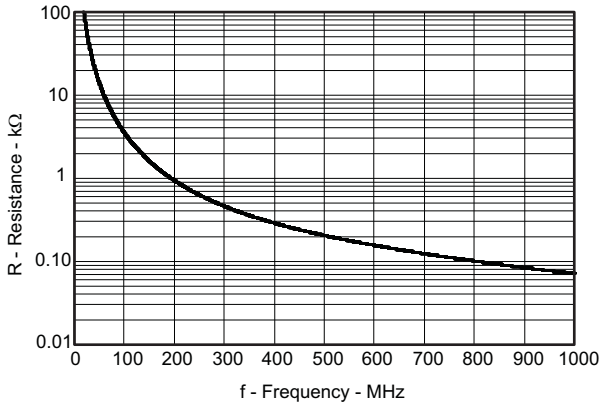


Figure 100. ADC Analog Input Resistance (Rin) Across Frequency

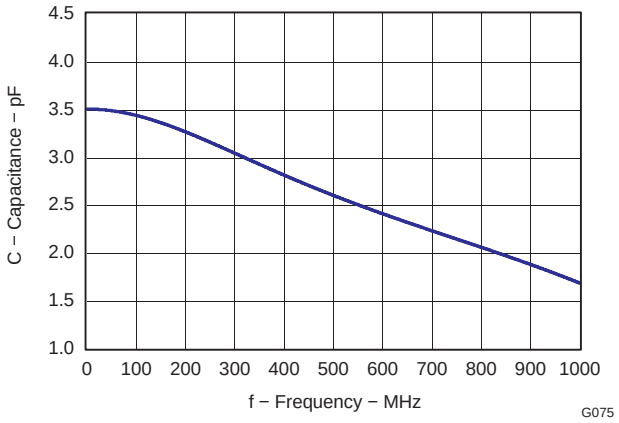


Figure 101. ADC Analog Input Capacitance (Cin) Across Frequency

Driving Circuit

Two example driving circuit configurations are shown in Figure 102 and Figure 103 one optimized for low bandwidth (low input frequencies) and the other one for high bandwidth to support higher input frequencies.

In Figure 102, an external R-C-R filter using 22 pF has been used. Together with the series inductor (39 nH), this combination forms a filter and absorbs the sampling glitches. Due to the large capacitor (22 pF) in the R-C-R and the 15-Ω resistors in series with each input pin, the drive circuit has low bandwidth and supports low input frequencies (< 100MHz).

To support higher input frequencies (up to about 300 MHz, see Figure 103), the capacitance used in the R-C-R is reduced to 3.3 pF and the series inductors are shorted out. Together with the lower series resistors (5 Ω), this drive circuit provides high bandwidth and supports high input frequencies. Transformers such as ADT1-1WT or ETC1-1-13 can be used up to 300MHz.

Without the external R-C-R filter, the drive circuit has very high bandwidth and can support very high input frequencies (> 300MHz). For example, a transmission line transformer such as ADTL2-18 can be used (see Figure 104).

Note that both the drive circuits have been terminated by 50 Ω near the ADC side. The termination is accomplished by a 25-Ω resistor from each input to the 1.5-V common-mode (VCM) from the device. This allows the analog inputs to be biased around the required common-mode voltage.

The mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back to back helps minimize this mismatch and good performance is obtained for high frequency input signals. An additional termination resistor pair may be required between the two transformers as shown in the figures. The center point of this termination is connected to ground to improve the balance between the P and M side. The values of the terminations between the transformers and on the secondary side have to be chosen to get an effective 50 Ω (in the case of 50-Ω source impedance).

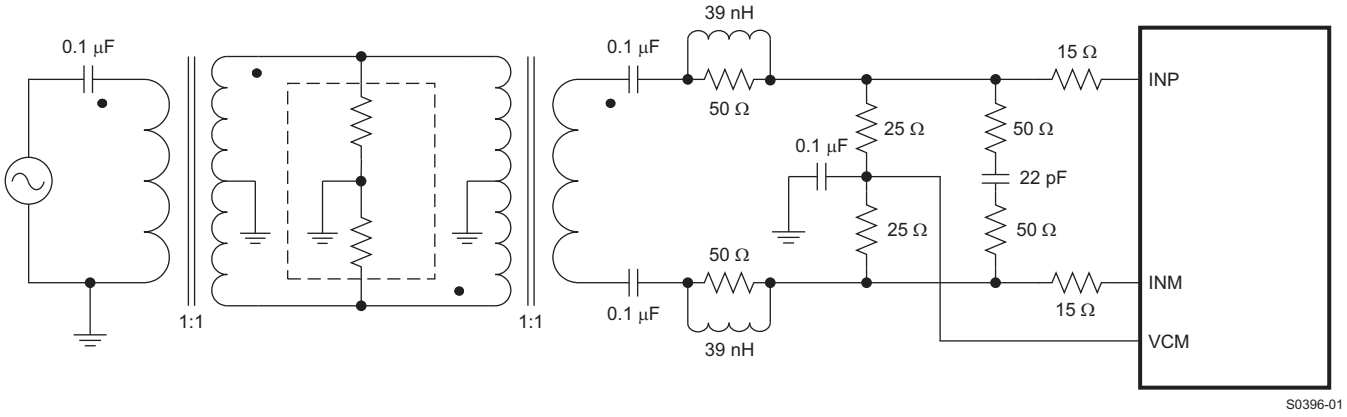


Figure 102. Drive Circuit With Low Bandwidth (for low input frequencies)

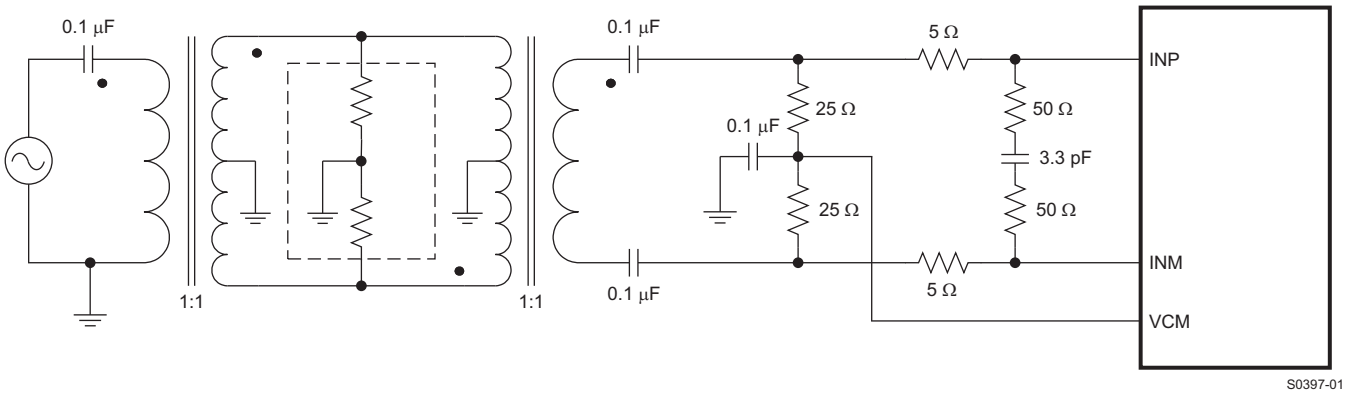


Figure 103. Drive Circuit With High Bandwidth (for high input frequencies)

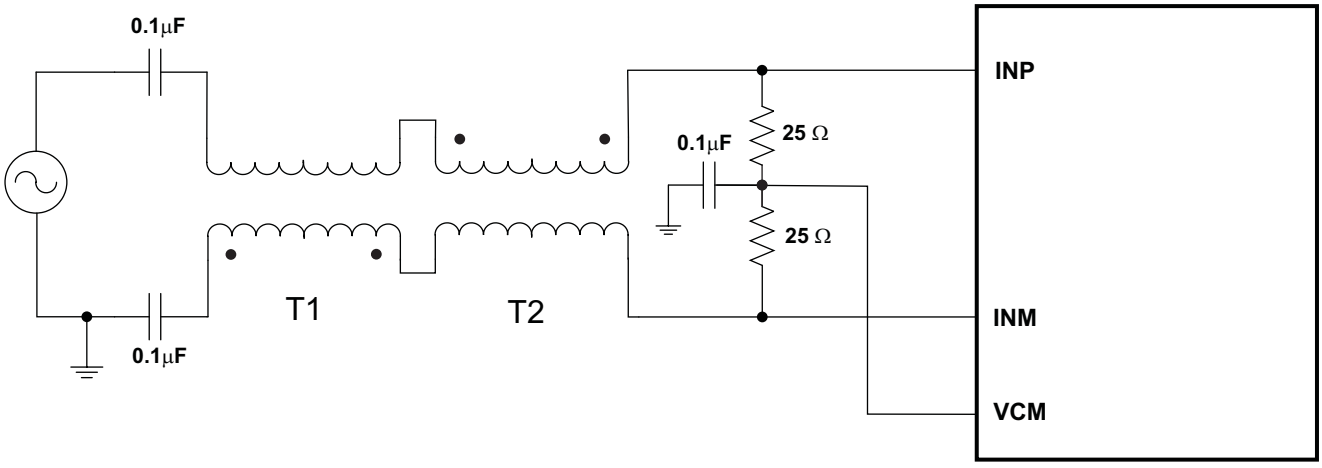


Figure 104. Drive Circuit with Very High Bandwidth (> 300 MHz)

All these examples show 1:1 transformers being used with a 50-Ω source. As explained in the “Drive Circuit Requirements”, this helps to present a low source impedance to absorb the sampling glitches. With a 1:4 transformer, the source impedance will be 200 ohms. The higher impedance can lead to degradation in performance, compared to the case with 1:1 transformers.

For applications where only a band of frequencies are used, the drive circuit can be tuned to present a low impedance for the sampling glitches. Figure 105shows an example with 1:4 transformer, tuned for a band around 150 MHz.

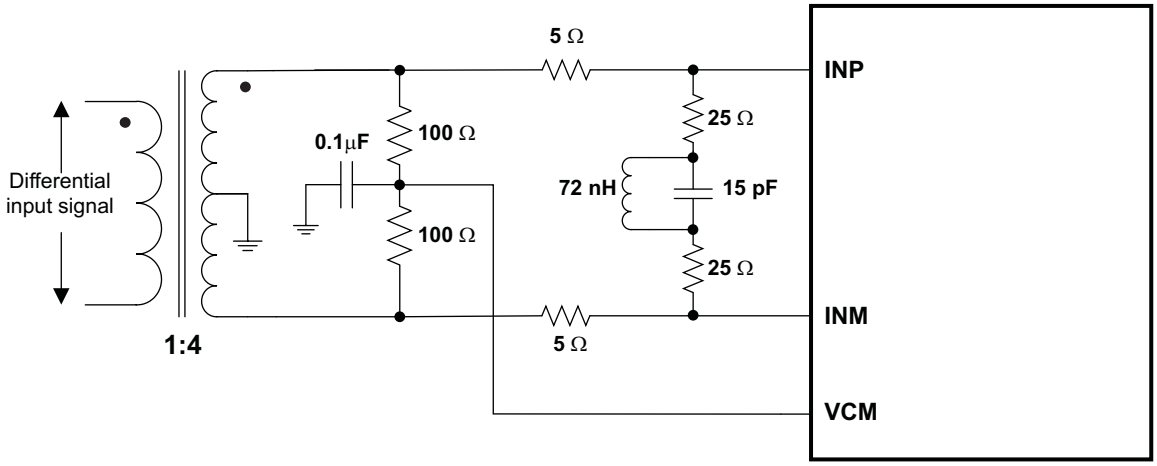


Figure 105. Drive Circuit with 1:4 Transformer

Input Common-Mode

To ensure a low-noise common-mode reference, the VCM pin is filtered with a 0.1μF low-inductance capacitor connected to ground. The VCM pin is designed to directly drive the ADC inputs. The input stage of the ADC sinks a common-mode current in the order of 3.6μA / MSPS (about 900μA at 250 MSPS).

REFERENCE

The ADS62Px9/x8 has built-in internal references REFP and REFM, requiring no external components. Design schemes are used to linearize the converter load seen by the references; this and the on-chip integration of the requisite reference capacitors eliminates the need for external decoupling. The full-scale input range of the converter can be controlled in the external reference mode as explained below. The internal or external reference modes can be selected by programming the serial interface register bit **<REF>**.

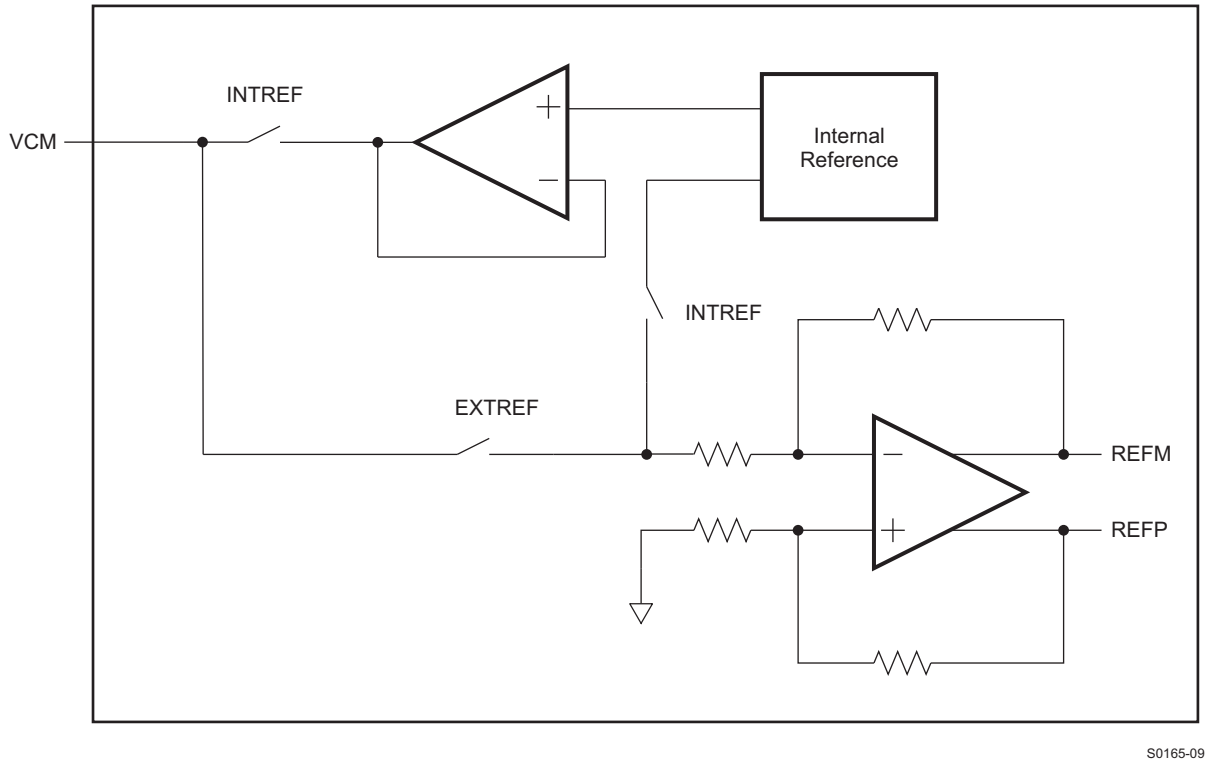


Figure 106. Reference Section

Internal Reference

When the device is in internal reference mode, the REFP and REFM voltages are generated internally. Common-mode voltage (1.5V nominal) is output on VCM pin, which can be used to externally bias the analog input pins.

External Reference

When the device is in external reference mode, the VCM acts as a reference input pin. The voltage forced on the VCM pin is buffered and gained by 1.33 internally, generating the REFP and REFM voltages. The differential input voltage corresponding to full-scale is given by the following:

Full-scale differential input pp = (Voltage forced on VCM) × 1.33

In this mode, the 1.5V common-mode voltage to bias the input pins has to be generated externally.

CLOCK INPUT

The ADS62Px9/x8 clock inputs can be driven differentially (sine, LVPECL or LVDS) or single-ended (LVCMOS), with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to VCM using internal 5-kΩ resistors as shown in Figure 107. This allows using transformer-coupled drive circuits for sine wave clock or ac-coupling for LVPECL, LVDS clock sources (Figure 108, Figure 109, and Figure 110).

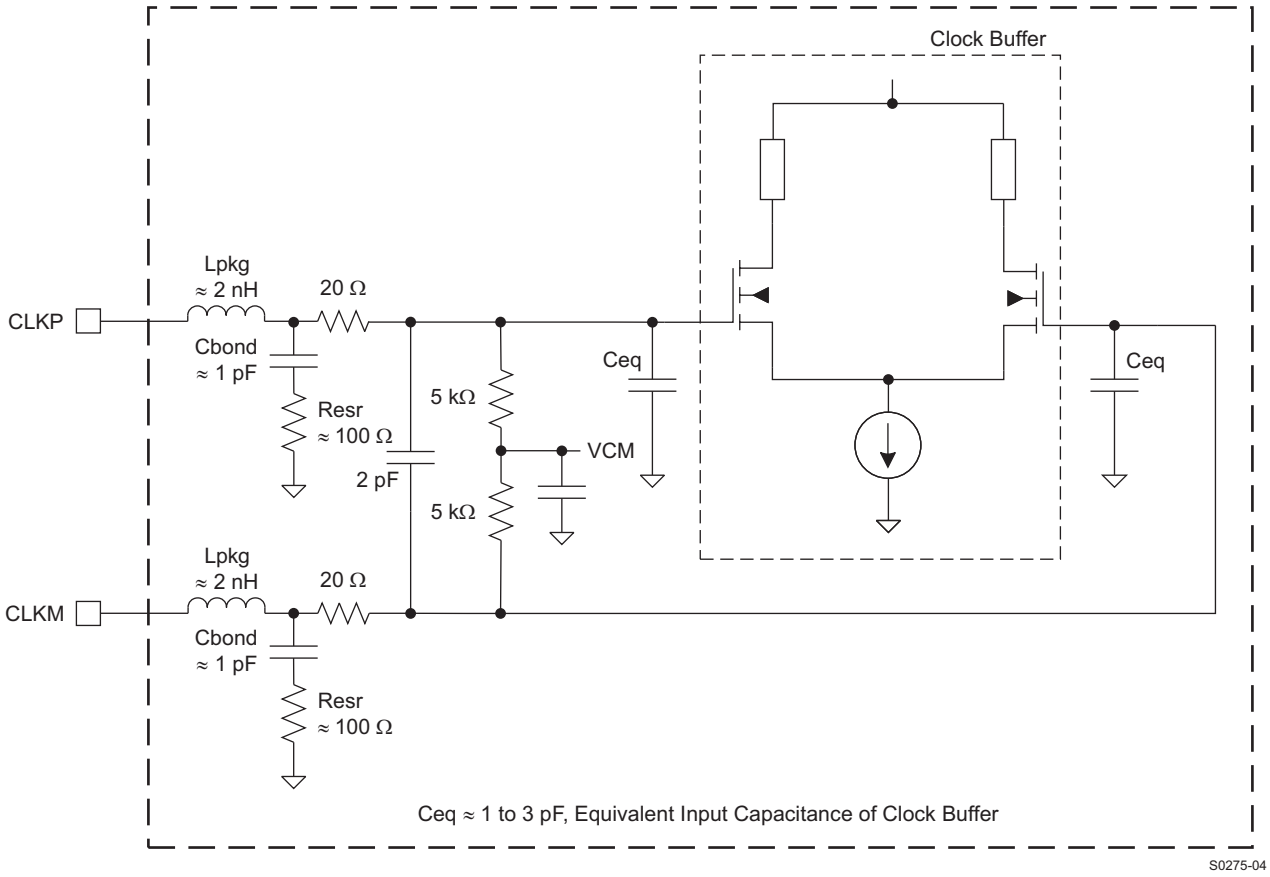


Figure 107. Internal Clock Buffer

Single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM (pin 11) connected to ground with a 0.1-μF capacitor, as shown in Figure 111.

For best performance, the clock inputs have to be driven differentially, reducing susceptibility to common-mode noise. For high input frequency sampling, it is recommended to use a clock source with very low jitter. Bandpass filtering of the clock source can help reduce the effect of jitter. There is no change in performance with a non-50% duty cycle clock input.

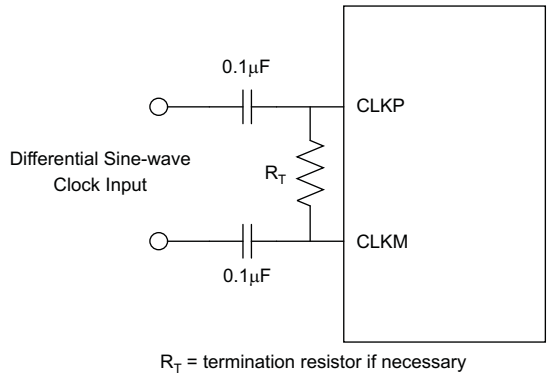


Figure 108. Differential Sine-Wave Clock Driving Circuit

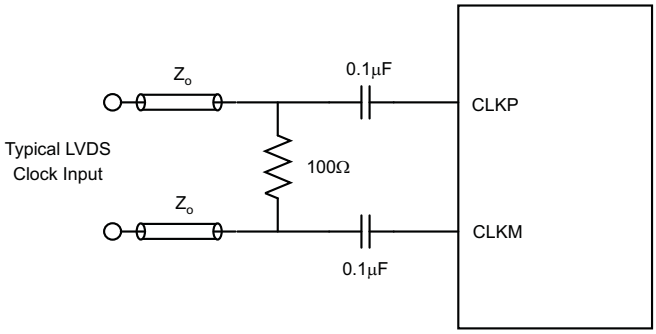


Figure 109. Typical LVDS Clock Driving Circuit

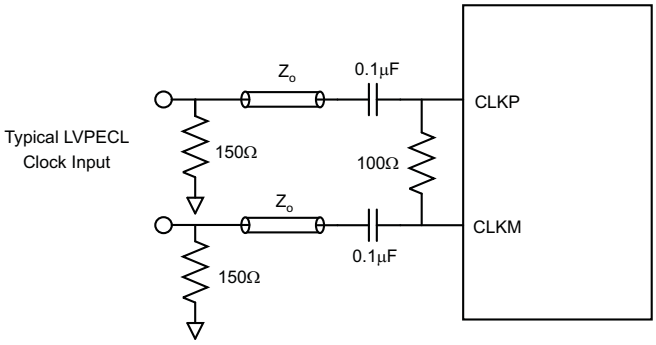


Figure 110. Typical LVPECL Clock Driving Circuit

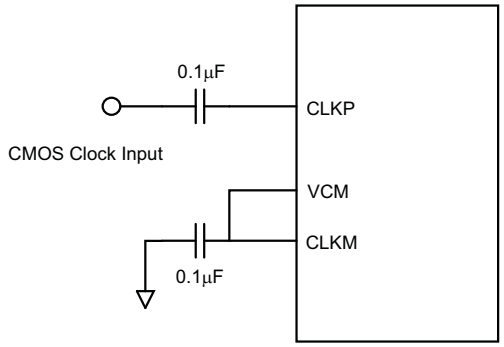


Figure 111. Typical LVCMOS Clock Driving Circuit

GAIN PROGRAMMABILITY

The ADS62Px9/x8 includes gain settings that can be used to get improved SFDR performance (compared to no gain). The gain is programmable from 0dB to 6dB (in 0.5 dB steps). For each gain setting, the analog input full-scale range scales proportionally, as shown in Table 9.

The SFDR improvement is achieved at the expense of SNR; for each 1dB gain step, the SNR degrades about 1dB. The SNR degradation is less at high input frequencies. As a result, the gain is very useful at high input frequencies as the SFDR improvement is significant with marginal degradation in SNR.

So, the gain can be used to trade-off between SFDR and SNR. Note that the default gain after reset is 0dB.

Table 9. Full-Scale Range Across Gains

GAIN, dB	TYPE	FULL-SCALE, Vpp
0	Default after reset	2 V
1	Fine, programmable	1.78
2		1.59
3		1.42
4		1.26
5		1.12
6		1.00

OFFSET CORRECTION

The ADS62Px9/x8 has an internal offset correction algorithm that estimates and corrects dc offset up to ±10mV. The correction can be enabled using the serial register bit **<ENABLE OFFSET CORRECTION>**. Once enabled, the algorithm estimates the channel offset and applies the correction every clock cycle. The time constant of the correction loop is a function of the sampling clock frequency. The time constant can be controlled using register bits **<OFFSET CORR TIME CONSTANT>** as described in Table 10.

After the offset is estimated, the correction can be frozen by setting **<ENABLE OFFSET CORRECTION>** back to 0.

Once frozen, the last estimated value is used for offset correction every clock cycle. The correction does not affect the phase of the signal. Note that offset correction is disabled by default after reset.

Figure 112 shows the time response of the offset correction algorithm, after it is enabled.

Table 10. Time Constant of Offset Correction Algorithm

<OFFSET CORR TIME CONSTANT> D3-D0	TIME CONSTANT (TC_{CLK}), NUMBER OF CLOCK CYCLES	TIME CONSTANT, sec (=TC_{CLK} × 1/Fs) (1)
0000	256 k	1 ms
0001	512 k	2 ms

(1) Sampling frequency, Fs = 250 MSPS

Table 10. Time Constant of Offset Correction Algorithm (continued)

<OFFSET CORR TIME CONSTANT> D3-D0	TIME CONSTANT (TC_{CLK}), NUMBER OF CLOCK CYCLES	TIME CONSTANT, sec (=TC_{CLK} × 1/Fs) (1)
0010	1 M	4 ms
0011	2 M	8 ms
0100	4 M	17 ms
0101	8 M	33 ms
0110	16 M	67 ms
0111	32 M	134 ms
1000	64 M	268 ms
1001	128 M	536 ms
1010	256 M	1.1 s
1011	512 M	2.2 s
1100	RESERVED	
1101	RESERVED	
1110	RESERVED	
1111	RESERVED	

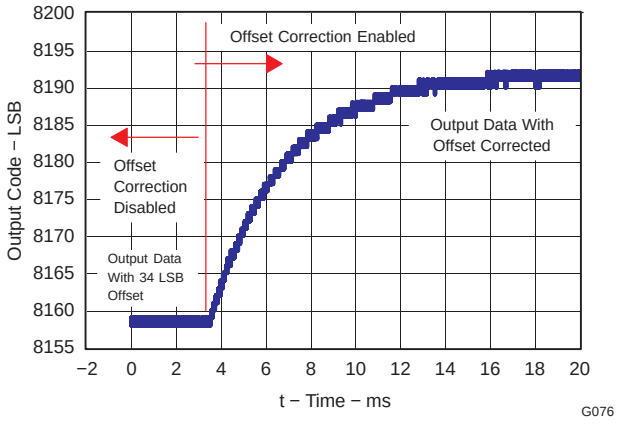


Figure 112. Time Response of Offset Correction

POWER DOWN

The ADS62Px9/x8 has two power down modes – global power down and individual channel standby. These can be set using either the serial register bits or using the control pins CTRL1 to CTRL3.

POWER DOWN MODES	CONFIGURE USING				WAKE-UP TIME
	SERIAL INTERFACE	PARALLEL CONTROL PINS			
Normal operation	**<POWER DOWN MODES>** = 0000	*low*	*low*	*low*	–
Output buffer disabled for channel B	**<POWER DOWN MODES>** = 1001	Not Available			–
Output buffer disabled for channel A	**<POWER DOWN MODES>** = 1010	Not Available			–
Output buffer disabled for channel A and B	**<POWER DOWN MODES>** = 1011	Not Available			–
Global power down	**<POWER DOWN MODES>** = 1100	*high*	*low*	*low*	Slow (30 µs)
Channel B standby	**<POWER DOWN MODES>** = 1101	*high*	*low*	*high*	Fast (1 µs)
Channel A standby	**<POWER DOWN MODES>** = 1110	*high*	*high*	*low*	Fast (1 µs)

POWER DOWN MODES	CONFIGURE USING				WAKE-UP TIME
	SERIAL INTERFACE	PARALLEL CONTROL PINS			
Multiplexed (MUX) mode – Output data of channel A and B is multiplexed and available on ***DA13 to DA0*** pins.(1)	**<POWER DOWN MODES>** = 1111	*high*	*high*	*high*	–

(1) Low Speed mode has to be enabled for Multiplexed Output mode (MUX mode). Therefore, MUX mode works with serial interface configuration only and is not supported with parallel configuration.

Global Power Down

In this mode, the entire chip including both the A/D converters, internal reference and the output buffers are powered down resulting in reduced total power dissipation of about 45 mW. The output buffers are in high impedance state. The wake-up time from the global power down to data becoming valid in normal mode is typically 30μs.

Channel Standby

Here, each channel's A/D converter can be powered down. The internal references are active, resulting in quick wake-up time of 1 μs. The total power dissipation in standby is about 475 mW.

Input Clock Stop

In addition to the above, the converter enters a low-power mode when the input clock frequency falls below 1 MSPS. The power dissipation is about 275 mW.

POWER SUPPLY SEQUENCE

During power-up, the AVDD and DRVDD supplies can come up in any sequence. The two supplies are separated in the device. Externally, they can be driven from separate supplies or from a single supply.

DIGITAL OUTPUT INFORMATION

The ADS62Px9/x8 provides 14-bit/12-bit data and an output clock synchronized with the data.

Output Interface

Two output interface options are available – Double Data Rate (DDR) LVDS and parallel CMOS. They can be selected using the serial interface register bit <LVDS_CMOS> or using DFS pin in parallel configuration mode.

DDR LVDS Outputs

In this mode, the data bits and clock are output using LVDS (Low Voltage Differential Signal) levels. Two data bits are multiplexed and output on each LVDS differential pair.

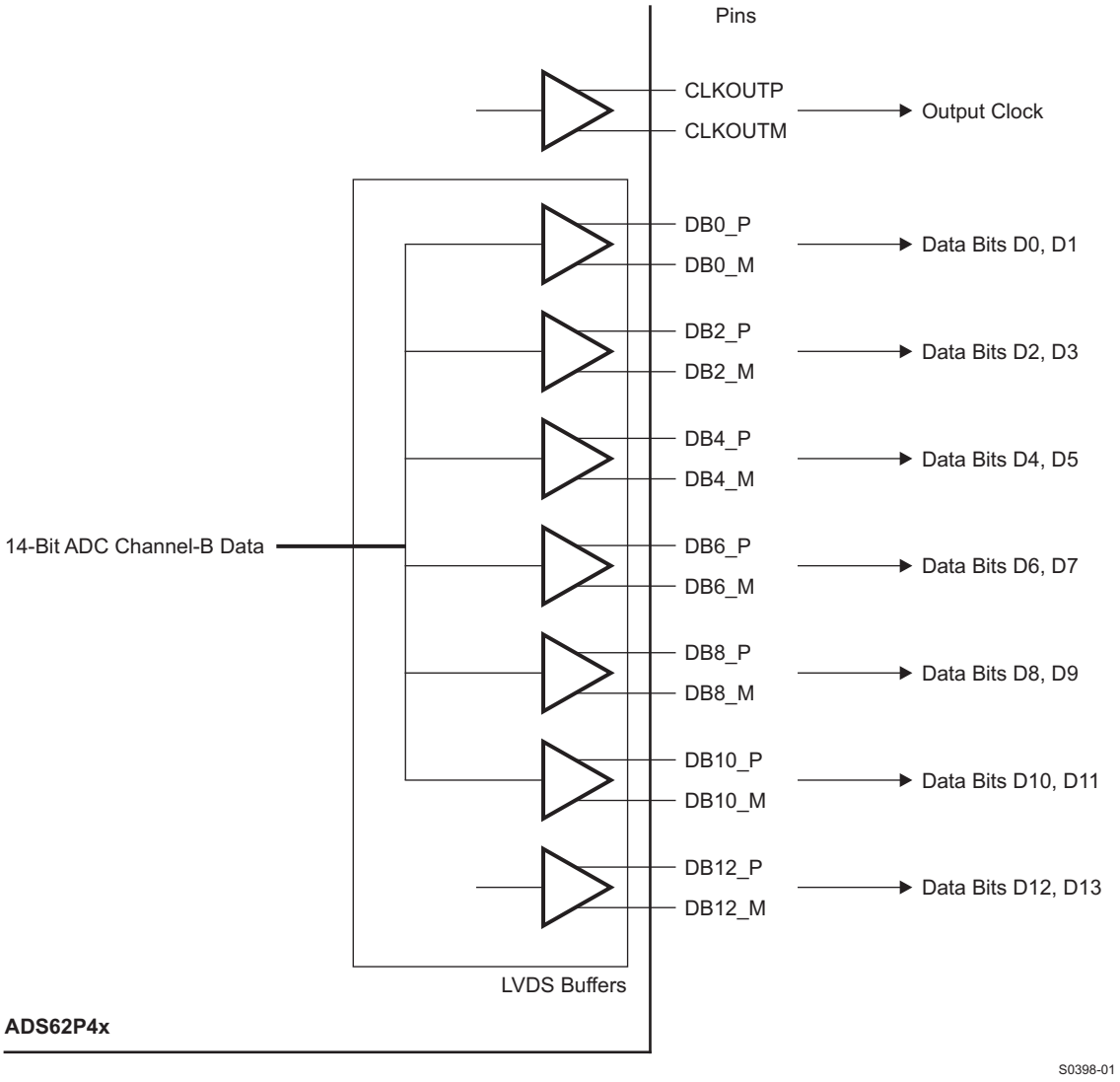


Figure 113. LVDS Outputs

Even data bits D0, D2, D4… are output at the rising edge of CLKOUTP and the odd data bits D1, D3, D5… are output at the falling edge of CLKOUTP. Both the rising and falling edges of CLKOUTP have to be used to capture all the data bits (see Figure 114).

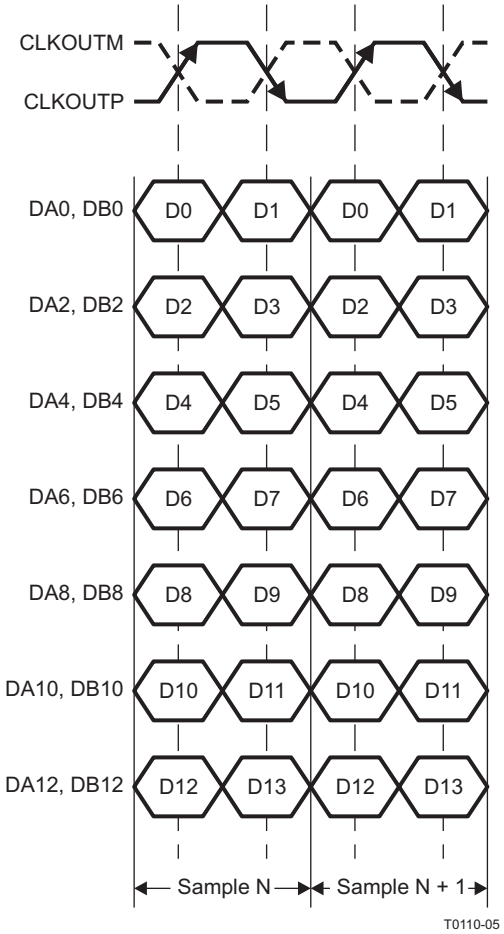


Figure 114. DDR LVDS Interface

LVDS Buffer

The equivalent circuit of each LVDS output buffer is shown in Figure 115. The buffer is designed to present an output impedance of 100 Ω (Rout). The differential outputs can be terminated at the receive end by a 100-Ω termination.

The buffer output impedance behaves like a source-side series termination. By absorbing reflections from the receiver end, it helps to improve signal integrity. Note that this internal termination cannot be disabled and its value cannot be changed.

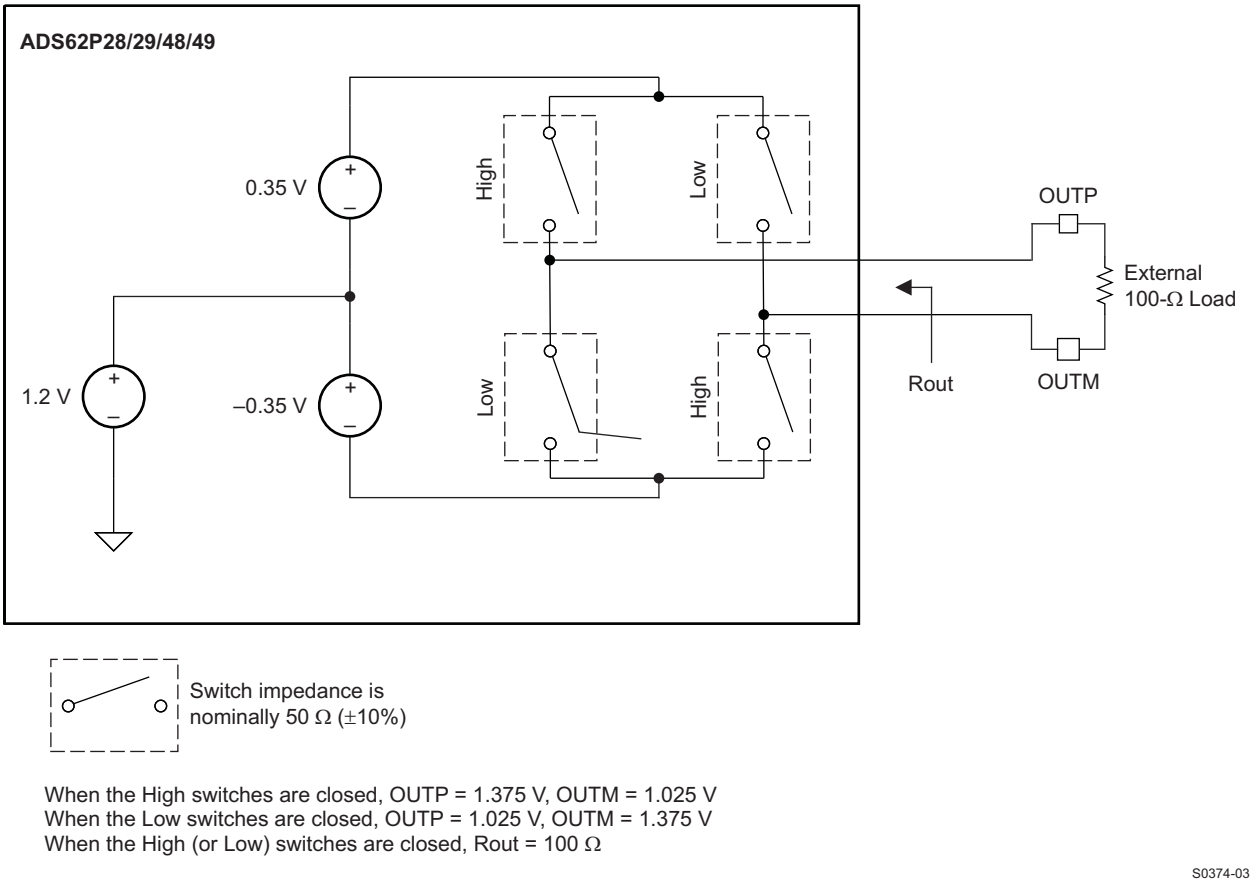


Figure 115. LVDS Buffer Equivalent Circuit

Parallel CMOS Interface

In CMOS mode, each data bit is output on a separate pin as a CMOS voltage level, every clock cycle. This mode is recommended only up to 210 MSPS, beyond which the CMOS data outputs do not have sufficient time to settle to valid logic levels.

For sampling frequencies up to 150 MSPS, the rising edge of the output clock CLKOUT can be used to latch data in the receiver. The setup and hold timings of the output data with respect to CLKOUT are specified in the timing specification table up to 150 MSPS.

For sampling frequencies above 150 MSPS, it is recommended to use an external clock to capture data. The delay from input clock to output data and the data valid times are specified up to 210 MSPS. These timings can be used to delay the input clock appropriately and use it to capture the data.

When using the CMOS interface, it is important to minimize the load capacitance seen by data and clock output pins by using short traces on the board.

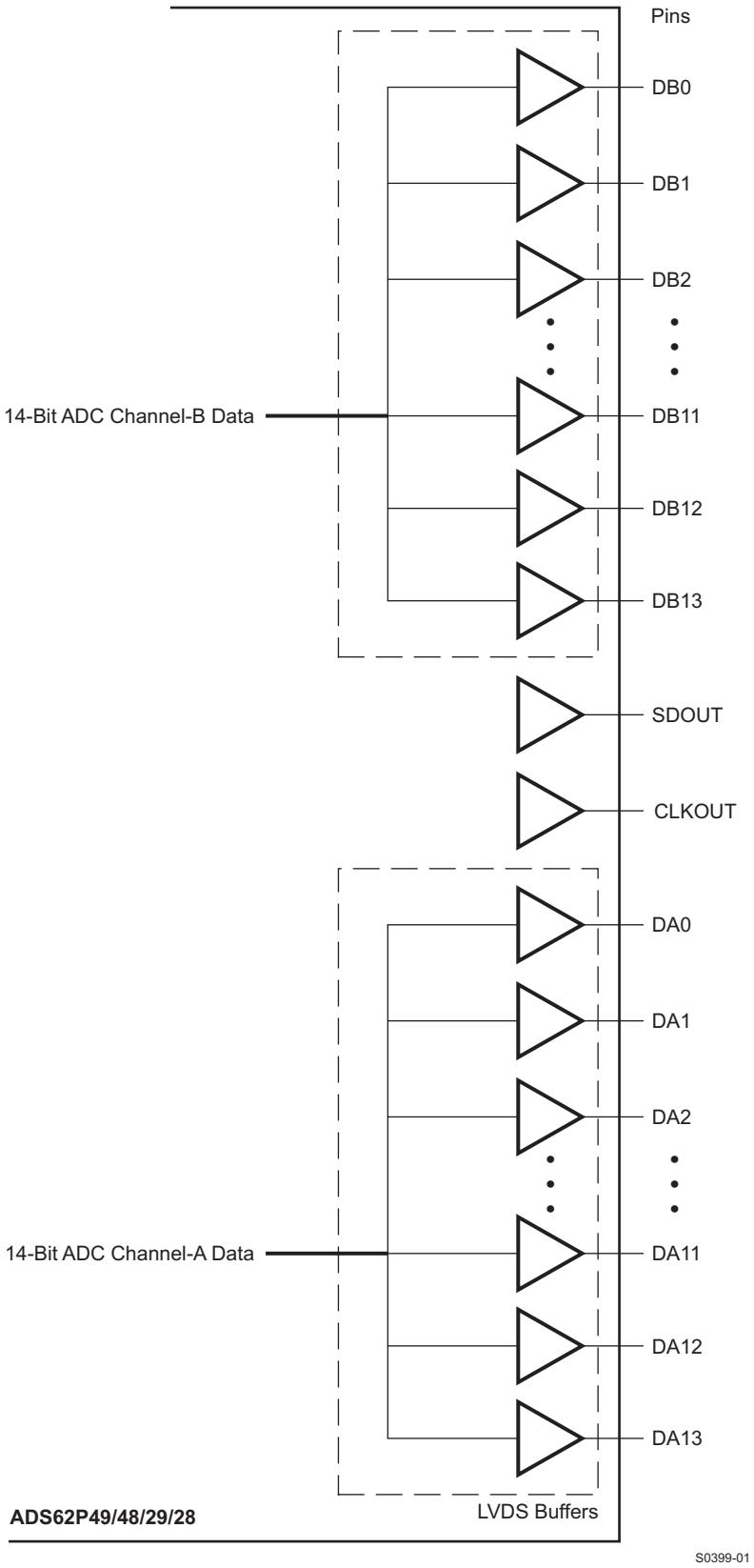


Figure 116. CMOS Outputs

CMOS Interface Power Dissipation

With CMOS outputs, the DRVDD current scales with the sampling frequency and the load capacitance on every output pin. The maximum DRVDD current occurs when each output bit toggles between 0 and 1 every clock cycle. In actual applications, this condition is unlikely to occur. The actual DRVDD current would be determined by the average number of output bits switching, which is a function of the sampling frequency and the nature of the analog input signal.

Digital current due to CMOS output switching = $C_L \times DRVDD \times (N \times F_{AVG})$,

where

C_L = load capacitance,

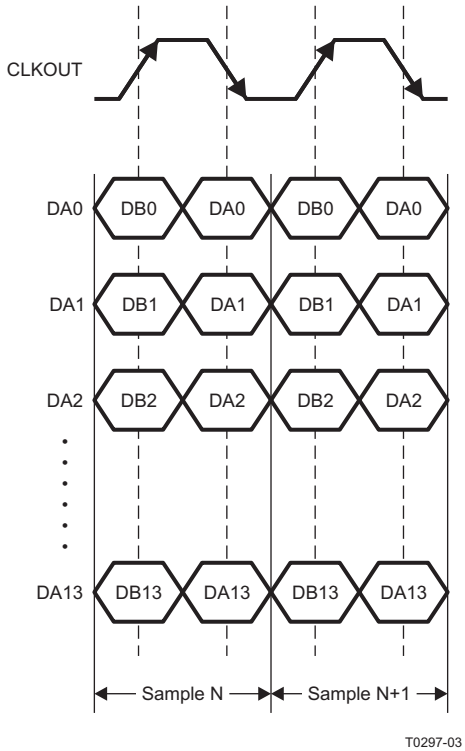
$N \times F_{AVG}$ = average number of output bits switching.

Figure 92 shows the current with various load capacitances across sampling frequencies at 2.5-MHz analog input frequency

Multiplexed Output Mode (only with CMOS interface)

In this mode, the digital outputs of both channels are multiplexed and output on a single bus (DA0-DA13 pins). Channel B data bits are output at the rising edge of CLKOUT, and channel A data bits are output at the falling edge of CLKOUT. The channel B output data pins (DB0-DB13) are 3-stated (see Figure 117 for details). Since the output data rate on the DA bus is effectively doubled, this mode is recommended only for low sampling frequencies (<65MSPS).

Low Speed mode has to be enabled for Multiplexed Output Mode (MUX mode). Therefore, MUX mode works with serial interface configuration only and is not supported with parallel configuration. This mode can be enabled using register bits **<POWER DOWN MODES>** or using the parallel pins CTRL1-3.



NOTES: 1. Both channel outputs are output on the channel A output data lines.

2. Channel A outputs are output on the falling edges whereas channel B outputs are output on the rising edges of the output clock.

Figure 117. Multiplexed Output Mode Timing

Output Data Format

Two output data formats are supported – 2s complement and offset binary. They can be selected using the serial interface register bit **<DATA FORMAT>** or controlling the DFS pin in parallel configuration mode.

In the event of an input voltage overdrive, the digital outputs go to the appropriate full scale level. For a positive overdrive, the output code is 0x3FFF in offset binary output format, and 0x1FFF in 2s complement output format. For a negative input overdrive, the output code is 0x0000 in offset binary output format and 0x2000 in 2s complement output format.

BOARD DESIGN CONSIDERATIONS

Grounding

A single ground plane is sufficient to give good performance, provided the analog, digital, and clock sections of the board are cleanly partitioned. See the EVM User Guide (SLAU237) for details on layout and grounding.

Supply Decoupling

As ADS62Px9/x8 already includes internal decoupling, minimal external decoupling can be used without loss in performance. Note that decoupling capacitors can help filter external power supply noise, so the optimum number of capacitors would depend on the actual application. The decoupling capacitors should be placed very close to the converter supply pins.

Exposed Pad

In addition to providing a path for heat dissipation, the pad is also electrically connected to digital ground internally. So, it is necessary to solder the exposed pad to the ground plane for best thermal and electrical performance. For detailed information, see application notes *QFN Layout Guidelines* (SLOA122) and *QFN/SON PCB Attachment* (SLUA271).

DEFINITION OF SPECIFICATIONS

Analog Bandwidth – The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low frequency value.

Aperture Delay – The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs. This delay will be different across channels. The maximum variation is specified as aperture delay variation (channel-channel).

Aperture Uncertainty (Jitter) – The sample-to-sample variation in aperture delay.

Clock Pulse Width/Duty Cycle – The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

Maximum Conversion Rate – The maximum sampling rate at which certified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate – The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL) – An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

Integral Nonlinearity (INL) – The INL is the deviation of the ADC's transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

Gain Error – Gain error is the deviation of the ADC's actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range. Gain error has two components: error due to reference inaccuracy and error due to the channel. Both these errors are specified independently as E_{GREF} and E_{GCHAN}.

To a first order approximation, the total gain error will be $E_{TOTAL} \sim E_{GREF} + E_{GCHAN}$.

For example, if $E_{TOTAL} = \pm 0.5\%$, the full-scale input varies from $(1\text{-}0.5/100) \times FS_{ideal}$ to $(1 + 0.5/100) \times FS_{ideal}$.

Offset Error – The offset error is the difference, given in number of LSBs, between the ADC's actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into mV.

Temperature Drift – The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from T_{MIN} to T_{MAX}. It is calculated by dividing the maximum deviation of the parameter across the T_{MIN} to T_{MAX} range by the difference $T_{MAX}–T_{MIN}$.

Signal-to-Noise Ratio – SNR is the ratio of the power of the fundamental (PS) to the noise floor power (PN), excluding the power at DC and the first nine harmonics.

$$SNR = 10Log^{10} \frac{P_S}{P_N} \quad (1)$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Signal-to-Noise and Distortion (SINAD) – SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$SINAD = 10Log^{10} \frac{P_S}{P_N + P_D} \quad (2)$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Effective Number of Bits (ENOB) – The ENOB is a measure of the converter performance as compared to the theoretical limit based on quantization noise.

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02} \tag{3}$$

Total Harmonic Distortion (THD) – THD is the ratio of the power of the fundamental (P_S) to the power of the first nine harmonics (PD).

$$\text{THD} = 10\text{Log}^{10}\ \frac{P_S}{P_N} \tag{4}$$

THD is typically given in units of dBc (dB to carrier).

Spurious-Free Dynamic Range (SFDR) – The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion – IMD3 is the ratio of the power of the fundamental (at frequencies f1 and f2) to the power of the worst spectral component at either frequency 2f1–f2 or 2f2–f1. IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

DC Power Supply Rejection Ratio (DC PSRR) – The DC PSSR is the ratio of the change in offset error to a change in analog supply voltage. The DC PSRR is typically given in units of mV/V.

AC Power Supply Rejection Ratio (AC PSRR) – AC PSRR is the measure of rejection of variations in the supply voltage by the ADC. If ΔV_{SUP} is the change in supply voltage and ΔVout is the resultant change of the ADC output code (referred to the input), then

$$\text{PSRR} = 20\text{Log}^{10}\ \frac{\Delta V_{OUT}}{\Delta V_{SUP}}\ \text{(Expressed in dBc)} \tag{5}$$

Voltage Overload Recovery – The number of clock cycles taken to recover to less than 1% error after an overload on the analog inputs. This is tested by separately applying a sine wave signal with 6dB positive and negative overload. The deviation of the first few samples after the overload (from their expected values) is noted.

Common Mode Rejection Ratio (CMRR) – CMRR is the measure of rejection of variation in the analog input common-mode by the ADC. If ΔVcm_in is the change in the common-mode voltage of the input pins and ΔV_{OUT} is the resultant change of the ADC output code (referred to the input), then

$$\text{CMRR} = 20\text{Log}^{10}\ \frac{\Delta V_{OUT}}{\Delta V_{CM}}\ \text{(Expressed in dBc)} \tag{6}$$

Cross-Talk (only for multi-channel ADC)– This is a measure of the internal coupling of a signal from adjacent channel into the channel of interest. It is specified separately for coupling from the immediate neighboring channel (near-channel) and for coupling from channel across the package (far-channel). It is usually measured by applying a full-scale signal in the adjacent channel. Cross-talk is the ratio of the power of the coupling signal (as measured at the output of the channel of interest) to the power of the signal applied at the adjacent channel input. It is typically expressed in dBc.

REVISION HISTORY

Changes from Original (April 2009) to Revision A **Page**

- Changed ADS62P48, ADS62P29, ADS62P28 from product preview to production data 4
- Added Analog supply current max value of 320 mA 7
- Added Output buffer supply current, LVDS interface max value of 165 mA 7
- Added Analog power max value of 1.05 W 7
- Added Digital power, LVDS interface max value of 0.3 W 7
- Added SNR Signal to noise ratio,LVDS, Fin = 170 MHz, 0 dB gain min value of 68 dBFS 8
- Added SINADSignal to noise and distortion ratio, LVDS, Fin = 170 MHz, 0 dB gain min value of 66.5 dBFS 8
- Added SNR Signal to noise ratio,LVDS, Fin = 170 MHz, 0 dB gain min value of 66.5 dBFS 8
- Added SNR Signal to noise ratio,LVDS, Fin = 170 MHz, 0 dB gain min value of 66.5 dBFS 8
- Added SINADSignal to noise and distortion ratio, LVDS, Fin = 170 MHz, 0 dB gain min value of 66 dBFS 8
- Added SINADSignal to noise and distortion ratio, LVDS, Fin = 170 MHz, 0 dB gain min value of 66 dBFS 8
- Added DNL Differential non-linearity min value of –0.9 LSB 8
- Added DNL Differential non-linearity max value of 1.3 LSB 8
- Added DNL Differential non-linearity min value of –0.9 LSB 8
- Added DNL Differential non-linearity max value of 1.3 LSB 8
- Added INL Integrated non-linearity min value of –5 LSB 8
- Added INL Integrated non-linearity max value of 5 LSB 8
- Added INL Integrated non-linearity min value of –5 LSB 8
- Added INL Integrated non-linearity max value of 5 LSB 8
- Added SFDR Spurious Free Dynamic Range, Fin = 170 MHz min value of 71 dBc 9
- Added SFDRSpurious Free Dynamic Range, excluding HD2,HD3, Fin = 170 MHz min value of 78 dBc 9
- Added HD2 Second Harmonic Distortion, Fin = 170 MHz min value of 71 dBc 9
- Added HD3 Third Harmonic Distortion, Fin = 170 MHz min value of 71 dBc 9
- Added THDTotal harmonic distortion, Fin = 170 MHz min value of 70.5 dBc 9
- Added IMD2-Tone Inter-modulation Distortion, F1 = 46 MHz, F2 = 50 MHz, each tone at –7 dBFS typ value of 91 dBFS 9

Changes from Revision A (June 2009) to Revision B **Page**

- Changed Voltage between AVDD to DRVDD in ABSOLUTE MAXIMUM RATINGS 4
- Changed Voltage between DRVDD to AVDD in ABSOLUTE MAXIMUM RATINGS 4
- Added new thermal table 6
- Added table note 2 6
- Added table notes 5 and 6 and Figure 3 6
- Changed Sine wave, ac-coupled, TYP from 3 to 1.5 V_{PP} 6
- Added Figure 3 6
- Changed Digital Characteristics - ADS62Px9/x8 table note 2 10
- Added table note to Timing Requirements table in row t_{OE} 12
- Added table note 1 to Table 2 and Table 3 12
- Added for Fs ≤ 80 to Table 2 and Table 3 12
- Changed To put the device in parallel configuration mode, keep RESET tied to ***high*** (AVDD). to To put the device in parallel configuration mode, keep RESET tied to ***high*** (AVDD or DRVDD). in PARALLEL CONFIGURATION ONLY section 15
- Changed Table 4 15

- Deleted 2 in Table 5 15
- Changed Table 6 16
- Added note to Table 7 and changed rows to Not available 16
- Changed sampling frequency from 100 MSPS to 80 MSPS in serial register 20 22
- Added 00 and 10 to D6-D5 of serial register 3F 22
- Added reference to the Multiplexed Output Mode section in the APPLICATION INFORMATION 22
- Changed Serial register 44 description 23
- Added Figure 12 24
- Added Figure 13 24
- Added information to serial register 62 D2-D0 test patterns 27
- Added Figure 14 28
- Added Figure 15 29
- Added Figure 16 30
- Added information to serial register 75 D2-D0 test patterns 33
- Changed DRVDD to AVDD in Pin Assignments (LVDS MODE) pin 15 description 37
- Added to Pin Assignments (LVDS MODE) pin 37 description 37
- Deleted true from DA and DB descriptions in Pin Assignments (LVDS MODE) 37
- Changed SDATA to SCLK in Pin Assignments (CMOS MODE) pin 12 description 40
- Changed DRVDD to AVDD in Pin Assignments (CMOS MODE) pin 15 description 40
- Added to Pin Assignments (CMOS MODE) pin 37 description 40
- Changed CMSO mode CLKOUT pin number from 5 to 57 40
- Changed Figure 96 55
- Changed Figure 98 56
- Changed Figure 108 63
- Changed Figure 109 63
- Added Figure 110 63
- Added Figure 111 63
- Changed Power Down Modes table and added note 65
- Changed Figure 115 69
- Added Multiplexed Output Mode (only with CMOS interface) section information 71

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS62P28IRGCR	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ62P28
ADS62P28IRGCR.A	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ62P28
ADS62P28IRGCT	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ62P28
ADS62P28IRGCT.A	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ62P28
ADS62P29IRGCR	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ62P29
ADS62P29IRGCR.A	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ62P29
ADS62P29IRGCT	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ62P29
ADS62P29IRGCT.A	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ62P29
ADS62P48IRGCR	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ62P48
ADS62P48IRGCR.A	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ62P48
ADS62P48IRGCT	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ62P48
ADS62P48IRGCT.A	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ62P48
ADS62P49IRGCR	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ62P49
ADS62P49IRGCR.A	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ62P49
ADS62P49IRGCT	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ62P49
ADS62P49IRGCT.A	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ62P49

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

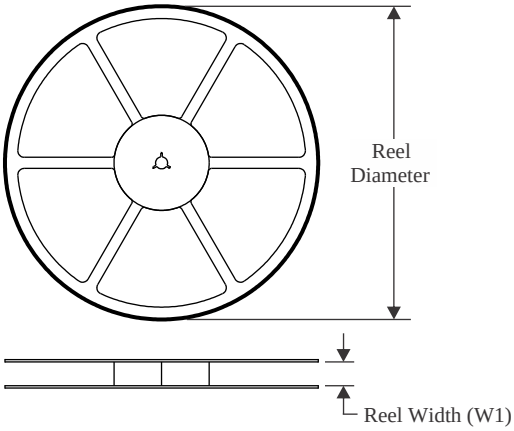
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

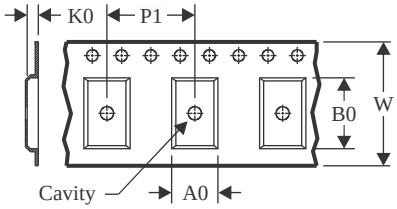
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

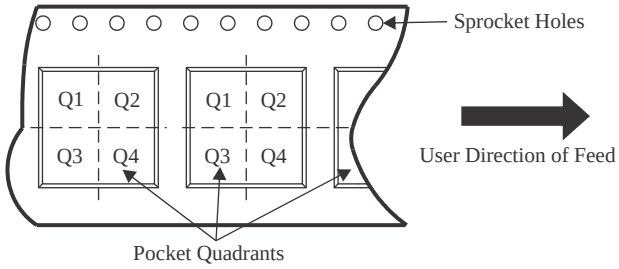


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

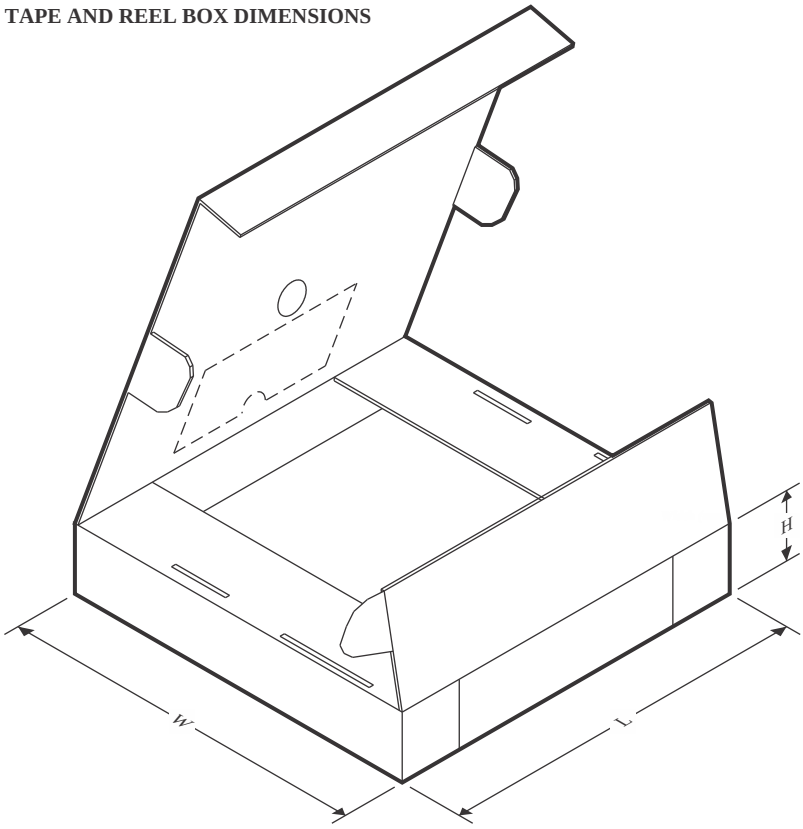
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS62P28IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADS62P29IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADS62P48IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADS62P49IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS62P28IRGCR	VQFN	RGC	64	2000	350.0	350.0	43.0
ADS62P29IRGCR	VQFN	RGC	64	2000	350.0	350.0	43.0
ADS62P48IRGCR	VQFN	RGC	64	2000	350.0	350.0	43.0
ADS62P49IRGCR	VQFN	RGC	64	2000	350.0	350.0	43.0

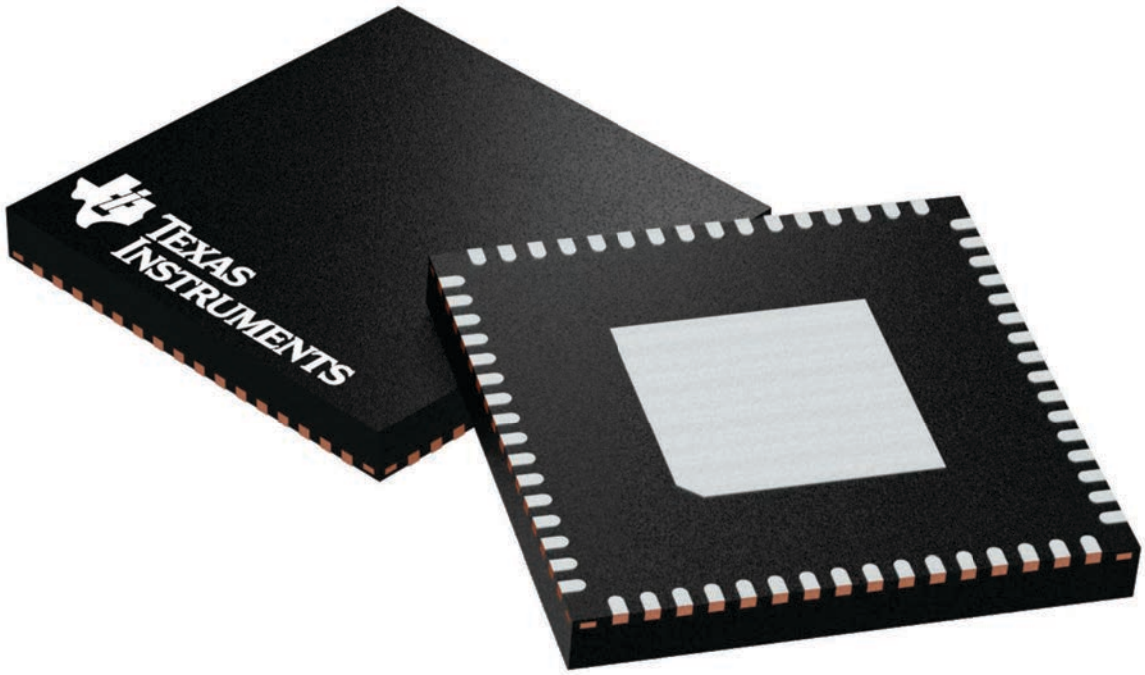
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

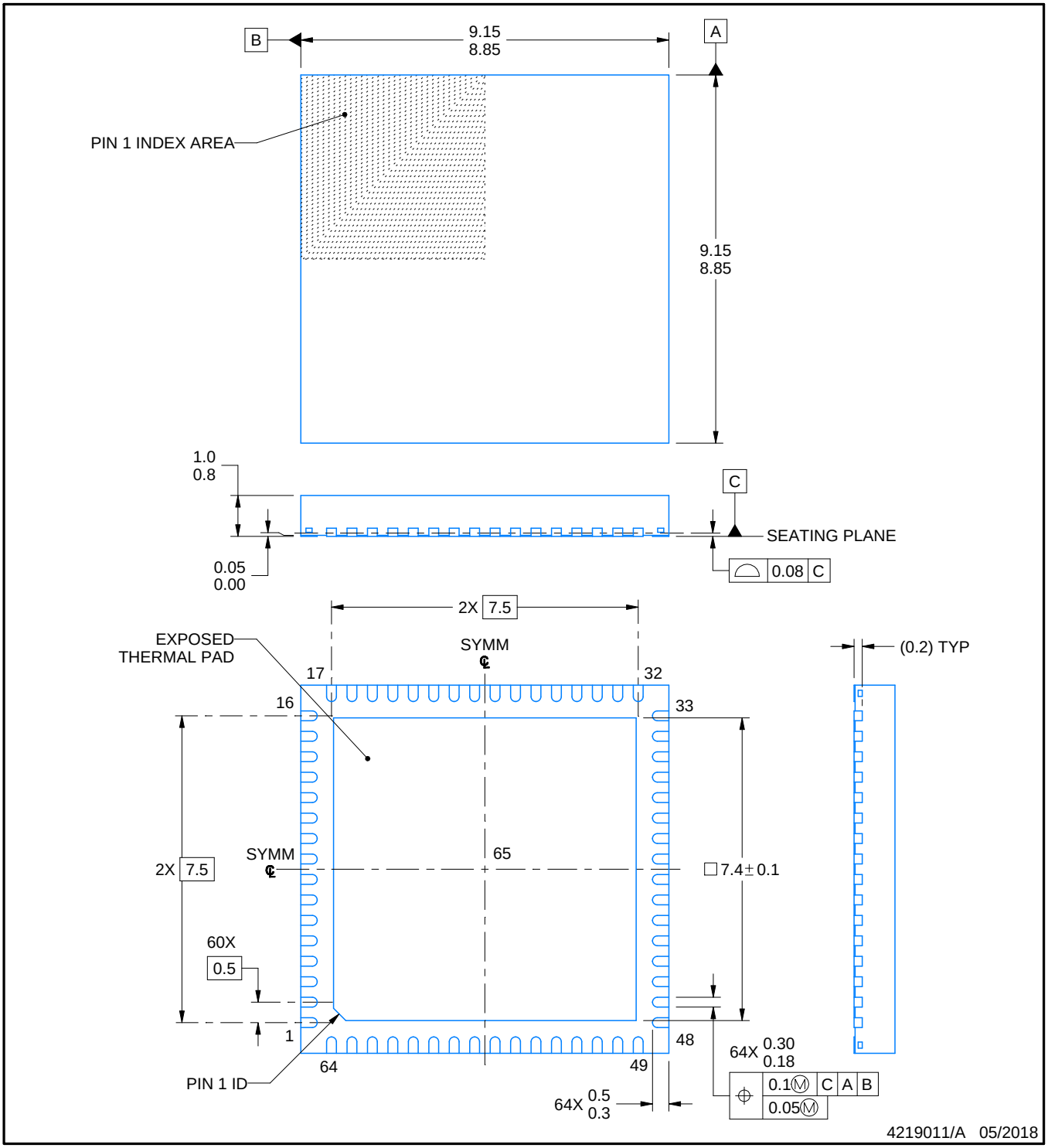
4224597/A

RGC0064H

PACKAGE OUTLINE

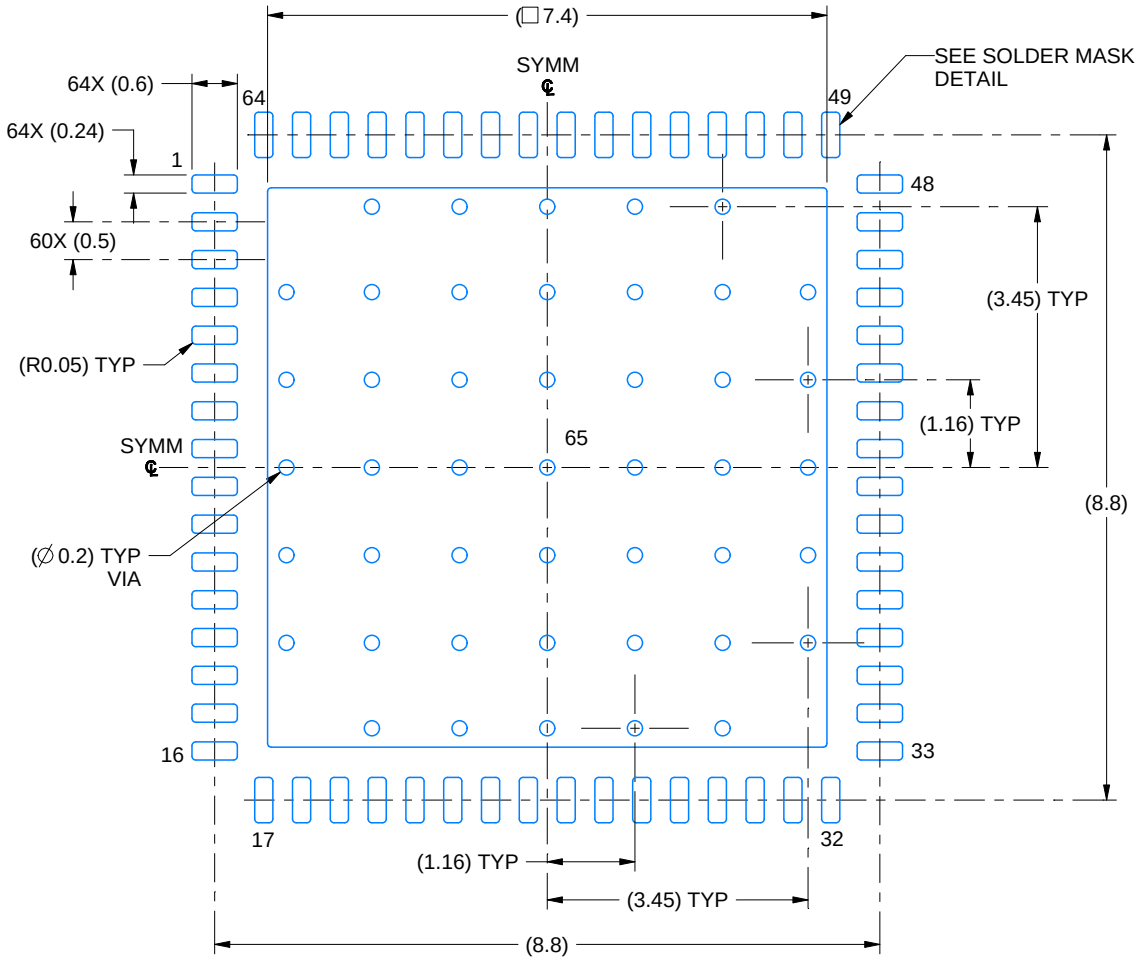
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

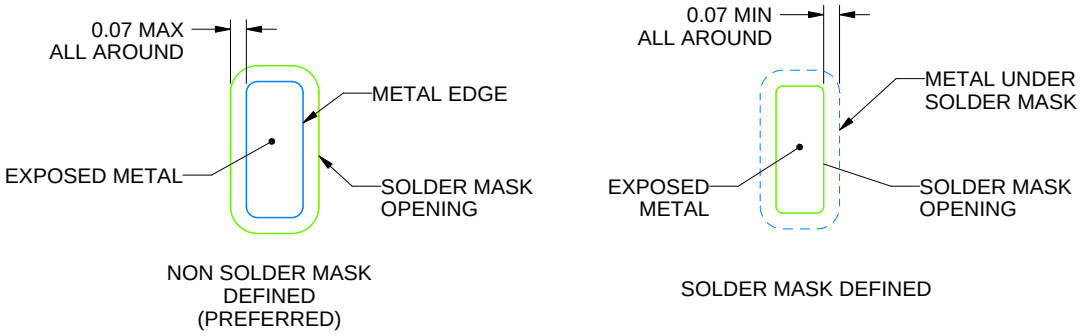


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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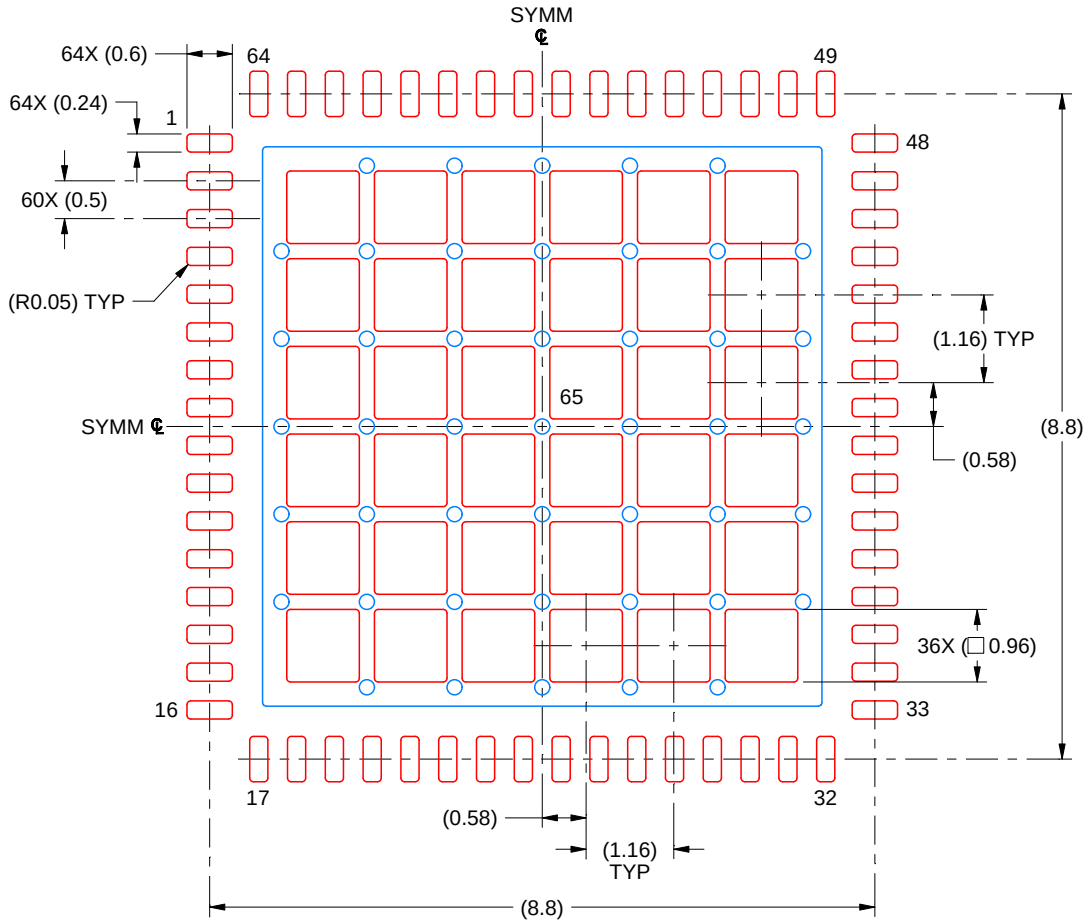
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
61% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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