www.ti.com

14-/12-Bit, 250-MSPS ADCs With Integrated Analog Buffer

FEATURES

- Integrated High Impedance Analog Input Buffer
- Maximum Sample Rate: 250 MSPS
- 14-Bit Resolution ADS61B49
- 12-Bit Resolution ADS61B29
- 790 mW Total Power Dissipation at 250 MSPS
- Double Data Rate (DDR) LVDS and Parallel CMOS Output Options
- Programmable Fine Gain up to 6 dB for SNR/SFDR Trade-Off and 1-V_{pp} Full-Scale Operation
- DC Offset Correction
- Supports Input Clock Amplitude Down to 400 mV_{PP} Differential
- 48-QFN Package (7mm × 7mm)
- Pin Compatible with ADS6149 Family

APPLICATIONS

- Multicarrier, Wide Bandwidth Communications
- Wireless Multi-Carrier Communications Infrastructure
- Software Defined Radio
- Power Amplifier Linearization Feedback ADC
- 802.16d/e
- Test and Measurement Instrumentation
- High Definition Video
- Medical Imaging
- Radar Systems

DESCRIPTION

The ADS61B49 (ADS61B29) is a 14-bit (12-bit) A/D converter with a sampling rate up to 250 MSPS. It combines high dynamic performance and low power consumption in a compact 48-QFN package. An integrated analog buffer makes it well-suited for multi-carrier, wide bandwidth communications applications. The buffer maintains constant performance and input impedance across a wide frequency range.

The ADS61B49 (ADS61B29) has fine gain options that can be used to improve SFDR performance at lower full-scale input ranges. It includes a dc offset correction loop that can be used to cancel the ADC offset. Both Double Data Rate (DDR) LVDS and parallel CMOS digital output interfaces are available. At lower sampling rates, the ADC automatically operates at scaled down power with no loss in performance.

It includes internal references while the traditional reference pins and associated decoupling capacitors have been eliminated. The device is specified over the industrial temperature range (-40°C to 85°C).

	ANALOG BUFFER	250 MSPS	210 MSPS
ADS614X	NO	ADS6149	ADS6148
14-Bit Family	YES	ADS61B49	
ADS612X	NO	ADS6129	ADS6128
12-Bit Family	YES	ADS61B29	



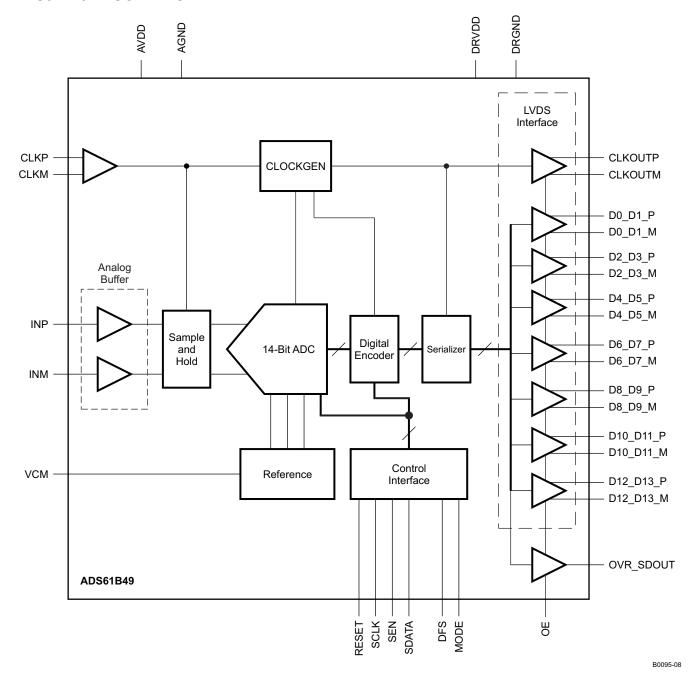
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





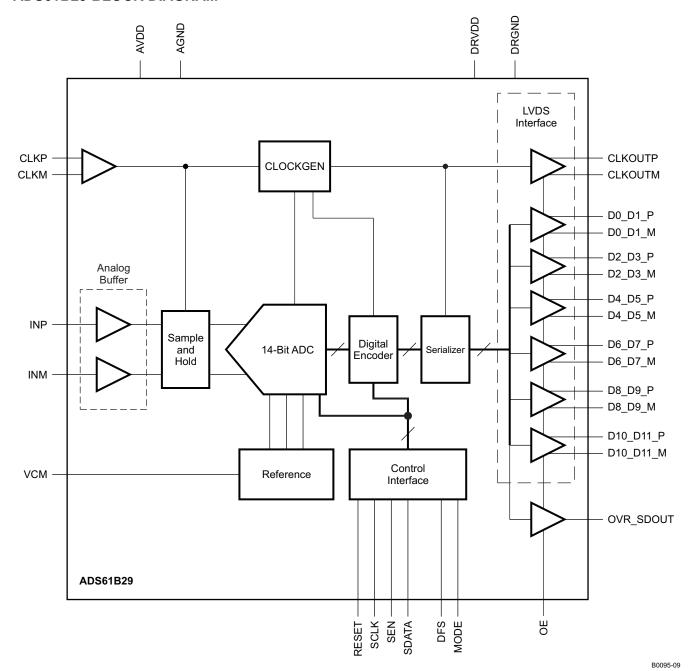
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ADS61B49 BLOCK DIAGRAM





ADS61B29 BLOCK DIAGRAM





PACKAGE/ORDERING INFORMATION(1)(2)

PRODUCT	PACKAGE- LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	LEAD/BALL FINISH	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS61B49	QFN-48	RGZ	–40°C to 85°C	Cu NiPdAu	AZ61B49	ADS61B49IRGZR	Tape and reel
AD301B49	QFN-48	NOZ	-40 C to 65 C	Cu NiFuAu	A201B49	ADS61B49IRGZT	rape and reer
ADS61B29	QFN-48	RGZ	–40°C to 85°C	Cu NiPdAu	AZ61B29	ADS61B29IRGZR	Tape and reel
AD301B29	QFIN-46	RGZ	-40 C to 65 C	Cu NiFuAu	AZOTBZ9	ADS61B29IRGZT	Tape and reel

- For thermal pad size on the package, see the mechanical drawings at the end of this data sheet. θ_{JA} = 25.41° C/W (0LFM air flow), θ_{JC} = 16.5° C/W when used with 2oz. copper trace and pad soldered directly to a JEDEC standard four layer 3 in x 3 in (7.62 cm x 7.62 cm) PCB.
- For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
	Supply Voltage, AVDD	-0.3 to 3.9	V
	Supply Voltage, DRVDD	-0.3 to 2.2	V
	Voltage between AGND and DRGND	-0.3 to 0.3	V
	Voltage between AVDD to DRVDD (when AVDD leads DRVDD)	0 to 3.3	V
	Voltage between DRVDD to AVDD (when DRVDD leads AVDD)	-1.5 to 1.8	V
	Voltage applied to analog input pins - INP, INM	-0.3 to minimum (3.6, AVDD + 0.3)	V
	Voltage applied to input pins - CLKP, CLKM ⁽²⁾ , RESET, SCLK, SDATA, SEN, DFS and MODE	-0.3 to (AVDD + 0.3)	V
T _A	Operating free-air temperature range	-40 to 85	°C
T_{J}	Max Operating junction temperature	125	°C
T _{stg}	Storage temperature range	-65 to 150	°C

⁽¹⁾ Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
SUPPLIE	S					
AVDD	Analog supply voltage		3	3.3	3.6	V
DRVDD	Digital supply voltage		1.7	1.8	1.9	V
ANALOG	INPUTS		•		•	
	Differential input voltage range			2		V_{pp}
	Input common-mode voltage (different t	han ADS6149 family)		2.3 ±0.1		V
	Maximum analog input frequency with 2	PVpp input amplitude ⁽¹⁾		500		MHz
	Maximum analog input frequency with 1	Vpp input amplitude(1)		800		MHz
CLOCK I	NPUT		•		•	
	Input clock sample rate		1		250	MSPS
		Sine wave, ac-coupled	0.3	1.5		
	Input clock amplitude differential	LVPECL, ac-coupled		1.6		V_{pp}
	(V _{CLKP} -V _{CLKM})	LVDS, ac-coupled		0.7		
		LVCMOS, single-ended, ac-coupled		3.3		V

See the Theory of Operations in the applications section.

Submit Documentation Feedback

When AVDD is turned off, it is recommended to switch off the input clock (or ensure the voltage on CLKP, CLKM is < 0.3V.) This prevents the ESD protection diodes at the clock input pins from turning on.



RECOMMENDED OPERATING CONDITIONS (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
	Input clock duty cycle	40%	50%	60%	
DIGITA	L OUTPUTS			,	
C_L	Maximum external load capacitance from each output pin to DRGND		5		pF
R_L	Differential load resistance between the LVDS output pairs (LVDS mode)		100		Ω
T _A	Operating free-air temperature	-40		85	°C



ELECTRICAL CHARACTERISTICS - ADS61B49 and ADS61B29

Typical values are at 25° C, AVDD = 3.3 V, DRVDD = 1.8 V, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode unless otherwise noted.

Min and max values are across the full temperature range $T_{MIN} = -40$ °C to $T_{MAX} = 85$ °C, AVDD = 3.3 V, DRVDD = 1.8 V

	PARAMETER		49/ADS6 0 MSPS	1B29	UNIT
		MIN	TYP	MAX	
ANALOG	INPUT			<u> </u>	
	Differential input voltage range		2		V_{PP}
	Differential input resistance (at dc), See Figure 62		10		kΩ
	Differential input capacitance, See Figure 63		2		pF
	Analog input bandwidth		750		MHz
	Analog Input common-mode current (per input pin)		2		μΑ
	VCM common-mode output voltage (different than ADS6149 family)		2.3		V
	VCM output current capability		±4		mA
DC ACCU	RACY			<u> </u>	
	Offset error	-15	±2	+15	mV
	Temperature coefficient of offset error		0.005		mV/°C
	Variation of offset error with supply		0.3		mV/V
E _{GREF}	Gain error due to internal reference inaccuracy alone	-2.5	±0.2	+2.5	%FS
E _{GCHAN}	Gain error of channel alone		0.2		%FS
	Temperature coefficient of EGCHAN		.001		Δ%/°C
POWER S	UPPLY	Ų.			
I _{AVDD}	Analog supply current		200		mA
	Output buffer supply current, LVDS interface with 100-Ω external termination		70		mA
I_{DRVDD}	Output buffer supply current, CMOS interface F _{in} = 3 MHz, 10-pF external load capacitance		56		mA
	Analog power		660	730	mW
	Digital power LVDS interface		130	160	mW
	Digital power CMOS interface, F _{in} = 3 MHz, 10-pF external load capacitance		101		mW
	Global power down		20	75	mW
	Standby		120		mW



ELECTRICAL CHARACTERISTICS – ADS61B49 and ADS61B29

Typical values are at 25° C, AVDD = 3.3 V, DRVDD = 1.8 V, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode unless otherwise noted.

Min and max values are across the full temperature range $T_{MIN} = -40$ °C to $T_{MAX} = 85$ °C, AVDD = 3.3 V, DRVDD = 1.8 V

PARAM	ETER		S61B4 0 MSP			S61B2 MSP	-	UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
	F _{in} = 20 MHz		72.3			70.1		
OND	F _{in} = 80 MHz		72			69.8		
SNR Signal-to-noise ratio, LVDS	F _{in} = 100 MHz		71.6			69.6		dBFS
3	F _{in} = 170 MHz	68.5	70.7		66.5	69		
	F _{in} = 300 MHz		69			67.8		
	F _{in} = 20 MHz		72.5			70.3		
	F _{in} = 80 MHz		71.8			69.7		
SINAD Signal-to-noise and distortion ratio, LVDS	F _{in} = 100 MHz		71.6			69.5		dBFS
original to Holos and distortion ratio, 2120	F _{in} = 170 MHz	67.5	70		65.7	68.4		
	F _{in} = 300 MHz		67.1			66.3		
ENOB Effective number of bits	F _{in} = 170 MHz (using SINAD in dBFS)		11.3			11.1		LSB
DNL Differential non-linearity		-0.95	±0.4	1	-0.5	±0.2	1	LSB
INL Integrated non-linearity		-5	±2	5	-2.5	±1	2.5	LSB



ELECTRICAL CHARACTERISTICS – ADS61B49 and ADS61B29

Typical values are at 25° C, AVDD = 3.3 V, DRVDD = 1.8 V, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode unless otherwise noted.

Min and max values are across the full temperature range $T_{MIN} = -40$ °C to $T_{MAX} = 85$ °C, AVDD = 3.3 V, DRVDD = 1.8 V

	PARAMETER	ADS61B 25	49/ADS6 0 MSPS	1B29	UNIT
		MIN	TYP	MAX	
	F _{in} = 20 MHz		92		
	F _{in} = 80 MHz				
SFDR	F _{in} = 100 MHz		86		dBc
Spurious free dynamic range	F _{in} = 170 MHz (all spurs/harmonics)	74	84		ubc
	F _{in} = 170 MHz (excluding 2nd harmonic)	77	87		
	F _{in} = 300 MHz		76		
	F _{in} = 20 MHz		89		
	F _{in} = 80 MHz		83		
THD Total harmonic distortion	F _{in} = 100 MHz		82		dBc
Total Harmonic distortion	F _{in} = 170 MHz	72	79		
	F _{in} = 300 MHz		73		
	F _{in} = 20 MHz		94		
HD2,	F _{in} = 80 MHz		90		
•	F _{in} = 100 MHz		88		dBc
ID2, second harmonic distortion	F _{in} = 170 MHz	74	84		
	F _{in} = 300 MHz		76		
	F _{in} = 20 MHz		93		
	F _{in} = 80 MHz		86		
HD3 Third harmonic distortion	F _{in} = 100 MHz		85		dBc
Third Harmonic distortion	F _{in} = 170 MHz	77	87		
	F _{in} = 300 MHz		76		
	F _{in} = 20 MHz		96		
	F _{in} = 80 MHz		94		
Worst Spur	F _{in} = 100 MHz		94		dBc
Other than second, third harmonics	F _{in} = 170 MHz	80	92		
	F _{in} = 300 MHz		90		
IMD	F1 = 46 MHz, F2 = 50 MHz, Each tone at –7 dBFS		94		4DE0
2-tone inter-modulation distortion	F1 = 185 MHz, F2 = 190 MHz, Each tone at –7 dBFS		90		dBFS
Input overload recovery	Recovery to within 1% (of final value) for 6-dB overload with sine wave input		1		Clock Cycles
PSRR AC power supply rejection ratio	For 100-mV _{pp} signal on AVDD supply		25		dB

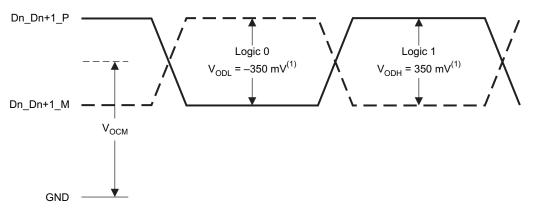


DIGITAL CHARACTERISTICS – ADS61B49 and ADS61B29

The DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1. AVDD = 3.3 V, DRVDD = 1.8 V

DADAM	ETED	TEST SOMBITIONS	ADS6	B49/ADS6	1B29	LINUT	
PARAM	IETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
DIGITAL INPUTS - RES	SET, SCLK, SDATA,	SEN ⁽¹⁾			1.		
High-level input voltage		All digital inputs support 1.8-V and 3.3-V CMOS	1.3			V	
Low-level input voltage		logic levels			0.4	V	
SDATA, SCLK ⁽²⁾		V _{High} = 3.3 V		16			
High-level input current	SEN ⁽³⁾	V _{High} = 3.3 V		10		μΑ	
Lave laved Samuel arrowant	SDATA, SCLK	V _{Low} = 0 V		0		^	
Low-level input current SEN		V _{Low} = 0 V		-20		μΑ	
Input capacitance	1			4		pF	
DIGITAL OUTPUTS - C	MOS INTERFACE (F	Pins D0 to D13 and OVR_SDOUT)			1		
High-level output voltage	9	with I _{OH} = 1mA	DRVDD -0.1	DRVDD		V	
Low-level output voltage		with I _{OL} = 1mA		0	0.1	V	
Output capacitance (inte	rnal to device)			2		pF	
DIGITAL OUTPUTS - L	VDS INTERFACE (P	ins D0_D1_P/M to D12_D13_P/M) ⁽⁴⁾					
V _{ODH} , High-level output	voltage ⁽⁵⁾		275	350	425	mV	
V _{ODL} , Low-level output v	roltage ⁽⁵⁾		-425	-350	-275	mV	
V _{OCM} , Common-mode o	utput voltage	Capacitance inside the device, from either output to ground	1	1.2	1.3	V	
Output capacitance				2		pF	

- 1) SCLK, SDATA, SEN function as digital input pins in serial configuration mode.
- (2) SDATA, SCLK have internal 200-kΩ pull-down resistor.
- (3) SEN has internal 100-kΩ pull-up resistor to AVDD.
- (4) OVR_SDOUT has CMOS output logic levels, determined by DRVDD voltage.
- (5) With external 100-Ω termination



T0399-01

Figure 1. LVDS Voltage Levels



TIMING REQUIREMENTS – LVDS AND CMOS MODES(1)

Typical values are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, sampling frequency = 250 MSPS, sine wave input clock, C_{LOAD} = 5 pF⁽²⁾, R_{LOAD} = 100 $\Omega^{(3)}$, Low Speed mode disabled, unless otherwise noted.

Min and max values are across the full temperature range $T_{MIN} = -40$ °C to $T_{MAX} = 85$ °C, AVDD = 3.3 V, DRVDD = 1.7 V to 1.9 V.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _a	Aperture delay		0.7	1.2	1.7	ns
t _j	Aperture jitter			170		fs rms
		Time to valid data after coming out of STANDBY mode		0.3	1	
	Wake-up time	Time to valid data after coming out of PDN GLOBAL mode		25	100	μs
		Time to valid data after stopping and restarting the input clock		10		Clock Cycles
	ADC Latency ⁽⁴⁾	Default, after reset		18		Clock Cycles
DDR LVD	S MODE (5)					
t _{su}	Data setup time	Data valid ⁽⁶⁾ to zero-crossing of CLKOUTP	0.8	1.2		ns
t _h	Data hold time	Zero-crossing of CLKOUT to data becoming invalid (6)	0.25	0.6		ns
t _{PDI}	Clock propagation delay	Input clock rising edge cross-over to output clock rising edge cross-over	0.2 ×	t _s + t _{del}	ay	ns
	t _{delay}	100 MSPS ≤ Sampling frequency ≤ 250 MSPS	5	6.2	7.5	ns
	LVDS bit clock duty cycle	Duty cycle of differential clock, (CLKOUTP–CLKOUTM) 100 MSPS ≤ Sampling frequency ≤ 250 MSPS		52%		
t _{RISE} , t _{FALL}	Data rise time, Data fall time	Rise time measured from −100 mV to 100 mV Fall time measured from 100 mV to −100 mV 1 MSPS ≤ Sampling frequency ≤ 250 MSPS	0.08	0.14	0.2	ns
t _{CLKRISE} , t _{CLKFALL}	Output clock rise time, Output clock fall time	Rise time measured from −100 mV to 100 mV Fall time measured from 100 mV to −100 mV 1 MSPS ≤ Sampling frequency ≤ 250 MSPS	0.08	0.14	0.2	ns
t _{OE}	Output enable (OE) to data delay	Time to valid data after OE becomes active		40		ns
PARALLE	L CMOS MODE ⁽⁷⁾					
t _{START}	Input clock to data delay	Input clock rising edge cross-over to start of data valid (8)			3.2	ns
t _{DV}	Data valid time	Time interval of valid data ⁽⁸⁾	0.7	1.5		ns
t _{PDI}	Clock propagation delay	Input clock rising edge cross-over to output clock rising edge cross-over	0.78	× t _s + t _{de}	elay	ns
	t _{delay}	100 MSPS ≤ Sampling frequency ≤ 150 MSPS	5	6.5	8	ns
	Output clock duty cycle	Duty cycle of differential clock, (CLKOUT) 100 MSPS ≤ Sampling frequency ≤ 150 MSPS		50%		
t _{RISE} , t _{FALL}	Data rise time, Data fall time	Rise time measured from 20% to 80% of DRVDD, Fall time measured from 80% to 20% of DRVDD, 1 MSPS ≤ Sampling frequency ≤ 250 MSPS	0.7	1.2	2	ns
t _{CLKRISE} , t _{CLKFALL}	Output clock rise time, Output clock fall time	Rise time measured from 20% to 80% of DRVDD, Fall time measured from 80% to 20% of DRVDD, 1 MSPS ≤ Sampling frequency ≤ 150 MSPS	0.5	1	1.5	ns
t _{OE}	Output enable (OE) to data delay	Time to valid data after OE becomes active		20		ns
		l .	1			

- Timing parameters are specified by design and characterization and not tested in production.
- C_{LOAD} is the effective external single-ended load capacitance between each output pin and ground R_{LOAD} is the differential load resistance between the LVDS output pair.
- At higher frequencies, t_{PDI} is greater than one clock period and overall latency = ADC latency + 1.
- Measurements are done with a transmission line of $100-\Omega$ characteristic impedance between the device and the load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.
- Data valid refers to logic high of +100 mV and logic low of -100 mV.
- For F_s > 150 MSPS, it is recommended to use external clock for data capture and NOT the device output clock signal (CLKOUT).
- Data valid refers to logic high of 1.26 V and logic low of 0.54 V.

Product Folder Link(s): ADS61B29 ADS61B49



LVDS Timings at Lower Sampling Frequencies

CAMPLING EDECLIENCY MCDC	SETUP TIME, ns			HOLD TIME, ns		
SAMPLING FREQUENCY, MSPS	MIN	TYP	MAX	MIN	TYP	MAX
210	1.0	1.4		0.4	0.8	
190	1.1	1.5		0.5	0.9	
170	1.3	1.7		0.7	1.1	
150	1.6	1.9		0.9	1.2	
125	1.9	2.2		1.1	1.4	
<100 Enable low speed mode	2.5			2.0		
					t _{PDI} , ns	
				MIN	TYP	MAX
$1 \le F_s \le 100$, Enable low speed mode					8.2	

CMOS Timings at Lower Sampling Frequencies

	TIM	INGS SPECI	FIED WITH R	ESPECT TO	INPUT CLO	OCK
SAMPLING FREQUENCY, MSPS		t _{START} , ns		DAT	A VALID TIN	IE, ns
	MIN	TYP	MAX	MIN	TYP	MAX
210			1.7	1.6	2.4	
190			0.4	2.2	3.0	
170			5.1	2.4	3.6	
150			4.8	3.0	4.3	
		TIMINGS SPE	CIFIED WITH	H RESPECT	TO CLKOU	Т
SAMPLING FREQUENCY, MSPS	S	ETUP TIME,	ns	Н	IOLD TIME, I	ns
	MIN	TYP	MAX	MIN	TYP	MAX
150	2.0	3.2		1.5	2.2	
125	2.9	4		2.2	2.7	
<100 Enable low speed mode	5.0			3.8		
					t _{PDI} , ns	
				MIN	TYP	MAX
1 ≤ F _s ≤ 100 Enable low speed mode					14	

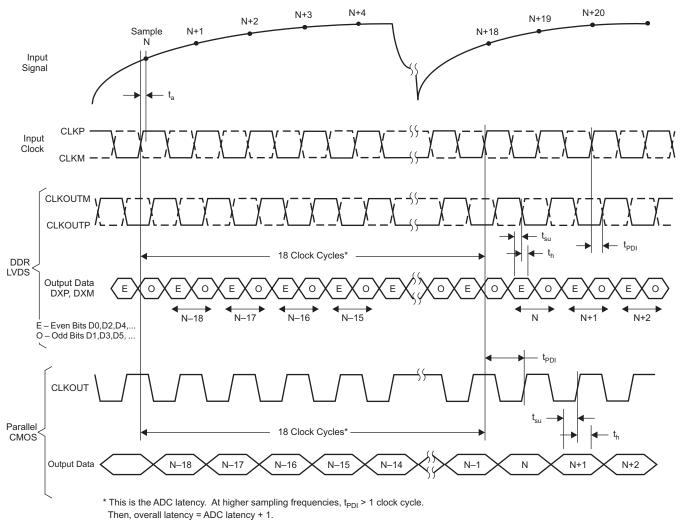
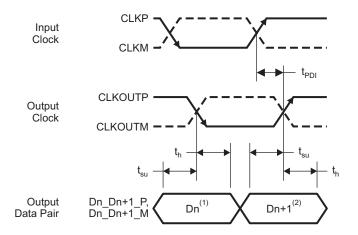


Figure 2. Latency Diagram

T0105-10

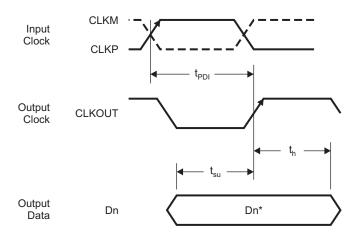


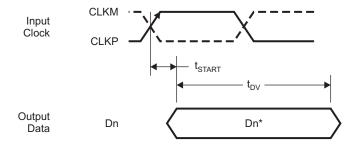


⁽¹⁾Dn – Bits D0, D2, D4,...

(2)Dn+1 – Bits D1, D3, D5, ...

Figure 3. LVDS Mode Timing





*Dn - Bits D0, D1, D2, ...

T0107-05

T0106-07

Figure 4. CMOS Mode Timing



DEVICE CONFIGURATION

The ADS61B49/29 can be configured independently using either parallel interface control or serial interface programming.

PARALLEL CONFIGURATION ONLY

To put the device in parallel configuration mode, keep RESET tied to high (DRVDD).

Now, pins DFS, MODE, SEN, and SDATA can be used to directly control certain modes of the ADC. The device can be easily configured by connecting the parallel pins to the correct voltage levels (as described in Table 3 to Table 6). There is no need to apply reset.

In this mode, SEN and SDATA function as parallel interface control pins. Frequently used functions can be controlled in this mode – standby, selection between LVDS/CMOS output formats, 2s complement/straight binary output format, and position of the output clock edge.

Table 1 briefly describes the modes controlled by the parallel pins.

TYPE OF PIN **CONTROL MODES** CONTROL **DFS** Data format and LVDS/CMOS output interface. Analog In the ADS61B49/B29, external reference is not supported. Prior use of the MODE pin in the ADS6149/29 family is therefore not the same in the ADS61B49/B29 family. In the next generation pin-compatible MODE Analog ADC family, MODE is converted to a digital control pin for certain reserved functions. The MODE pin can be routed to a digital controller for possible future migration to a next generation ADC. SEN CLKOUT edge programmability. Analog Global power down (ADC, internal references and output buffers are **SDATA** Digital powered down)

Table 1. Parallel Pin Functions

SERIAL INTERFACE CONFIGURATION ONLY

To exercise this mode, first the serial registers have to be reset to their default values and the RESET pin has to be kept low.

SEN, SDATA, and SCLK function as serial interface pins in this mode and can be used to access the internal registers of the ADC.

The registers can be reset either by applying a pulse on the RESET pin or by setting the <RESET> bit (D7 in register 0x00) high. The serial interface section describes register programming and register reset in more detail.

Since the parallel pin DFS is not to be used in this mode, it has to be tied to ground.



CONFIGURATION USING BOTH THE SERIAL INTERFACE AND PARALLEL CONTROLS

For increased flexibility, an additional configuration mode is supported wherein a combination of serial interface registers and parallel pin control (DFS) can be used to configure the device.

To exercise this mode, the serial registers have to be reset to their default values and the RESET pin has to be kept low.

SEN, SDATA, and SCLK function as serial interface pins in this mode and can be used to access the internal registers of ADC. The registers can be reset either by applying a pulse on the RESET pin or by setting the <RESET> bit (D7 in register 0x00) high. The serial interface section describes register programming and register reset in more detail.

The parallel interface control pin DFS can be used and its function is determined by the appropriate voltage levels as described in Table 3. The voltage levels can be easily derived, by using a resistor string as illustrated with an example as shown in Figure 5.

Since some functions can be controlled using both the parallel pins and serial registers, the priority between the two is determined by a priority table as listed in Table 2.

Table 2. Priority Between Parallel Pins and Serial Registers

FUNCTION	PRIORITY
Int/ext reference - not used	MODE is not used in this device (legacy from the ADS6149 and future family this pin could be redefined)
Data format selection	DFS pin controls this selection ONLY if the register bits <data format=""></data> = 00, otherwise <data format=""></data> controls the selection
LVDS or CMOS interface selection	DFS pin controls this selection ONLY if the register bits <lvds cmos=""></lvds> = 00, otherwise <lvds< b=""> CMOS> controls the selection</lvds<>

DESCRIPTION OF PARALLEL PINS

Table 3. SDATA - DIGITAL CONTROL PIN

SDATA	DESCRIPTION
0	Normal operation (default)
AVDD	Global power down. ADC, internal references and the output buffers are powered down.

Table 4. SEN - ANALOG CONTROL PIN

SEN	DESCRIPTION – OUTPUT CLOCK EDGE PROGRAMMABILITY ⁽¹⁾
0	LVDS: Data and output clock transitions are aligned CMOS: Setup time increases by (6xT _s /26), hold time reduces by (6xT _s /26)
(3/8)AVDD	LVDS: Setup time decreases by (4xT _s /26), hold time increases by (4xT _s /26) CMOS: Setup time increases by (9xT _s /26), hold time reduces by (9xT _s /26)
(5/8)AVDD	LVDS: Setup time increases by (4xT _s /26), hold time reduces by (4xT _s /26) CMOS: Setup time increases by (3xT _s /26), hold time reduces by (3xT _s /26)
AVDD	Default output clock position (setup/hold timings of output data with respect to this clock position is specified in the timing characteristics table).

(1) $T_s = 1 / sampling frequency$

Table 5. DFS - ANALOG CONTROL PIN

DFS	DESCRIPTION
0	2s complement data and DDR LVDS output
(3/8)AVDD	2s complement data and parallel CMOS output
(5/8)AVDD	Offset binary data and parallel CMOS output
AVDD	Offset binary data and DDR LVDS output



Table 6. MODE – ANALOG CONTROL PIN

MODE	DESCRIPTION
Not used	In the ADS61B49/B29, external reference is not supported. The prior use of the MODE pin in ADS6149/29 family is therefore not the same in the ADS61B49/B29 family. In the next generation pin-compatible ADC family, MODE could be converted to a digital control pin for certain reserved functions. The MODE pin can be routed to a digital controller for possible future migration to a next generation ADC.

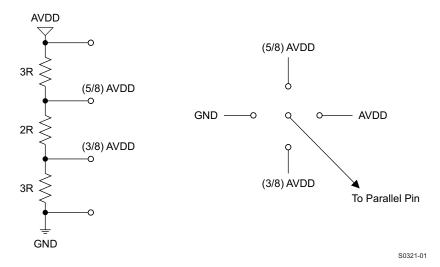


Figure 5. Simple Scheme to Configure Parallel Pins SEN and SCLK

SERIAL INTERFACE

The ADC has a set of internal registers, which can be accessed by the serial interface formed by pins SEN (Serial Interface Enable), SCLK (Serial Interface Clock) and SDATA (Serial Interface Data).

Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA is latched at every falling edge of SCLK when SEN is active (low). The serial data is loaded into the register at every 16th SCLK falling edge when SEN is low. In case the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiples of 16-bit words within a single active SEN pulse.

The first 8 bits form the register address, and the remaining 8 bits are the register data. The interface can work with a SCLK frequency from 20 MHz down to very low speeds (few hertz) and also with a non-50% SCLK duty cycle.

Register Initialization

After power-up, the internal registers MUST be initialized to their default values. This can be done in one of two ways:

1. Either through hardware reset by applying a high-going pulse on the RESET pin (of width greater than 10 ns) as shown in Figure 6.

OR

2. By applying a software reset. Using the serial interface, set the **<RESET>** bit (D7 in register 0x00) to high. This initializes the internal registers to their default values and then self-resets the **<RESET>** bit to low. In this case the RESET pin is kept low.



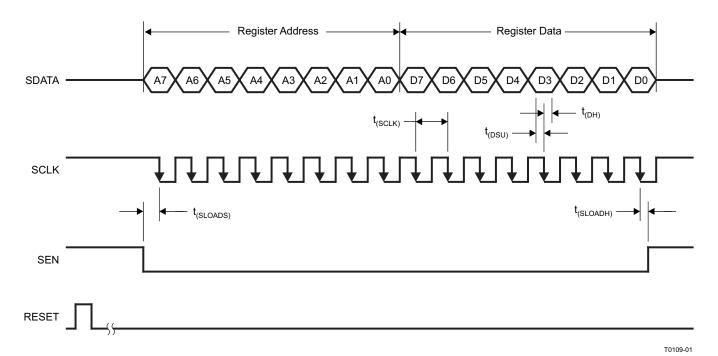


Figure 6. Serial Interface Timing

SERIAL INTERFACE TIMING CHARACTERISTICS

Typical values at 25°C, min and max values across the full temperature range $T_{MIN} = -40$ °C to $T_{MAX} = 85$ °C, AVDD = 3.3 V, DRVDD = 1.8 V, unless otherwise noted.

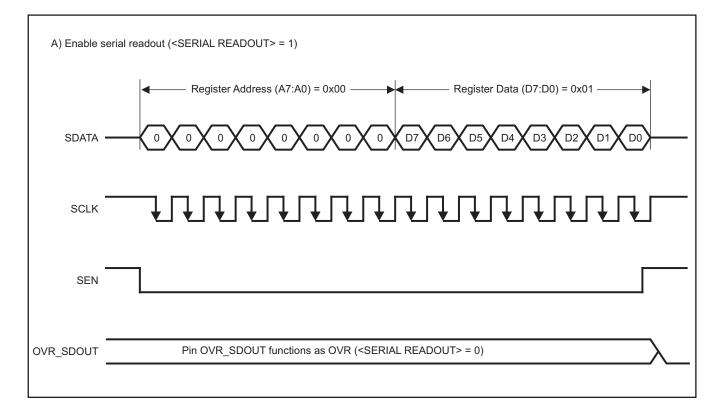
	PARAMETER	MIN	TYP	MAX	UNIT
f _{SCLK}	SCLK frequency (= 1/ t _{SCLK})	> dc		20	MHz
t _{SLOADS}	SEN to SCLK setup time	25			ns
t _{SLOADH}	SCLK to SEN hold time	25			ns
t _{DS}	SDATA setup time	25			ns
t _{DH}	SDATA hold time	25			ns

SERIAL REGISTER READOUT

The device includes an option where the contents of the internal registers can be read back. This may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC.

- a. First, set register bit <SERIAL READOUT> = 1. This also disables any further writes into the registers (EXCEPT register bit <SERIAL READOUT> itself).
- b. Initiate a serial interface cycle specifying the address of the register (A7-A0) whose content has to be read.
- c. The device outputs the contents (D7-D0) of the selected register on the OVR_SDOUT pin.
- d. The external controller can latch the contents at the falling edge of SCLK.
- e. To enable register writes, reset register bit <SERIAL READOUT> = 0.





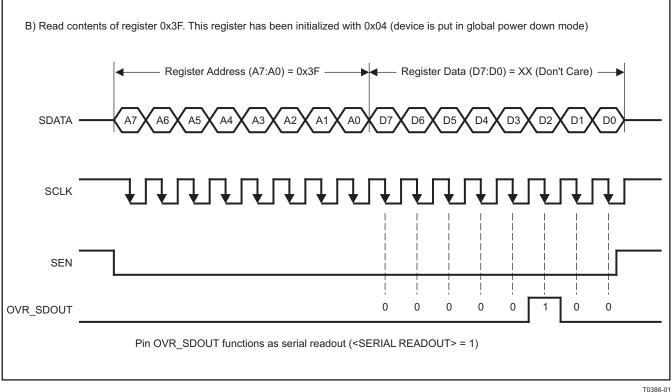


Figure 7. Serial Readout



RESET TIMING

Typical values at 25°C, min and max values across the full temperature range $T_{MIN} = -40$ °C to $T_{MAX} = 85$ °C, unless otherwise noted.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t ₁	Power-on delay time	Delay from power-up of AVDD and DRVDD to RESET pulse active		1		ms
t ₂	Reset pulse width	Pulse width of active RESET signal that resets the serial registers	10			ns
		Fulse width of active RESET signal that resets the serial registers			1	μs
t ₃	Delay time	Delay from RESET disable to SEN active	100			ns

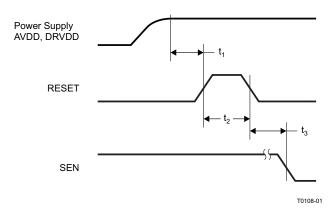


Figure 8. Reset Timing Diagram

SERIAL REGISTER MAP

Table 7. Summary of Functions Supported by Serial Interface⁽¹⁾

REGISTER ADDRESS		REGISTER FUNCTIONS									
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0			
00	<reset> Software Reset</reset>	0	0	0	0	0	0	<serial READOUT></serial 			
20	0	0	0	0	0	<enable LOW SPEED MODE></enable 	0	0			
3F	0	<ref> (RESERVED)</ref>		0	0	<pdn GLOBAL></pdn 	<standby></standby>	<pdn OBUF></pdn 			
41		0	0	0	0	0	0				
44		<clkout posn<br="">Output clock position</clkout>		ol			0	0			
50	0	0	0	0	0	<data fo<br="">2s compleme bina</data>	ent or offset	0			
51		<cus1< td=""><td>гом г</td><td>PATTI</td><td>ERN I</td><td>_OW></td><td></td><td></td></cus1<>	гом г	PATTI	ERN I	_OW>					
52	0	0				<custom pat<="" td=""><td>TERN HIGH></td><td></td></custom>	TERN HIGH>				
53	0	<enable corr="" offset=""></enable>	0	0	0	0	0	0			
55		<pre> <fine gain=""> </fine></pre>					RR TIME CONS				
62	0	0 0 0 0 <tes< td=""><td>ST PATTERNS</td><td>S></td></tes<>					ST PATTERNS	S>			
63	0	0			<p< td=""><td>ROGRAM OFFS</td><td>ET PEDESTAL</td><td>></td></p<>	ROGRAM OFFS	ET PEDESTAL	>			

⁽¹⁾ Multiple functions in a register can be programmed in a single write operation.



DESCRIPTION OF SERIAL REGISTERS

A)

A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
00	<reset> Software Reset</reset>	0	0	0	0	0	0	<serial readout=""></serial>

D7 <RESET>

1 Software reset applied – resets all internal registers and self-clears to 0.

D0 <SERIAL READOUT>

0 Serial readout disabled

Serial readout enabled, pin OVR_SDOUT functions as serial data readout.

B)

A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
20	0	0	0	0	0	<enable LOW SPEED MODE></enable 	0	0

D2 < ENABLE LOW SPEED MODE>

- 0 Low speed mode disabled. Use for sampling frequency > 100 MSPS
- 1 Enable low speed mode for sampling frequencies ≤ 100 MSPS.

C)

A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
3F	0	<ref>(RE</ref>	SERVED)	0	0	<pdn GLOBAL></pdn 	<standby></standby>	<pdn OBUF></pdn

D6,D5 <REF> RESERVED (Not used)

In the ADS61B49/61B29, external reference mode is not supported. See ADS6149/6129 non-buffered ADCs if an external reference is required. This register controls the reference mode in those devices.

- D2 <PDN GLOBAL>
- 0 Normal operation
- 1 Total power down ADC, internal references and output buffers are powered down. Slow wake-up time.
- D1 <STANDBY>
- 0 Normal operation
- 1 ADC alone powered down. Internal references, output buffers are active. Quick wake-up time
- D0 <PDN OBUF> Power down output buffer
- 0 Output buffer enabled
- 1 Output buffer powered down

D)

A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
41	<lvds< th=""><th>CMOS></th><th>0</th><th>0</th><th>0</th><th>0</th><th>0</th><th>0</th></lvds<>	CMOS>	0	0	0	0	0	0

D7,D6 <LVDS CMOS>

- 00 DFS pin controls LVDS or CMOS interface selection
- 10 DDR LVDS interface
- 11 Parallel CMOS interface

E)

A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
44		CLKO	UT POSN> O	utput clock posi	tion control		0	0

Submit Documentation Feedback



LVDS Interface

D7-D5	<clkout posn=""> Output clock rising edge position</clkout>
000	Default output clock position (refer to timing specification table)
100	Default output clock position (refer to timing specification table)
101	Rising edge shifted by $+ (4/26)T_s$
110	Rising edge aligned with data transition
111	Rising edge shifted by - $(4/26)T_s$
D4-D2	< CLKOUT POSN> Output clock falling edge position
D4-D2 000	<clkout posn=""> Output clock falling edge position Default output clock position (refer to timing specification table)</clkout>
000	Default output clock position (refer to timing specification table)
000	Default output clock position (refer to timing specification table) Default output clock position (refer to timing specification table)

CMOS Interface

D7-D5	<clkout posn=""> Output clock rising edge position</clkout>
000	Default output clock position (refer to timing specification table)
100	Default output clock position (refer to timing specification table)
101	Rising edge shifted by + $(4/26)T_s$
110	Rising edge shifted by + $(6/26)T_s$
111	Rising edge aligned with data transition
D4-D2	<clkout posn=""> Output clock falling edge position</clkout>
D4-D2 000	<clkout posn=""> Output clock falling edge position Default output clock position (refer to timing specification table)</clkout>
000	Default output clock position (refer to timing specification table)
000	Default output clock position (refer to timing specification table) Default output clock position (refer to timing specification table)

F)

A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
50	0	0	0	0	0	<data fo<="" td=""><th></th><td>0</td></data>		0

D2,D1 <DATA FORMAT>

00 DFS pin controls data format selection

10 2s complement

11 Offset binary

G)

A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
51				<cus< th=""><th>tom LOW></th><th></th><td></td><th></th></cus<>	tom LOW>			
52					<custo< th=""><th>m HIGH></th><td></td><th></th></custo<>	m HIGH>		

D7-D0 <CUSTOM LOW>

8 lower bits of custom pattern available at the output instead of ADC data.

D5-D0 <CUSTOM HIGH>

6 upper bits of custom pattern available at the output instead of ADC data



H)

-	A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
	53	0	<enable corr="" offset=""> Offset correction enable</enable>	0	0	0	0	0	0

D6 < ENABLE OFFSET CORR>

0 Offset correction disabled

1 Offset correction enabled

I)

A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
55		<fine< th=""><th>GAIN></th><th></th><th><offset< th=""><th>CORR TC> Offs</th><th>et correction tin</th><th>ne constant</th></offset<></th></fine<>	GAIN>		<offset< th=""><th>CORR TC> Offs</th><th>et correction tin</th><th>ne constant</th></offset<>	CORR TC> Offs	et correction tin	ne constant

D7-D4	<fine gain=""> Gain programmability in 0.5-dB steps</fine>
0000	0-dB gain, default after reset
0001	0.5-dB gain
0010	1.0-dB gain
0011	1.5-dB gain
0100	2.0-dB gain
0101	2.5-dB gain
0110	3.0-dB gain
0111	3.5-dB gain
1000	4.0-dB gain
1001	4.5-dB gain
1010	5.0-dB gain
1011	5.5-dB gain
1100	6.0-dB gain
D3-D0	<offset corr="" tc=""></offset> Time constant of correction loop in number of clock cycles. See <i>Offset Correction</i> in application section.
0000	256 k
0001	512 k
0010	1 M
0011	2 M
0100	4 M
0101	8 M
0110	16 M
0111	32 M
1000	64 M
1001	128 M
1010	256 M
1011	512 M
1100 to 1111	Reserved



www.ti.com

J)

A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
62	0	0	0	0	0	<te< td=""><th>EST PATTERNS</th><th>S></th></te<>	EST PATTERNS	S>

D2-D0	<test patterns=""> Test patterns to verify data capture</test>	
000	Normal operation	
001	Outputs all zeros	
010	Outputs all ones	
011	Outputs toggle pattern	
100	Outputs digital ramp	
101	Outputs custom pattern	
110	Unused	
111	Unused	

K)

A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
63	0	0			<offset< th=""><th>PEDESTAL></th><td></td><th></th></offset<>	PEDESTAL>		

OFFSET PEDESTAL> When the offset correction is enabled, the final converged value after the offset is corrected is the ADC mid-code value.

A pedestal can be added to the final converged value by programming these bits. For example, See *Offset Correction* in application section.

011111 Mid-code + 31 LSB 011110 Mid-code + 30 LSB

011101 Mid-code + 29 LSB

....

000000 Mid-code

111111 Mid-code - 1 LSB111110 Mid-code - 2 LSB

....

100000 Mid-code - 32 LSB



DEVICE INFORMATION

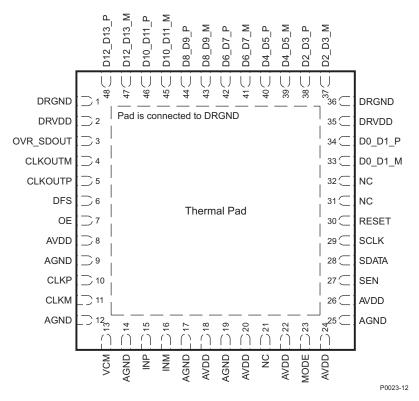


Figure 9. PIN CONFIGURATION (LVDS MODE) — ADS61B49

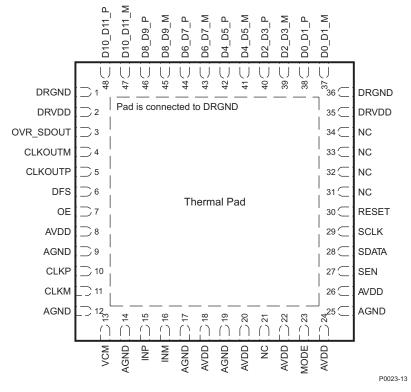


Figure 10. PIN CONFIGURATION (LVDS MODE) — ADS61B29



Table 8. PIN ASSIGNMENTS (LVDS MODE) — ADS61B49 and ADS61B29

PIN			NO.	ADSCIDING (EVDS MODE) — ADSCID49 and ADSCID29
NAME	NO.	1/0	of PINS	DESCRIPTION
AVDD	8, 18, 20, 22, 24, 26	I	6	3.3-V analog power supply
AGND	9, 12, 14, 17, 19, 25	I	6	Analog ground
CLKP, CLKM	10, 11	- 1	2	Differential clock input
INP, INM	15, 16	I	2	Differential analog input
				Internal reference mode – Common-mode voltage output.
VCM	13	Ю	1	External reference mode – Reference input. The voltage forced on this pin sets the internal references.
				Serial interface RESET input.
RESET	30	ı	1	When using serial interface mode, the user MUST initialize the internal registers through a hardware RESET by applying a high-going pulse on this pin or by using the software reset option. Refer to the SERIAL INTERFACE section.
			In parallel interface mode, the user has to tie the RESET pin permanently high. (SDATA and SEN are used as parallel pin controls in this mode.)	
				The pin has an internal 100-k Ω pull-down resistor.
SCLK	29	I	1	Serial interface clock input. The pin has an internal 100-kΩ pull-down resistor.
CDATA	00		4	This pin functions as the serial interface data input when RESET is low. It functions as the power-down control pin when RESET is tied high.
SDATA	28	1	1	See Table 3 for detailed information.
				The pin has an internal 100-kΩ pull-down resistor.
				This pin functions as the serial interface enable input when RESET is low.
SEN	27	ı	1	It functions as the output clock edge control when RESET is tied high. See Table 4 for detailed information.
				The pin has an internal 100-k Ω pull-up resistor to AVDD.
OE	7	- 1	1	Output buffer enable input, active high. The pin has an internal 100-kΩ pull-up resistor to DRVDD
DFS	6	ı	1	Data format select input. This pin sets the data format (2s complement or offset binary) and the LVDS/CMOS output interface type.
40				See Table 5 for detailed information.
MODE ⁽¹⁾	23	ı	1	Not used. See Table 6 and note below for detailed information.
CLKOUTP	5	0	1	Differential output clock, true
CLKOUTM	4	0	1	Differential output clock, complement
D0_D1_P	-	0	1	Differential output data D0 and D1 multiplexed, true
D0_D1_M	-	0	1	Differential output data D0 and D1 multiplexed, complement
D2_D3_P	_	0	1	Differential output data D2 and D3 multiplexed, true
D2_D3_M	=	0	1	Differential output data D2 and D3 multiplexed, complement
D4_D5_P	_	0	1	Differential output data D4 and D5 multiplexed, true
D4_D5_M	See	0	1	Differential output data D4 and D5 multiplexed, complement
D6_D7_P	Figure 9 and	0	1	Differential output data D6 and D7 multiplexed, true
D6_D7_M	Figure 10	0	1	Differential output data D6 and D7 multiplexed, complement
D8_D9_P	=	0	1	Differential output data D8 and D9 multiplexed, true Differential output data D8 and D9 multiplexed, complement
D8_D9_M D10_D11_P	-	0	1	Differential output data D0 and D1 multiplexed, complement
D10_D11_P	1	0	1	Differential output data D10 and D11 multiplexed, true Differential output data D10 and D11 multiplexed, complement
D10_D11_M D12_D13_P	1	0	1	Differential output data D12 and D13 multiplexed, complement
D12_D13_F	1	0	1	Differential output data D12 and D13 multiplexed, true
J 12_D 10_IVI				It is a CMOS output with logic levels determined by the DRVDD supply. It functions as an out-of-range indicator
OVR_SDOUT	3	0	1	after a reset and when register bit <serial readout=""> = 0. It functions as the serial register readout pin when register bit <serial readout=""> = 1.</serial></serial>
DRVDD	2, 35	I	2	1.8-V digital and output buffer supply
DRGND	1, 36, PAD	- 1	2	Digital and output buffer ground

⁽¹⁾ In the next generation pin-compatible ADC family, MODE is converted to a digital control pin for certain reserved functions. So, the selection of the internal or external reference and low speed functions are supported using MODE. In a system board using the ADS61x9/x8, the MODE pin can be routed to a digital controller. This avoids board modification if migrating to the next generation ADC.



Table 8. PIN ASSIGNMENTS (LVDS MODE) — ADS61B49 and ADS61B29 (continued)

PIN			NO.	
NAME	NO.	1/0	of PINS	DESCRIPTION
NC	See Figure 9 and Figure 10			Do not connect



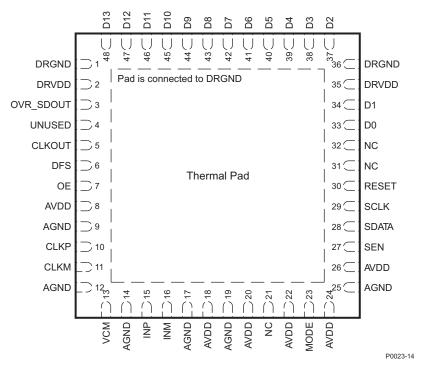


Figure 11. PIN CONFIGURATION (CMOS MODE) - ADS61B49

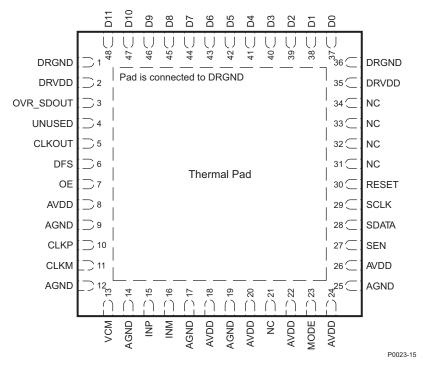


Figure 12. PIN CONFIGURATION (CMOS MODE) - ADS61B29



Table 9. PIN ASSIGNMENTS (CMOS MODE) - ADS61B49 and ADS61B29

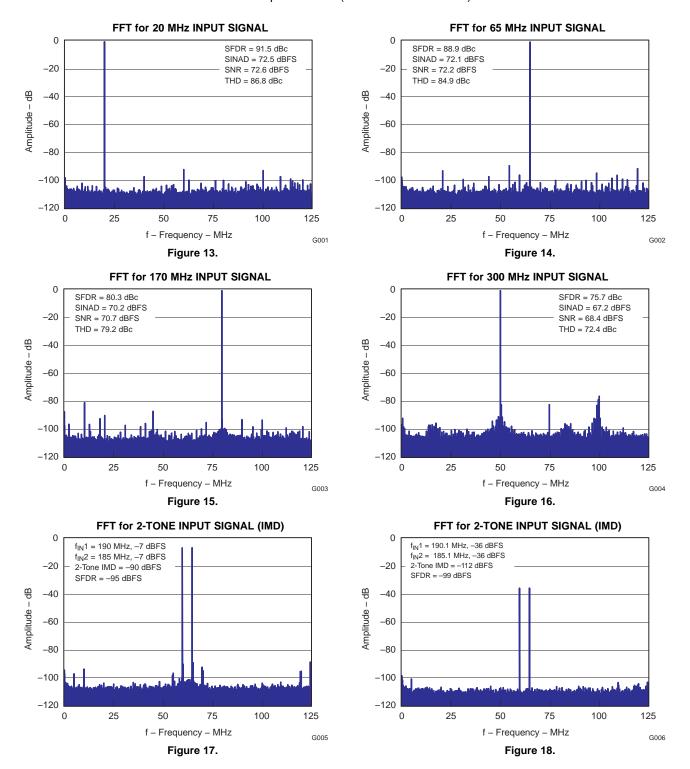
PIN			NO. of	
NAME	NO.	1/0	PINS	DESCRIPTION
AVDD	8, 18, 20, 22, 24, 26	I	6	3.3-V analog power supply
AGND	9, 12, 14, 17, 19, 25	I	6	Analog ground
CLKP, CLKM	10, 11	I	2	Differential clock input
INP, INM	15, 16	I	2	Differential analog input
VCM	13	Ю	1	Internal reference mode – Common-mode voltage output.
				External reference mode – Reference input. The voltage forced on this pin sets the internal references.
RESET	30	I	1	Serial interface RESET input.
				When using serial interface mode, the user MUST initialize the internal registers through a hardware RESET by applying a high-going pulse on this pin or by using the software reset option. Refer to the SERIAL INTERFACE section.
				In parallel interface mode, the user has to tie the RESET pin permanently high. (SDATA and SEN are used as parallel pin controls in this mode.)
				The pin has an internal 100-k Ω pull-down resistor.
SCLK	29	I	1	Serial interface clock input. The pin has an internal 100-k Ω pull-down resistor.
	28	ı	1	This pin functions as the serial interface data input when RESET is low. It functions as the power-down control pin when RESET is tied high.
SDATA				See Table 3 for detailed information.
				The pin has an internal 100-k Ω pull-down resistor.
	27	I	1	This pin functions as the serial interface enable input when RESET is low.
SEN				It functions as the output clock edge control when RESET is tied high. See Table 4 for detailed information.
				The pin has an internal 100-k Ω pull-up resistor to DVDD.
DFS	6	I	1	Data format select input. This pin sets the data format (2s complement or offset binary) and the LVDS/CMOS output interface type.
				See Table 5 for detailed information.
MODE ⁽¹⁾	23	I	1	Not used. See Table 6 and note below for detailed information.
CLKOUT	5	0	1	CMOS output clock
OE	7	I	1	Output buffer enable input, active high. The pin has an internal 100-k Ω pull-up resistor to DRVDD
D0-D13	See Figure 11 and Figure 12	0	14/12	14-bit/12-bit CMOS output data
OVR_SDOUT	3	0	1	It is a CMOS output with logic levels determined by the DRVDD supply. It functions as an out-of-range indicator after a reset and when register bit <serial readout=""> = 0. It functions as the serial register readout pin when <serial readout=""> = 1.</serial></serial>
DRVDD	2, 35	I	2	1.8-V digital and output buffer supply
DRGND	1, 36, PAD	I	2	Digital and output buffer ground
UNUSED	4		1	Unused pin in CMOS mode
NC	See Figure 11 and Figure 12			Do not connect

⁽¹⁾ In the next generation pin-compatible ADC family, MODE is converted to a digital control pin for certain reserved functions. So, the selection of the internal or external reference and low speed functions are supported using MODE. In a system board using the ADS61x9/x8, the MODE pin can be routed to a digital controller. This avoids board modification while migrating to the next generation ADC.



TYPICAL CHARACTERISTICS - ADS61B49

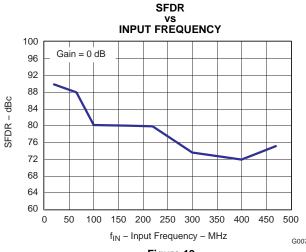
All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode, 0-dB gain, LVDS output interface (unless otherwise noted)





TYPICAL CHARACTERISTICS - ADS61B49 (continued)

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode, 0 -dB gain, LVDS output interface (unless otherwise noted)



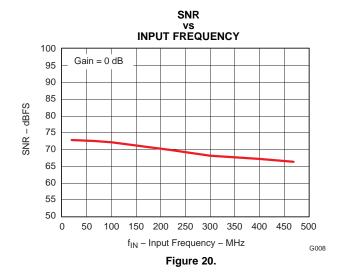
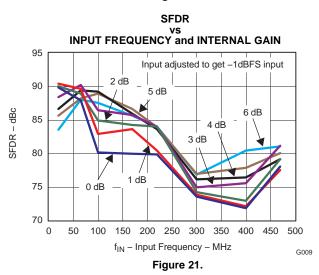
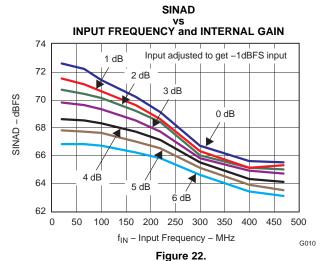


Figure 19.

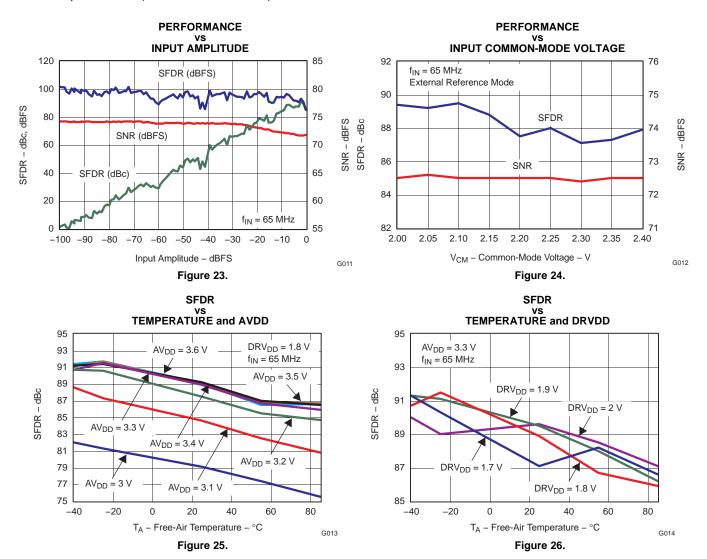






TYPICAL CHARACTERISTICS - ADS61B49 (continued)

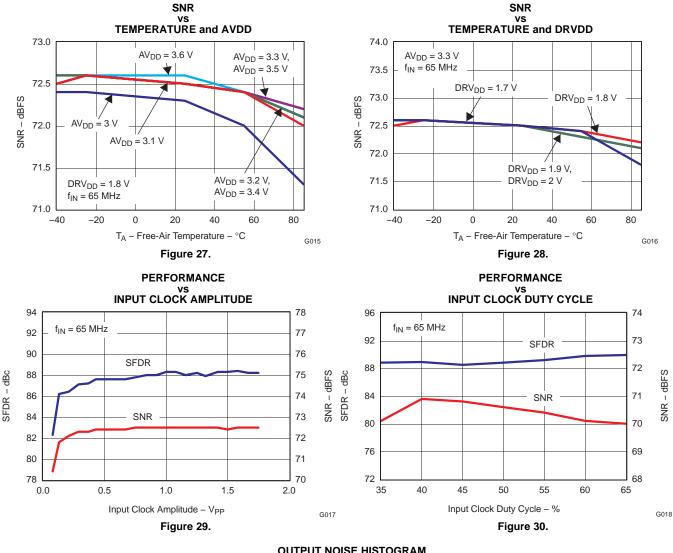
All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode, 0 -dB gain, LVDS output interface (unless otherwise noted)

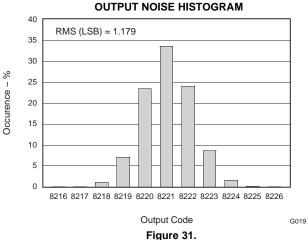




TYPICAL CHARACTERISTICS - ADS61B49 (continued)

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode, 0 -dB gain, LVDS output interface (unless otherwise noted)

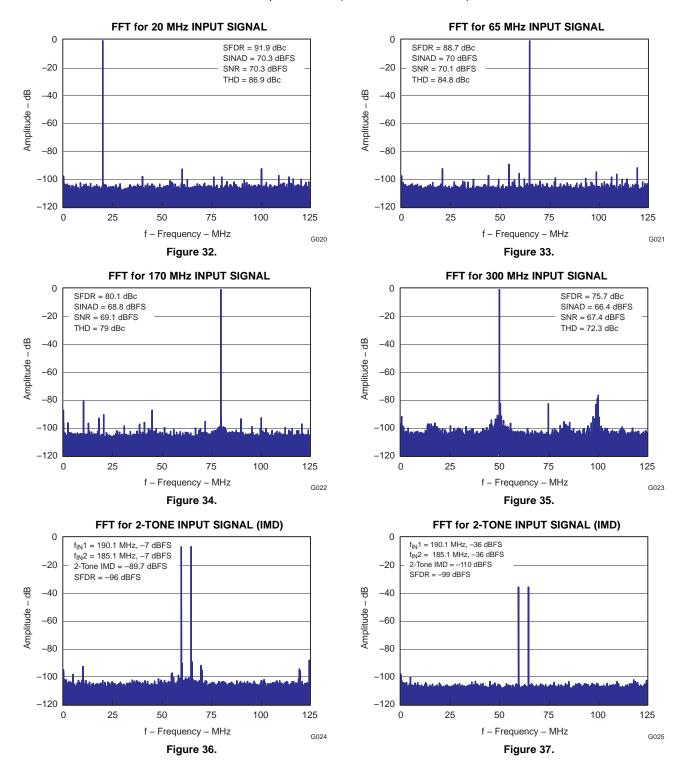






TYPICAL CHARACTERISTICS - ADS61B29

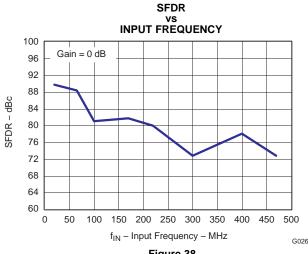
All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, -1 DBFS differential analog input, internal reference mode, 0-dB gain, LVDS output interface (unless otherwise noted)

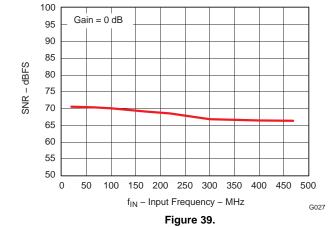




TYPICAL CHARACTERISTICS - ADS61B29 (continued)

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, -1 DBFS differential analog input, internal reference mode, 0-dB gain, LVDS output interface (unless otherwise noted)

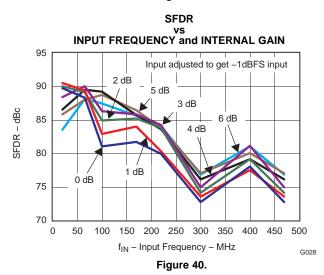




SNR

vs INPUT FREQUENCY

Figure 38.



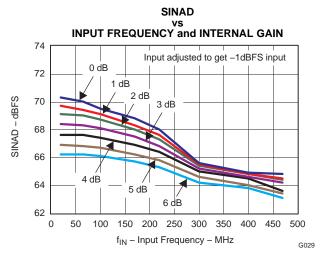
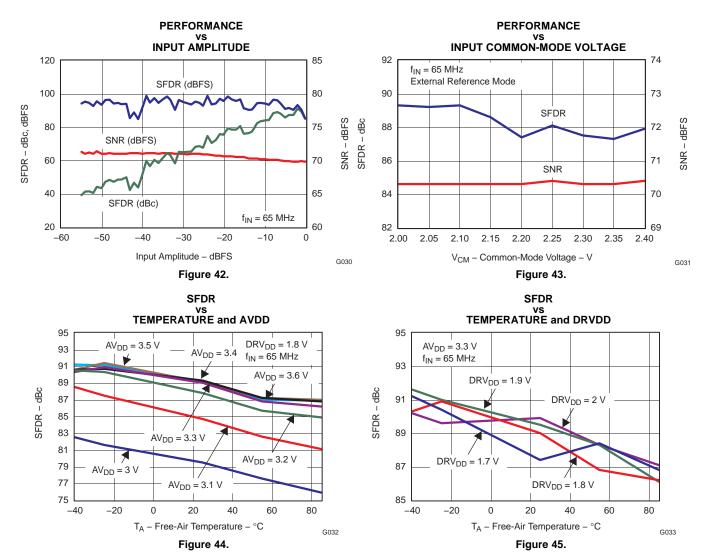


Figure 41.



TYPICAL CHARACTERISTICS - ADS61B29 (continued)

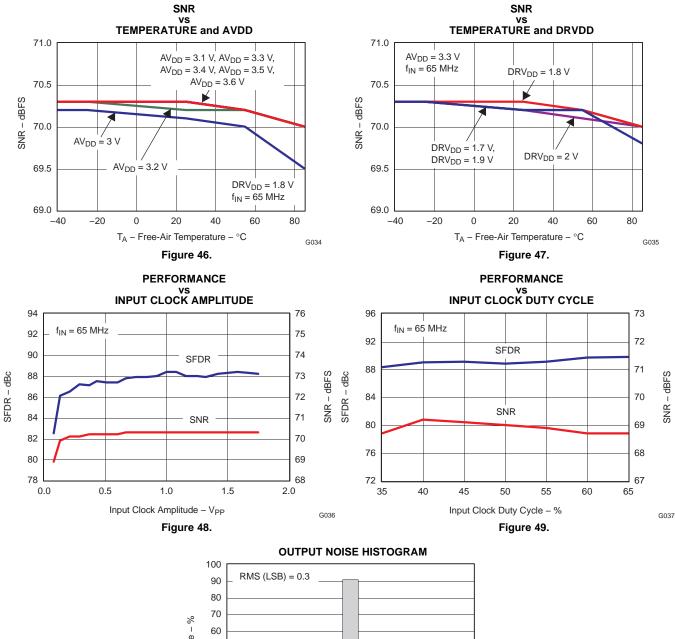
All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, -1 DBFS differential analog input, internal reference mode, 0 -dB gain, LVDS output interface (unless otherwise noted)





TYPICAL CHARACTERISTICS - ADS61B29 (continued)

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, -1 DBFS differential analog input, internal reference mode, 0 -dB gain, LVDS output interface (unless otherwise noted)



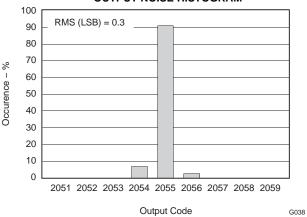
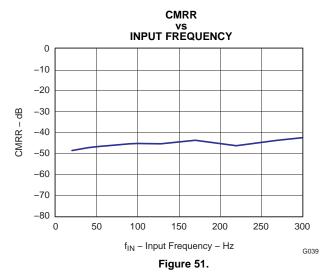


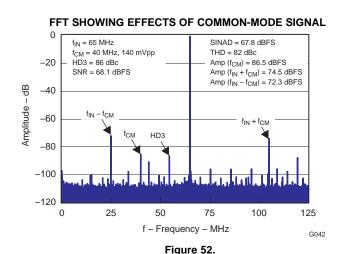
Figure 50.

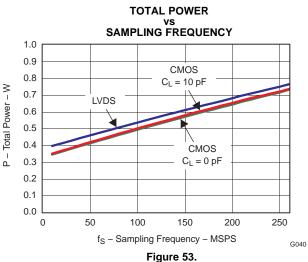


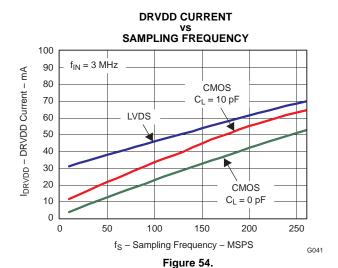
TYPICAL CHARACTERISTICS - COMMON PLOTS (Both ADS61B49/61B29)

All plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, -1 DBFS differential analog input, internal reference mode, 0-dB gain, LVDS output interface (unless otherwise noted)











CONTOUR PLOTS - ADS61B49/ADS61B29

Plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode, 0-dB gain, LVDS output interface (unless otherwise noted)

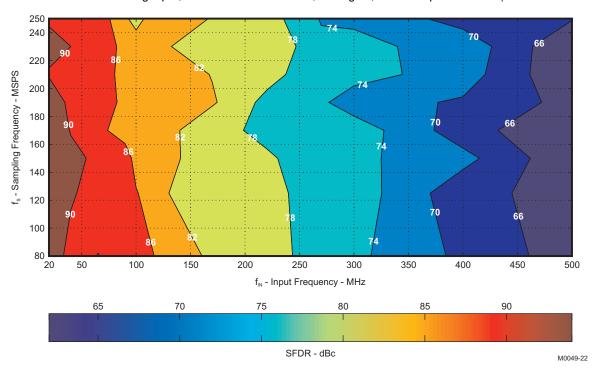


Figure 55. SFDR Contour Plot (0-dB gain)

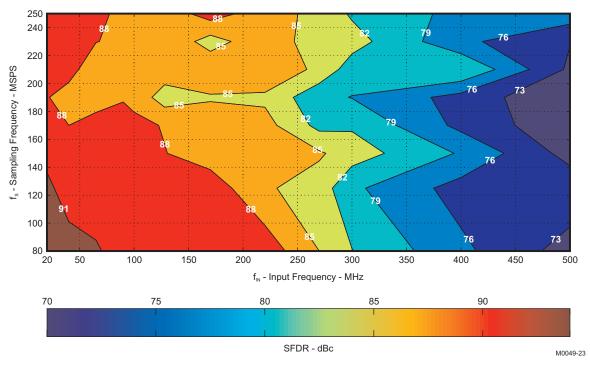


Figure 56. SFDR Contour Plot (6-dB gain)



CONTOUR PLOTS - ADS61B49

Plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode, 0-dB gain, LVDS output interface (unless otherwise noted)

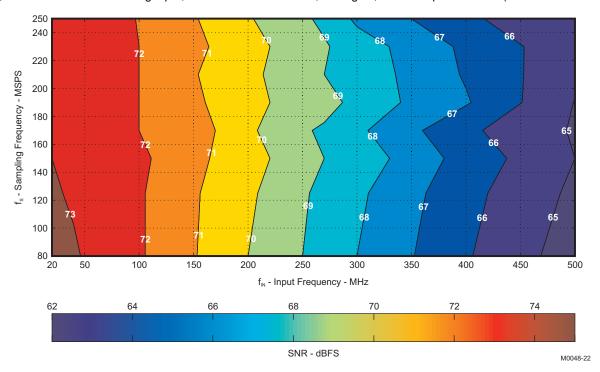


Figure 57. SNR Contour Plot (0-dB gain)

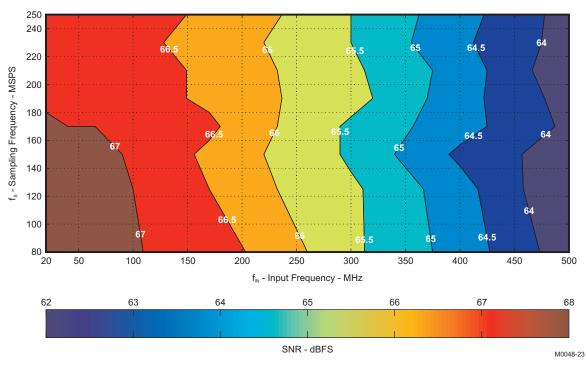


Figure 58. SNR Contour Plot (6-dB gain)

CONTOUR PLOTS - ADS61B29

Plots are at 25°C, AVDD = 3.3 V, DRVDD = 1.8 V, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode, 0-dB gain, LVDS output interface (unless otherwise noted)

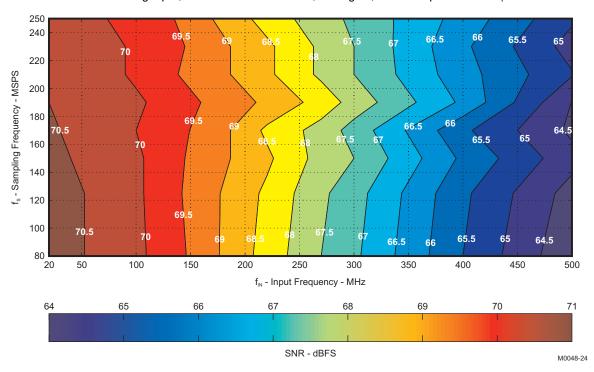


Figure 59. SNR Contour Plot (0-dB gain)

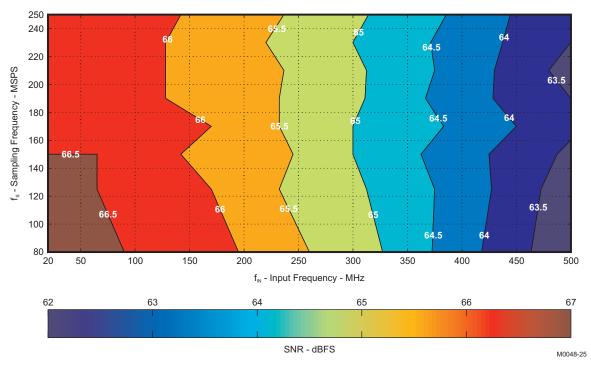


Figure 60. SNR Contour Plot (6-dB gain)



APPLICATION INFORMATION

THEORY OF OPERATION

The ADS61B49/29 are high performance, low power 14-bit and 12-bit A/D converters with maximum sampling rates up to 250 MSPS. The primary difference from the ADS6149/29 is the addition of an integrated analog buffer (hence B in the device name).

The conversion process is initiated by a rising edge of the external input clock and the analog input signal is sampled. The sampled signal is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. At every clock edge the sample propagates through the pipeline resulting in a data latency of 18 clock cycles. The output is available as 14-bit/12-bit data, in DDR LVDS or CMOS and coded in either straight offset binary or binary 2s complement format.

The dynamic offset of the first stage sub-ADC limits the maximum analog input frequency to about 500MHz (with 2-Vpp amplitude) and about 800MHz (with 1-Vpp amplitude) before the performance becomes ill-behaved. This is separate from the full power analog bandwidth of 750MHz, which is only an indicator of signal amplitude versus frequency.

ANALOG INPUT

The analog input consists of an integrated input buffer followed by a switched-capacitor based differential sample and hold architecture. The addition of a buffer provides isolation from the non-linear impedance and switching transients of the switched-capacitor circuit. With a constant input impedance, the ADC is easier to drive and to reproduce data sheet measurements. For wide-band applications, like power amplifier linearization, the signal gain across frequency is more consistent. Spectral performance variance across frequency is also reduced.

This differential topology results in very good ac performance even for high input frequencies at high sampling rates. The INP and INM pins have to be externally biased around a common-mode voltage of 2.3 V, available on the VCM pin. For a full-scale differential input, each input pin INP, INM has to swing symmetrically between VCM+ 0.5 V and VCM -0.5 V, resulting in a 2-V_{pp} differential input swing.

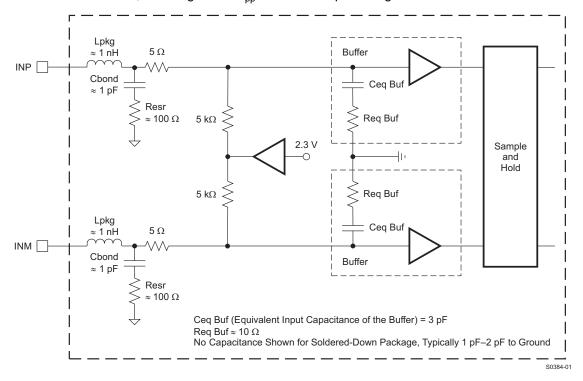


Figure 61. Analog Input Equivalent Circuit

The input sampling circuit has a high 3-dB bandwidth that extends up to 750 MHz (measured from the input pins to the sampled voltage).



Drive Circuit Requirements

For optimum performance, the analog inputs must be driven differentially. This improves the common-mode noise immunity and even-order harmonic rejection. A $5-\Omega$ resistor in series with each input pin is recommended to dampen out ringing caused by package parasitics.

Due to the integrated high impedance buffer in the ADS61B49/29 family, the filtering of the glitches with an external R-C-R filter suggested for the ADS6149/29 family is not required. The drive circuit may have to be designed to provide a low insertion loss over the desired frequency range and matched impedance to the source. While doing this, the ADC input impedance must be considered. Figure 62 and Figure 63 show the impedance $(Z_{IN} = R_{IN} \mid\mid C_{IN})$ looking into the ADC input pins. These figures compare the buffered ADS61B49 to the non-buffered ADS6149.

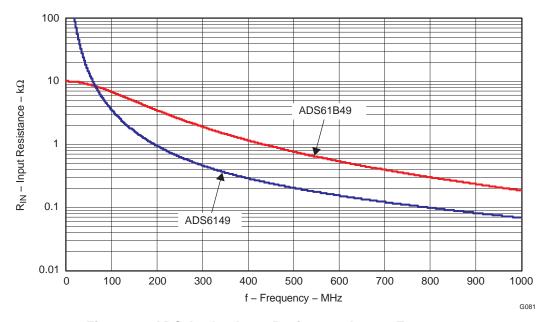


Figure 62. ADC Analog Input Resistance Across Frequency

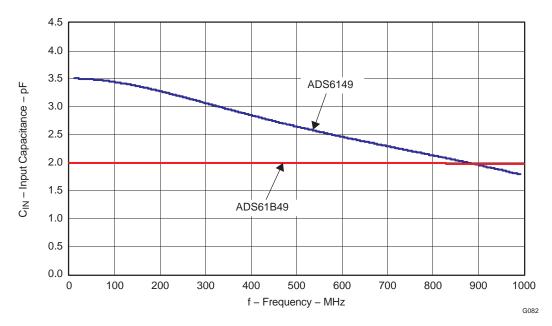


Figure 63. ADC Analog Input Capacitance Across Frequency



Driving Circuit

Two example driving circuit configurations are shown in Figure 64 and Figure 65 – one optimized for low input frequencies and the other for high input frequencies. Notice in both cases that the board circuitry is simplified compared to the non-buffered ADS6149. In Figure 64, a single transformer is used and is suited for low input frequencies and works for some high frequency applications as well. To optimize even-harmonic performance at high input frequencies (> 2nd Nyquist), the use of back-to-back transformers is recommended (see Figure 65).

Note that both drive circuits have been terminated by $50-\Omega$ near the ADC side. The ac-coupling capacitors allow the analog inputs to self-bias around the required common-mode voltage.

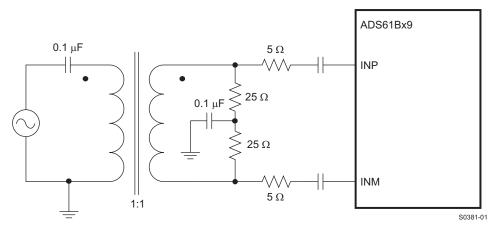


Figure 64. Drive Circuit for Low Frequencies

The mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back-to-back helps minimize this mismatch and good performance is obtained for high frequency input signals. An additional termination resistor pair may be required between the two transformers as shown in the figures. The center point of this termination is connected to ground to improve the balance between the P and M sides. The values of the terminations between the transformers and on the secondary side have to be chosen to achieve an effective 50 Ω (in the case of 50- Ω source impedance).

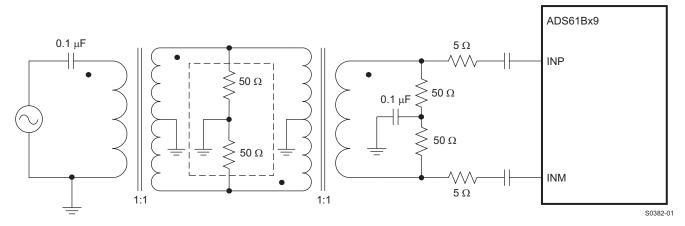


Figure 65. Drive Circuit for High Frequencies

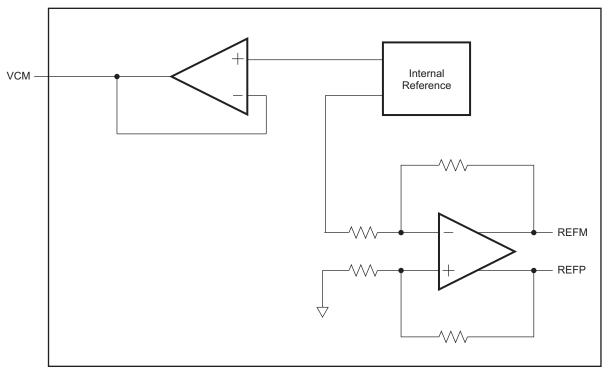
Input Common-Mode

To ensure a low-noise common-mode reference, the VCM pin is filtered with a 0.1-μF low-inductance capacitor connected to ground. The input common-mode voltage is nominally 2.3 V, which is 1.5 V for the ADS6149.

TEXAS INSTRUMENTS

REFERENCE

The ADS61B49/29 have built-in internal references REFP and REFM, requiring no external components. Design schemes are used to linearize the converter load seen by the references; this and the on-chip integration of the requisite reference capacitors eliminates the need for external decoupling. External reference mode is not supported. The reference generates the VCM output (2.3 V).



S0165-10

Figure 66. Reference Section

CLOCK INPUT

The ADS61B49/29 clock inputs can be driven differentially (sine, LVPECL, or LVDS) or single-ended (LVCMOS) with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to VCM using internal 5-k Ω resistors. This allows using transformer-coupled drive circuits for sine wave clock or ac-coupling for LVPECL, LVDS clock sources.



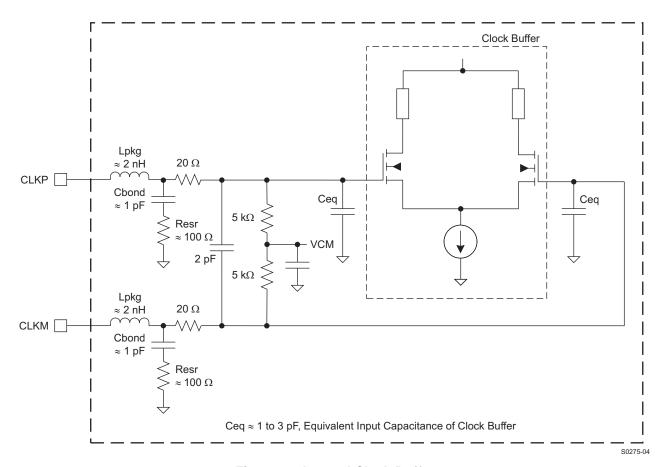


Figure 67. Internal Clock Buffer

A single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM connected to ground with a 0.1- μ F capacitor, as shown in Figure 69. For best performance, the clock inputs have to be driven differentially, reducing susceptibility to common-mode noise. For high input frequency sampling, it is recommended to use a clock source with very low jitter. Band-pass filtering of the clock source can help reduce the effect of jitter. There is no change in performance with a non-50% duty cycle clock input.

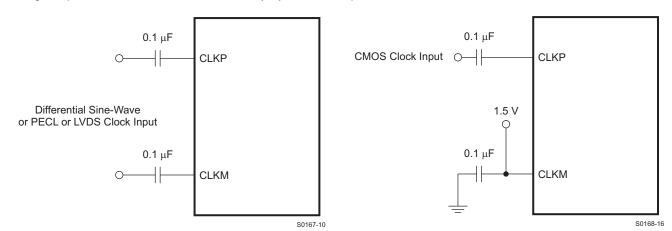


Figure 68. Differential Clock Driving Circuit

Figure 69. Single-Ended Clock Driving Circuit



FINE GAIN CONTROL

The ADS61B49/29 include gain settings that can be used to get improved SFDR performance (compared to no gain) or to reduce the required full-scale input voltage. The gain is programmable from 0 dB to 6 dB (in 0.5-dB steps). For each gain setting, the analog input full-scale range scales proportionally, as shown in Table 10.

The SFDR improvement is achieved at the expense of SNR; for each gain setting, the SNR degrades about 0.5–1 dB. The SNR degradation is less at high input frequencies. As a result, the fine gain is useful at high input frequencies as the SFDR improvement is significant with marginal degradation in SNR.

So, the fine gain can be used to trade-off between SFDR and SNR. Note that the default gain after reset is 0 dB.

GAIN, dB	TYPE	FULL-SCALE, V _{PP}				
0	Default after reset	2 V				
1	Fine, programmable	1.78				
2		1.59				
3		1.42				
4		1.26				
5		1.12				
6		1.00				

Table 10. Full-Scale Range Across Gains

OFFSET CORRECTION

The ADS61B49/29 have an internal offset correction algorithm that estimates and corrects the dc offset up to ±10 mV. The correction can be enabled using the serial register bit <ENABLE OFFSET CORR>. Once enabled, the algorithm estimates the channel offset and applies the correction every clock cycle. The time constant of the correction loop is a function of the sampling clock frequency. The time constant can be controlled using register bits <OFFSET CORR TIME CONSTANT> as described in Table 11.

After the offset is estimated, the correction can be locked in by setting <OFFSET CORR TIME CONSTANT> = 0. Once locked, the last estimated value is used for offset correction every clock cycle. Note that offset correction is disabled by default after a reset.

Figure 70 shows the time response of the offset correction algorithm, after it is enabled.

Table 11. Time Constant of Offset Correction Algorithm

<offset constant="" corr="" time=""> D3-D0</offset>	TIME CONSTANT (T _{CCLK}), NUMBER OF CLOCK CYCLES	TIME CONSTANT, sec $(T_{CCLK} \times 1/F_s)^{(1)}$ 1 ms		
0000	256 k			
0001	512 k	2 ms		
0010	1 M	4 ms		
0011	2 M	8 ms		
0100	4 M	17 ms		
0101	8 M	33 ms		
0110	16 M	67 ms		
0111	32 M	134 ms		
1000	64 M	268 ms		
1001	128 M	536 ms		
1010	256 M	1.1 s		
1011	512 M	2.2 s		
1100	Reserved	-		
1101	Reserved	-		
1110	Reserved	-		

(1) Sampling frequency, $F_s = 250 \text{ MSPS}$



Table 11. Time Constant of Offset Correction Algorithm (continued)

<offset constant="" corr="" time=""> D3-D0</offset>		TIME CONSTANT (T _{CCLK}), NUMBER OF CLOCK CYCLES	TIME CONSTANT, sec (T _{CCLK} x 1/F _s) ⁽¹⁾		
	1111	Reserved	_		

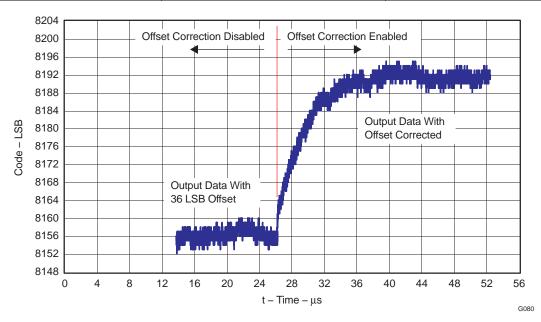


Figure 70. Output Code Time Response with Offset Correction Enabled

POWER DOWN

The ADS61B49/29 have three power-down modes – power-down global, standby, and output buffer disable.

Power-Down Global

In this mode, the entire chip including the A/D converter, the internal reference, and the output buffers are powered down resulting in reduced total power dissipation of about 20 mW. The output buffers are in a high impedance state. The wake-up time from global power down to data becoming valid in normal mode is typically $25 \, \mu s$.

This can be controlled using register bit **<PDN GLOBAL>** or using the SDATA pin (in parallel configuration mode).

Standby

Here, only the A/D converter is powered down and the internal references are active, resulting in a fast wake-up time of 300 ns. The total power dissipation in standby is about 120 mW.

This can be controlled using register bit <STANDBY>.

Output Buffer Disable

The output buffers can be disabled and put in a high impedance state – wakeup time from this mode is fast, about 40 ns. This can be controlled using register bit **<PDN OBUF>**.

Input Clock Stop

In addition to the above, the converter enters a low-power mode when the input clock frequency falls below 1 MSPS. The power dissipation is about 120 mW.



POWER SUPPLY SEQUENCE

During power-up, the AVDD and DRVDD supplies can come up in any sequence. The two supplies are separated in the device.

DIGITAL OUTPUT INFORMATION

The ADS61B49/29 provide 14-bit/12-bit data and an output clock synchronized with the data.

Output Interface

Two output interface options are available – double data rate (DDR) LVDS and parallel CMOS. They can be selected using the serial interface register bit **<ODI>** or using the DFS pin in parallel configuration mode.

DDR LVDS Outputs

In this mode, the data bits and clock are output using low voltage differential signal (LVDS) levels. Two data bits are multiplexed and output on each LVDS differential pair.

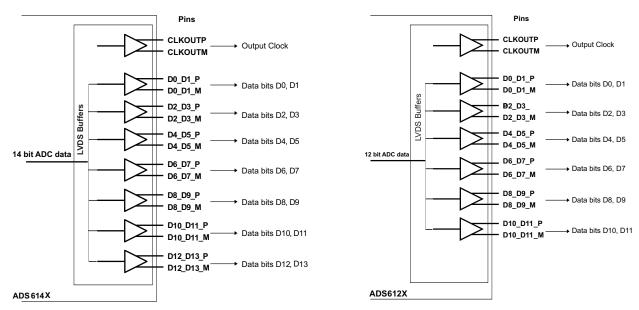


Figure 71. 14-Bit ADC LVDS Outputs

Figure 72. 12-Bit ADC LVDS Outputs

Even data bits D0, D2, D4... are output at the falling edge of CLKOUTP, and the odd data bits D1, D3, D5... are output at the rising edge of CLKOUTP. Both the rising and falling edges of CLKOUTP have to be used to capture all of the data bits (see Figure 73).



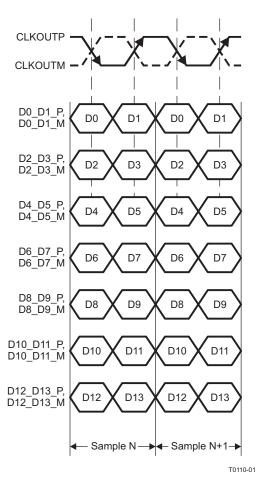
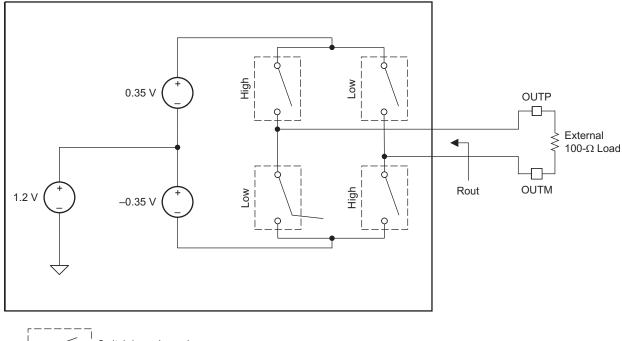


Figure 73. DDR LVDS Interface

LVDS Buffer

The equivalent circuit of each LVDS output buffer is shown in Figure 74. The buffer is designed to present an output impedance of 100 Ω (Rout). The differential outputs can be terminated at the receive end by a 100- Ω termination. The buffer output impedance behaves like a source-side series termination. By absorbing reflections from the receiver end, it helps to improve signal integrity. Note that this internal termination cannot be disabled and its value cannot be changed.



Switch impedance is nominally 50 Ω (±10%)

When the High switches are closed, OUTP = 1.375 V, OUTM = 1.025 V When the Low switches are closed, OUTP = 1.025 V, OUTM = 1.375 V When the High (or Low) switches are closed, Rout = 100 Ω

S0374-02

Figure 74. LVDS Buffer Equivalent Circuit

Parallel CMOS Interface

In CMOS mode, each data bit is output on a separate pin as a CMOS voltage level, every clock cycle. The rising edge of the output clock CLKOUT can be used to latch data in the receiver (for sampling frequencies up to approximately 150 MSPS).

Up to 150 MSPS, the setup and hold timings of the output data with respect to CLKOUT are specified. It is recommended to minimize the load capacitance seen by data and clock output pins by using short traces to the receiver. Also, match the output data and clock traces to minimize the skew between them.

For sampling frequencies > 150 MSPS in CMOS mode, it is recommended to use an external clock to capture data. The input clock to output data delay and data valid times are specified for the higher sampling frequencies. These timings can be used to delay the input clock appropriately and use it to capture the data (see Figure 4). It is recommended to consider using the LVDS output mode at high sample rates due to device and board noise generated by the CMOS mode.



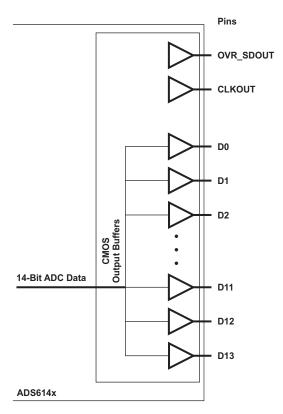


Figure 75. CMOS Output Interface

Output Buffer Strength Programmability

Switching noise (caused by CMOS output data transitions) can couple into the analog inputs during the instant of sampling and degrade the SNR. The coupling and SNR degradation increases as the output buffer drive is made stronger. To minimize this, the CMOS output buffers are designed with a controlled drive strength to achieve the best SNR. The default drive strength also ensures a wide data stable window for load capacitances up to 5 pF.

CMOS Interface Power Dissipation

With CMOS outputs, the DRVDD current scales with the sampling frequency and the load capacitance on every output pin. The maximum DRVDD current occurs when each output bit toggles between 0 and 1 every clock cycle. In an actual application, the DRVDD current would be determined by the average number of output bits switching, which is a function of the sampling frequency and the nature of the analog input signal.

Digital current due to CMOS output switching = $C_1 \times DRVDD \times (N \times F_{AVG})$,

where

 C_1 = load capacitance,

N x F_{AVG} = average number of output bits switching.

Figure 54 shows the current across the sampling frequencies with a 3-MHz analog input frequency.

Output Data Format

Two output data formats are supported – 2s complement and offset binary. They can be selected using the serial interface register bit **<DATA FORMAT>** or controlling the DFS pin in parallel configuration mode.

In the event of an input voltage overdrive, the digital outputs go to the appropriate full-scale level. For a positive overdrive, the output code is 0x3FFF in offset binary output format, and 0x1FFF in 2s complement output format. For a negative input overdrive, the output code is 0x0000 in offset binary output format and 0x2000 in 2s complement output format.



BOARD DESIGN CONSIDERATIONS

Grounding

A single ground plane is sufficient to achieve good performance, provided the analog, digital, and clock sections of the board are cleanly partitioned. See the EVM User Guide for details on layout and grounding.

Supply Decoupling

As the ADS61B49/29 already include internal decoupling, minimal external decoupling can be used without a loss in performance. Note that decoupling capacitors can help filter external power supply noise, so the optimum number of capacitors depends on the actual application. The decoupling capacitors should be placed very close to the converter supply pins.

Exposed Pad

In addition to providing a path for heat dissipation, the pad is also electrically connected to digital ground internally. So, it is necessary to solder the exposed pad to the ground plane for best thermal and electrical performance.

For detailed information, see the application notes for QFN Layout Guidelines (SLOA122) and QFN/SON PCB Attachment (SLUA271).



DEFINITION OF SPECIFICATIONS

Analog Bandwidth – The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low frequency value.

Aperture Delay – The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs. This delay will be different across channels. The maximum variation is specified as aperture delay variation (channel-channel).

Aperture Uncertainty (Jitter) - The sample-to-sample variation in aperture delay.

Clock Pulse Width/Duty Cycle – The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

Maximum Conversion Rate – The maximum sampling rate at which certified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate – The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL) – An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

Integral Nonlinearity (INL) – The INL is the deviation of the ADC transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

Gain Error – Gain error is the deviation of the ADC actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range. Gain error has two components: error due to reference inaccuracy and error due to the channel. Both these errors are specified independently as E_{GREF} and E_{GCHAN} .

To a first order approximation, the total gain error is E_{TOTAL} ~ E_{GREF} + E_{GCHAN}.

For example, if $E_{TOTAL} = \pm 0.5\%$, the full-scale input varies from (1-0.5/100) x FS_{ideal} to (1 + 0.5/100) x FS_{ideal}

Offset Error – The offset error is the difference, given in number of LSBs, between the actual average idle channel output code and the ideal average idle channel output code of the ADC. This quantity is often mapped into mV.

Temperature Drift – The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from T_{MIN} to T_{MAX} . It is calculated by dividing the maximum deviation of the parameter across the T_{MIN} to T_{MAX} range by the difference T_{MAX} – T_{MIN} .

Signal-to-Noise Ratio – SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N) , excluding the power at DC and the first nine harmonics.

$$SNR = 10Log^{10} \frac{P_S}{P_N}$$
 (1)

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the full-scale range of the converter.

Signal-to-Noise and Distortion (SINAD) – SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$SINAD = 10Log^{10} \frac{P_S}{P_N + P_D}$$
 (2)

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the full-scale range of the converter.

Effective Number of Bits (ENOB) – The ENOB is a measure of the converter performance as compared to the theoretical limit based on quantization noise.



$$ENOB = \frac{SINAD - 1.76}{6.02} \tag{3}$$

Total Harmonic Distortion (THD) – THD is the ratio of the power of the fundamental (P_S) to the power of the first nine harmonics (PD).

$$THD = 10Log^{10} \frac{P_S}{P_N}$$
 (4)

THD is typically given in units of dBc (dB to carrier).

Spurious-Free Dynamic Range (SFDR) – The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion – IMD3 is the ratio of the power of the fundamental (at frequencies f1 and f2) to the power of the worst spectral component at either frequency 2f1–f2 or 2f2–f1. IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

DC Power Supply Rejection Ratio (DC PSRR) – The DC PSSR is the ratio of the change in offset error to a change in analog supply voltage. The DC PSRR is typically given in units of mV/V.

AC Power Supply Rejection Ratio (AC PSRR) – AC PSRR is the measure of rejection of variations in the supply voltage by the ADC. If ΔV_{SUP} is the change in supply voltage and ΔV_{OUT} is the resultant change of the ADC output code (referred to the input), then

PSRR =
$$20Log^{10} \frac{\Delta V_{OUT}}{\Delta V_{SUP}}$$
 (Expressed in dBc) (5)

Voltage Overload Recovery – The number of clock cycles taken to recover to less than 1% error after an overload on the analog inputs. This is tested by separately applying a sine wave signal with 6dB positive and negative overload. The deviation of the first few samples after the overload (from their expected values) is noted.

Common Mode Rejection Ratio (CMRR) – CMRR is the measure of rejection of variation in the analog input common-mode by the ADC. If ΔV_{CM_IN} is the change in the common-mode voltage of the input pins and ΔV_{OUT} is the resultant change of the ADC output code (referred to the input), then

CMRR =
$$20\text{Log}^{10} \frac{\Delta V_{\text{OUT}}}{\Delta V_{\text{CM}}}$$
 (Expressed in dBc) (6)

Cross-Talk (only for multi-channel ADC)— This is a measure of the internal coupling of a signal from adjacent channel into the channel of interest. It is specified separately for coupling from the immediate neighboring channel (near-channel) and for coupling from channel across the package (far-channel). It is usually measured by applying a full-scale signal in the adjacent channel. Cross-talk is the ratio of the power of the coupling signal (as measured at the output of the channel of interest) to the power of the signal applied at the adjacent channel input. It is typically expressed in dBc.





www.ti.com

Changes from Revision A (December 2008) to Revision B					
•	Added OE input to ADS61B49 block diagram	2			
•	Added OE input to ADS61B29 block diagram	3			
•	Changed DFS pin number from 8 to 6 in Table 8	25			
•	Changed DFS pin number from 8 to 6 in Table 9.	28			

11-Nov-2025

www.ti.com

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(3)	(4)	(5)		(6)
ADS61B29IRGZR	Active	Production	VQFN (RGZ) 48	2500 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ61B29
ADS61B29IRGZR.A	Active	Production	VQFN (RGZ) 48	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ61B29
ADS61B29IRGZT	Active	Production	VQFN (RGZ) 48	250 SMALL T&R	Yes	NIPDAU NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ61B29
ADS61B29IRGZT.A	Active	Production	VQFN (RGZ) 48	250 SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ61B29
ADS61B49IRGZR	Active	Production	VQFN (RGZ) 48	2500 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ61B49
ADS61B49IRGZR.A	Active	Production	VQFN (RGZ) 48	2500 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ61B49
ADS61B49IRGZT	Active	Production	VQFN (RGZ) 48	250 SMALL T&R	Yes	NIPDAU NIPDAUAG	Level-3-260C-168 HR	-40 to 85	AZ61B49
ADS61B49IRGZT.A	Active	Production	VQFN (RGZ) 48	250 SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ61B49

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

www.ti.com 11-Nov-2025

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



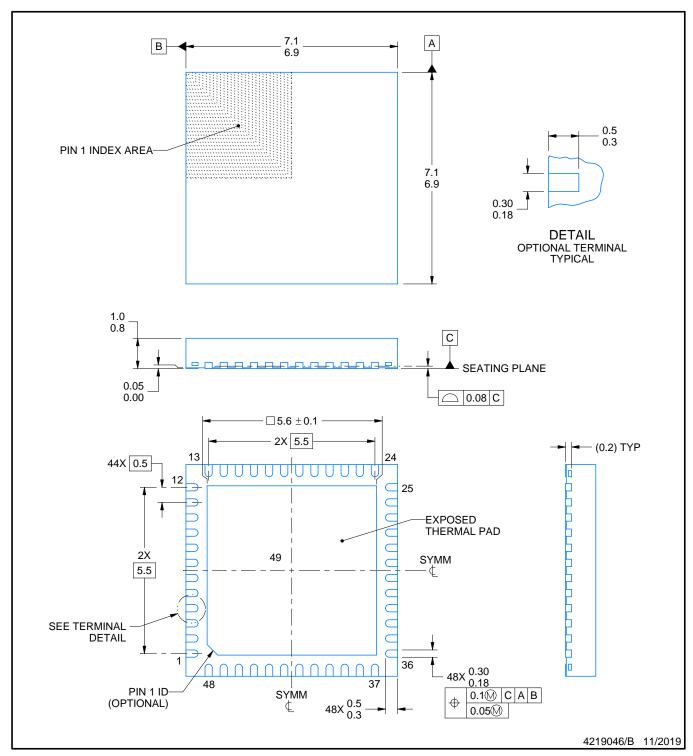
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4224671/A





PLASTIC QUAD FLATPACK - NO LEAD

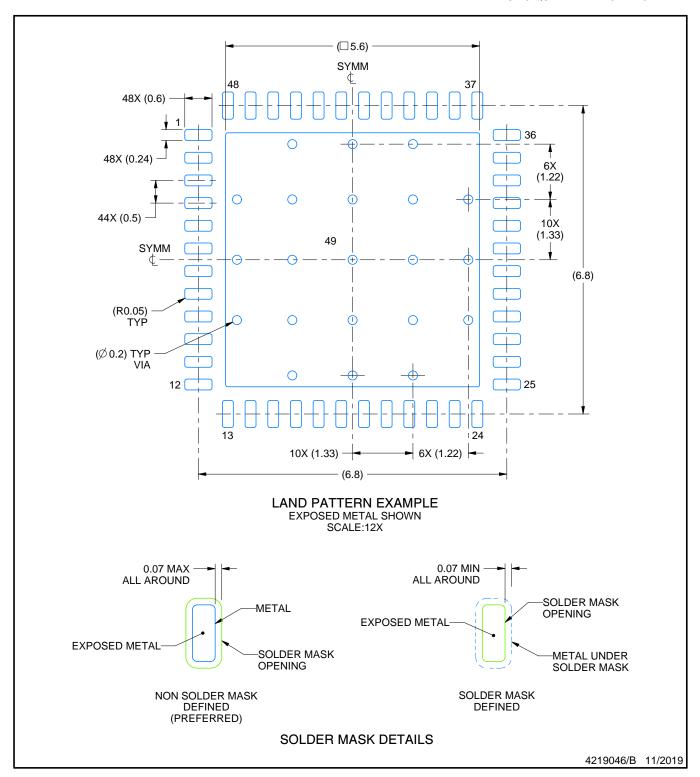


NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD

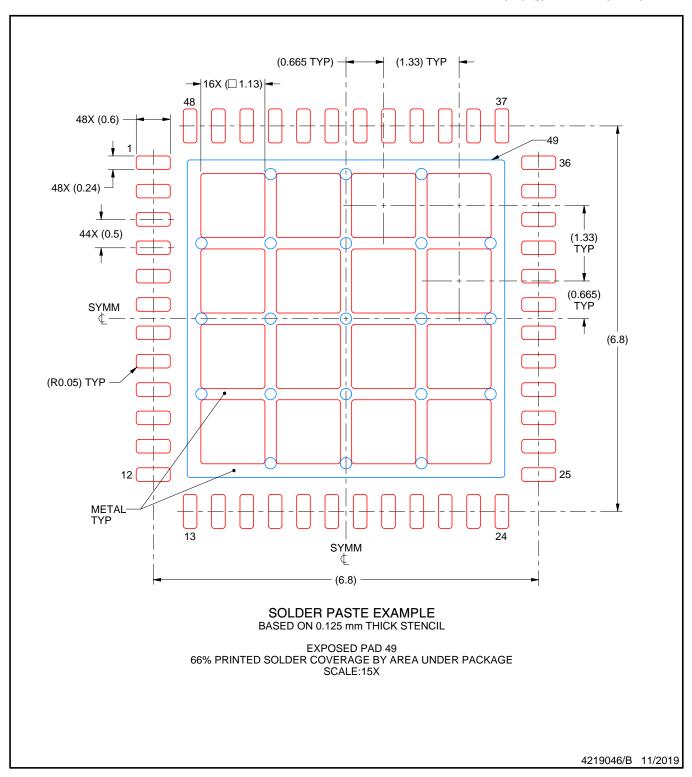


NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale, TI's General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025