

# ADS52J91 10-Bit, 12-Bit, 14-Bit, Multichannel, Low-Power, High-Speed ADC With LVDS, JESD Outputs

## 1 Features

- 16-Channel ADC configurable to convert 8, 16, or 32 inputs
- Maximum ADC Conversion Rate:
  - 125 MSPS in 10-bit mode
  - 100 MSPS in 12-bit mode
  - 65 MSPS in 14-bit mode
- Supplies: 1.2 V, 1.8 V
- Differential or single-ended input Clock
- Signal-to-noise ratio (SNR):
  - 61 dBFS in 10-bit mode
  - 69 dBFS in 12-bit mode
  - 73.5 dBFS in 14-Bit Mode
- Power at 125 MSPS: 48.6 mW/channel
- 16 ADCs configurable to convert:
  - 8 Inputs with a sampling rate of a 2X ADC conversion rate
  - 16 Inputs with a sampling rate of a 1X ADC conversion rate
  - 32 Inputs with a sampling rate of a 0.5X ADC conversion rate
- 1 Gbps LVDS interface with 16X, 14X, 12X, and 10X serialization
- 5 Gbps JESD interface:
  - JESD204B Subclass 0, 1, and 2
  - 2, 4, or 8 Channels per JESD lane
- Package: NFBGA-198 (9 mm × 15 mm)

## 2 Applications

- [Ultrasound imaging](#)
- [Portable instrumentation](#)
- [Sonar and Radar](#)
- [High-speed multichannel data acquisition](#)

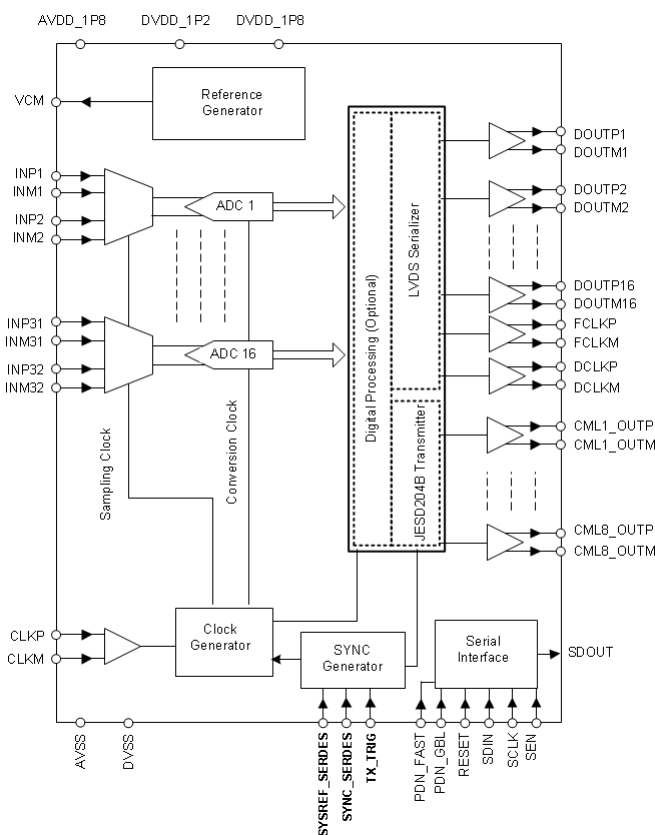
## 3 Description

The ADS52J91 is a low-power, high-performance, 16-channel, analog-to-digital converter (ADC). The conversion rate of each ADC goes up to a maximum of 125 MSPS in 10-bit mode. The maximum conversion rate reduces when the ADC resolution is set to a higher value.

The device can be configured to accept 8, 16, or 32 inputs. In 32-input mode, each ADC alternately samples and converts two different inputs each at an effective sampling rate that is half of the ADC conversion rate. In 8-bit input mode, two ADCs convert the same input in an interleaved manner, resulting in an effective sampling rate that is twice the ADC conversion rate. The ADC is designed to scale its power with the conversion rate.

### Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS52J91	NFBGA (198)	9.00 mm × 15.00 mm



Simplified Schematic



## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2021	*	Initial Release

## 5 Description (continued)

The ADC outputs are serialized and output through a low-voltage differential signaling (LVDS) interface along with a frame clock and a high-speed bit clock.

The device also has an optional JESD204B interface while operating in the 16-input and 32-input modes. This interface runs up to 5 Gbps

The device is available in a 9-mm × 15-mm, 0.8-mm pitch, NFBGA-198 package

## 6 Device and Documentation Support

### 6.1 Documentation Support

### 6.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 6.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 6.4 Trademarks

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### 6.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 6.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">ADS52J91ZZE</a>	Active	Production	NFBGA (ZZE)   198	160   JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	0 to 70	ADS52J91
ADS52J91ZZE.A	Active	Production	NFBGA (ZZE)   198	160   JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	0 to 70	ADS52J91

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TRAY**



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
ADS52J91ZZE	ZZE	NFBGA	198	160	10 x 16	150	315	135.9	7620	19.2	13.5	10.35
ADS52J91ZZE.A	ZZE	NFBGA	198	160	10 x 16	150	315	135.9	7620	19.2	13.5	10.35

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