

SBAS574A - JULY 2012-REVISED SEPTEMBER 2012

# Low-Cost, 8-Channel, Integrated Analog Front-End for Metering Applications

Check for Samples: ADS130E08

### **FEATURES**

- Eight Differential Current and Voltage Inputs
- Eight Low-Noise PGAs and Eight High-Resolution ADCs
- Exceeds Class 1.0 Performance
- CMRR: –110 dB
   Crosstalk: –105 dB
- THD: -108 dB
- Power: 750 µW/Channel
- Data Rates: 8 kSPS
- Programmable Gains (1, 2, and 8)
- DC Coupling:
  - Dual Supplies: +3 V to +5 V or +1.8 V to +3.6 V
  - Bipolar Supply: ±2.5 V
- Built-In Test Signals
- Fault Detection Comparators
- Four GPIO Pins
- Internal and External Reference
- Flexible Power-Down: STBY Mode
- SPI™ Data Interface
- Package: TQFP-64 (PAG)
- Operating Temperature Range: -40°C to +105°C

### **APPLICATIONS**

- Industrial Power Applications:
  - Three-Phase Metering
  - Industrial Applications

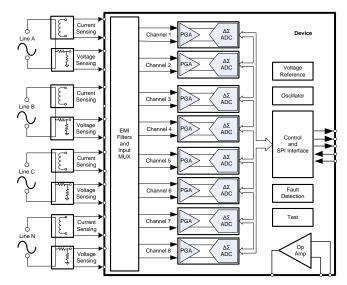
#### DESCRIPTION

The ADS130E08 is a multi-channel, simultaneous sampling, 16-bit, delta-sigma ( $\Delta\Sigma$ ) analog-to-digital converter (ADC) with a built-in programmable gain amplifier (PGA), internal reference, and an external oscillator interface.

The device incorporates commonly-required features in industrial metering applications. With high levels of integration and exceptional performance, the ADS130E08 enables the creation of scalable industrial power systems at significantly reduced size, power, and low overall cost.

The ADS130E08 has a flexible input multiplexer per channel that can be independently connected to the internally-generated signals for test, temperature, and fault detection. The ADS130E08 operates at a data rate of 8 kSPS. Fault detection can be implemented internal to the device using the integrated comparators with digital-to-analog converter (DAC)-controlled trigger levels.

Multiple devices can be cascaded in high channel count systems in a daisy-chain configuration. These complete analog front-end (AFE) solutions are packaged in a TQFP-64 package and specified over the industrial temperature range of -40°C to +105°C.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### FAMILY AND ORDERING INFORMATION(1)

PRODUCT	PACKAGE OPTION	NUMBER OF CHANNELS	ACCURACY	MAXIMUM SAMPLE RATE (kSPS)	OPERATING TEMPERATURE RANGE
ADS130E08	TQFP-64	8	Class 1.0	8	-40°C to +105°C
ADS131E04	TQFP-64	4	Class 0.1	64	-40°C to +105°C
ADS131E06	TQFP-64	6	Class 0.1	64	-40°C to +105°C
ADS131E08	TQFP-64	8	Class 0.1	64	-40°C to +105°C

<sup>(1)</sup> For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

### ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		VALUE	UNIT
AVDD to AVSS		-0.3 to +5.5	V
DVDD to DGND		-0.3 to +3.9	V
AVSS to DGND		-2.75 to +0.2	V
V <sub>REF</sub> input to AVSS		AVSS - 0.3 to AVDD + 0.3	V
Analog input to AVSS		AVSS - 0.3 to AVDD + 0.3	V
Digital input voltage to DV	DD	-0.3 to DVDD + 0.3	V
Digital output voltage to D	gital output voltage to DGND		V
lament accomment	Momentary	100	mA
Input current	Continuous	10	mA
	Operating, T <sub>A</sub>	-40 to +105	°C
Temperature	Storage, T <sub>stg</sub>	-60 to +150	°C
	Maximum junction, T <sub>J</sub>	+150	°C
Electrostatic discharge	Human body model (HBM) JEDEC standard 22, test method A114-C.01, all pins	±1000	V
(ESD) ratings	Charged device model (CDM) JEDEC standard 22, test method C101, all pins	±500	V

<sup>(1)</sup> Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

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### **ELECTRICAL CHARACTERISTICS**

Minimum and maximum specifications apply from  $-40^{\circ}$ C to  $+105^{\circ}$ C. Typical specifications are at  $+25^{\circ}$ C. All specifications are at DVDD = 1.8 V, AVDD = 3 V, AVSS = 0 V, V<sub>REF</sub> = 2.4 V, external f<sub>CLK</sub> = 2.048 MHz, data rate = 8 kSPS, and gain = 1, unless otherwise noted.

			ADS130E08		
	PARAMETER	TEST CONDITIONS	MIN TYP	MAX	UNIT
ANALOG	G INPUTS				
	Full-scale differential input voltage (AINP – AINN)		±V <sub>REF</sub> / gain		V
	Input common-mode range		See the <i>Input Common-Mode</i> subsection of the <i>PGA Setting</i> <i>Input Range</i> section		
Cı	Input capacitance		20		pF
I <sub>IB</sub>	Input bias current		2		nA
	DC input impedance		500		ΜΩ
PGA PE	RFORMANCE				
	Gain settings		1, 2, 8		
BW	Bandwidth		See Table 1		
ADC PE	RFORMANCE				
	Resolution	No missing codes	16		Bits
DR	Data rate	f <sub>CLK</sub> = 2.048 MHz	8		kSPS
CHANNE	EL PERFORMANCE (DC Performance)	,			
		G = 1	86 89		dB
	Dynamic range	G = 2 and 8	89		dB
INL	Integral nonlinearity	Full-scale with gain = 1, best fit	3		ppm
Eo	Offset error		±350		μV
	Offset error drift		0.6		μV/°C
E <sub>G</sub>	Gain error	Excluding voltage reference error	±0.1		% of FS
	Gain drift	Excluding voltage reference drift	3		ppm/°C
	Gain match between channels		0.2		% of FS
CHANNE	EL PERFORMANCE (AC Performance)	,			
CMRR	Common-mode rejection ratio	f <sub>CM</sub> = 50 Hz and 60 Hz <sup>(1)</sup>	-110		dB
PSRR	Power-supply rejection ratio	f <sub>PS</sub> = 50 Hz and 60 Hz	80		dB
	Crosstalk	f <sub>IN</sub> = 50 Hz and 60 Hz	-105		dB
	Accuracy	1:3000 dynamic range with a 1-second measurement (V <sub>RMS</sub> / I <sub>RMS</sub> )	0.5		%
SNR	Signal-to-noise ratio	f <sub>IN</sub> = 10-Hz input, -0.5 dBFs	89		dB
THD	Total harmonic distortion	10 Hz, -0.5 dBFs	-108		dB
OPEN-C	IRCUIT DETECT AND ALARM				
	Comparator threshold accuracy		±30		mV
EXTERN	IAL REFERENCE	·	<del></del>		
	B.(	AVDD = 3 V, V <sub>REF</sub> = (VREFP – VREFN)	2.5		V
V <sub>I(ref)</sub>	Reference input voltage	AVDD = 5 V, V <sub>REF</sub> = (VREFP - VREFN)	4		V
VREFN	Negative input		AVSS		V
VREFP	Positive input		AVSS + 2.5		V
	Input impedance		10		kΩ

<sup>(1)</sup> CMRR is measured with a common-mode signal of (AVSS + 0.3 V) to (AVDD – 0.3 V). The values indicated are the minimum of the eight channels.

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## **ELECTRICAL CHARACTERISTICS (continued)**

Minimum and maximum specifications apply from  $-40^{\circ}$ C to  $+105^{\circ}$ C. Typical specifications are at  $+25^{\circ}$ C. All specifications are at DVDD = 1.8 V, AVDD = 3 V, AVSS = 0 V, V<sub>REF</sub> = 2.4 V, external f<sub>CLK</sub> = 2.048 MHz, data rate = 8 kSPS, and gain = 1, unless otherwise noted.

				Α	DS130E08		
	PARAMETE	₹	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERA	TIONAL AMPLIFIER						
	Integrated noise		0.1 Hz to 100 Hz		7		$\mu V_{RMS}$
	Noise density		2 kHz		120		nV/√Hz
GBP	Gain bandwidth prod	uct	50 kΩ    10-pF load		100		kHz
SR	Slew rate		50 kΩ    10-pF load		0.25		V/µs
	Load current				50		μΑ
THD	Total harmonic distor	tion	f <sub>IN</sub> = 100 Hz		70		dB
CMIR	Common-mode input	range		AVSS + 0.7		AVSS - 0.3	V
	Quiescent power con	sumption			20		μΑ
INTERN	AL REFERENCE						
			CONFIG3.VREF_4V = 0		2.4		V
v <sub>0</sub>	Output voltage		CONFIG3.VREF_4V = 1		4		V
	V <sub>REF</sub> accuracy				±0.2		%
	Drift		-40°C to +105°C		45		ppm/°C
	Start-up time		Settled to 0.2%		150		ms
SYSTE	M MONITORS						
	Analog supply readin	g error			2		%
	Digital supply reading	error			2		%
	Device wake up		From power-up to DRDY low		150		ms
			STANDBY mode		125		μs
	Temperature sensor	Voltage	$T_A = +25^{\circ}C$		145		mV
	reading	Coefficient			490		μV/°C
TEST S	IGNAL		•	•		·	
	0: 11				f <sub>CLK</sub> / 2 <sup>21</sup>		Hz
	Signal frequency		See Register Map section for settings		f <sub>CLK</sub> / 2 <sup>20</sup>		Hz
		nal voltage See <i>Register Map</i> section for settings		±1		mV	
	Signal voltage			±2		mV	
	Accuracy				±2		%
CLOCK				1		<u> </u>	
			Nominal frequency		2.048		MHz
	Internal oscillator clos	ck frequency	T <sub>A</sub> = +25°C			±0.5	%
			-40°C ≤ T <sub>A</sub> ≤ +105°C			±2.5	%
	Internal oscillator star	rt-up time			20		μs
	Internal oscillator pov	-			120		μW
	External clock input f		CLKSEL pin = 0	0.7	2.048	2.25	MHz
DIGITAL	INPUT AND OUTPUT						
V <sub>IH</sub>	Logic level,	High		0.8 DVDD		DVDD + 0.1	V
V <sub>IL</sub>	input voltage	Low		-0.1		0.2 DVDD	V
V <sub>OH</sub>	Logic level,	High	I <sub>OH</sub> = -500 μA	0.9 DVDD			V
V <sub>OL</sub>	output voltage	Low	I <sub>OL</sub> = +500 μA	3.3 2 3 2		0.1 DVDD	V
I <sub>IN</sub>	Input current		0 V < V <sub>DigitalInput</sub> < DVDD	-10		+10	μA

## **ELECTRICAL CHARACTERISTICS (continued)**

Minimum and maximum specifications apply from  $-40^{\circ}$ C to  $+105^{\circ}$ C. Typical specifications are at  $+25^{\circ}$ C. All specifications are at DVDD = 1.8 V, AVDD = 3 V, AVSS = 0 V, V<sub>REF</sub> = 2.4 V, external f<sub>CLK</sub> = 2.048 MHz, data rate = 8 kSPS, and gain = 1, unless otherwise noted.

				AD	S130E08		
	PARAMETE	R	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER	S-SUPPLY REQUIREME	NTS				•	
AVDD	Analog supply	AVDD - AVSS		2.7	3	5.25	V
DVDD	Digital supply			1.7	1.8	3.6	V
	AVDD – DVDD			-2.1		3.6	V
SUPPL	Y CURRENT (Operation	nal Amplifier Turne	ed Off)				
			AVDD – AVSS = 3 V		1.8		mA
I <sub>AVDD</sub>	Name I am anation		AVDD – AVSS = 5 V		2.2		mA
	Normal operation		DVDD = 3.3 V		0.5		mA
I <sub>DVDD</sub>			DVDD = 1.8 V		0.3		mA
POWER	DISSIPATION						
	Quiescent power dissipation (analog supply = 3 V)		Normal mode		6	6.6	mW
			Power-down mode		10		μW
			Standby mode		2		mW
			Normal mode		11.5		mW
	Quiescent power dis- (analog supply = 5 V		Power-down mode		20		μW
	(arraiog suppry = 5 V)		Standby mode		4		mW
TEMPE	RATURE						
	Specified			-40		+105	°C
	Temperature range	Operating		-40		+105	°C
		Storage		-60		+150	°C

### THERMAL INFORMATION

		ADS130E08	
	THERMAL METRIC <sup>(1)</sup>	PAG (TQFP)	UNITS
		64 PINS	
$\theta_{JA}$	Junction-to-ambient thermal resistance	35	
$\theta_{JCtop}$	Junction-to-case (top) thermal resistance	31	
$\theta_{JB}$	Junction-to-board thermal resistance	26	00/11/
ΨЈТ	Junction-to-top characterization parameter	0.1	°C/W
ΨЈВ	Junction-to-board characterization parameter	NA	
$\theta_{\text{JCbot}}$	Junction-to-case (bottom) thermal resistance	NA	

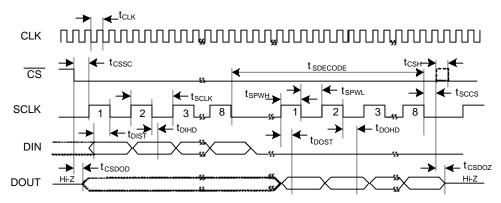
(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

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#### PARAMETER MEASUREMENT INFORMATION

### **TIMING CHARACTERISTICS**



NOTE: SPI settings are CPOL = 0 and CPHA = 1.

Figure 1. Serial Interface Timing

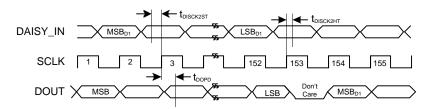


Figure 2. Daisy-Chain Interface Timing

### Timing Requirements For Figure 1 and Figure 2<sup>(1)</sup>

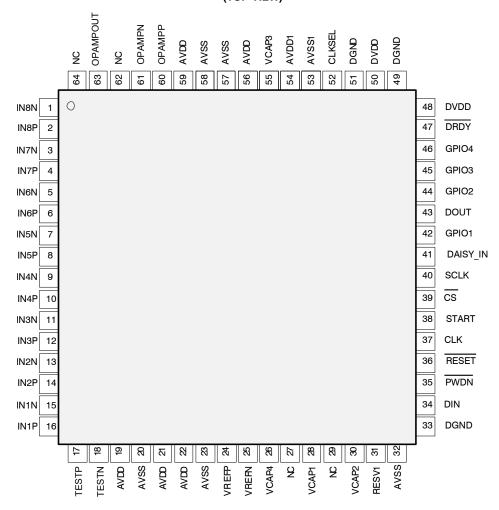
		2.7 V ≤ DVDD	≤ 3.6 V	1.7 V ≤ DVDD	≤ 2.0 V	
PARAMETER	DESCRIPTION	MIN	MAX	MIN	MAX	UNIT
t <sub>CLK</sub>	Master clock period	414	514	414	514	ns
t <sub>CSSC</sub>	CS low to first SCLK: setup time	6		17		ns
t <sub>SCLK</sub>	SCLK period	50		66.6		ns
t <sub>SPWH, L</sub>	SCLK pulse width, high and low	15		25		ns
t <sub>DIST</sub>	DIN valid to SCLK falling edge: setup time	10		10		ns
t <sub>DIHD</sub>	Valid DIN after SCLK falling edge: hold time	10		11		ns
t <sub>DOHD</sub>	SCLK falling edge to invalid DOUT: hold time	10		10		ns
t <sub>DOST</sub>	SCLK rising edge to DOUT valid: setup time		17		32	ns
t <sub>CSH</sub>	CS high pulse	2		2		t <sub>CLKs</sub>
t <sub>CSDOD</sub>	CS low to DOUT driven	10		20		ns
t <sub>sccs</sub>	Eighth SCLK falling edge to CS high	4		4		t <sub>CLKs</sub>
t <sub>SDECODE</sub>	Command decode time	4		4		t <sub>CLKs</sub>
t <sub>CSDOZ</sub>	CS high to DOUT Hi-Z		10		20	ns
t <sub>DISCK2ST</sub>	Valid DAISY_IN to SCLK rising edge: setup time	10		10		ns
t <sub>DISCK2HT</sub>	Valid DAISY_IN after SCLK rising edge: hold time	10		10		ns

(1) Specifications apply from  $-40^{\circ}$ C to  $+105^{\circ}$ C. Load on DOUT = 20 pF ||  $100 \text{ k}\Omega$ , unless otherwise noted.



### **PIN CONFIGURATION**

#### PAG PACKAGE TQFP-64 (TOP VIEW)



#### **PIN ASSIGNMENTS**

FIN ASSIGNMENTS					
NAME	TERMINAL	FUNCTION	DESCRIPTION		
AVDD	19, 21, 22, 56, 59	Supply	Analog supply		
AVDD1	54	Supply	Charge pump analog supply		
AVSS	20, 23, 32, 57, 58	Supply	Analog ground		
AVSS1	53	Supply	Charge pump analog ground		
CLK	37	Digital input	Master clock input		
CLKSEL	52	Digital input	Master clock select		
CS	39	Digital input	SPI chip select; active low		
DAISY_IN	41	Digital input	Daisy-chain input		
DGND	33, 49, 51	Supply	Digital ground		
DIN	34	Digital input	SPI data in		
DOUT	43	Digital output	SPI data out		
DRDY	47	Digital output	Data ready; active low		
DVDD	48, 50	Supply	Digital power supply		
GPIO1	42	Digital input/output	General-purpose input/output pin		

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## **PIN ASSIGNMENTS (continued)**

NAME	TERMINAL	FUNCTION	DESCRIPTION
GPIO2	44	Digital input/output	General-purpose input/output pin
GPIO3	45	Digital input/output	General-purpose input/output pin
GPIO4	46	Digital input/output	General-purpose input/output pin
IN1N <sup>(1)</sup>	15	Analog input	Differential analog negative input 1
IN1P	16	Analog input	Differential analog positive input 1
IN2N	13	Analog input	Differential analog negative input 2
IN2P	14	Analog input	Differential analog positive input 2
IN3N	11	Analog input	Differential analog negative input 3
IN3P	12	Analog input	Differential analog positive input 3
IN4N	9	Analog input	Differential analog negative input 4
IN4P	10	Analog input	Differential analog positive input 4
IN5N	7	Analog input	Differential analog negative input 5
IN5P	8	Analog input	Differential analog positive input 5
IN6N	5	Analog input	Differential analog negative input 6
IN6P	6	Analog input	Differential analog positive input 6
IN7N	3	Analog input	Differential analog negative input 7
IN7P	4	Analog input	Differential analog positive input 7
IN8N	1	Analog input	Differential analog negative input 8
IN8P	2	Analog input	Differential analog positive input 8
NC	27, 29, 62, 64	_	No connection, leave floating
OPAMPN	61	Analog	Op amp inverting input
OPAMPOUT	63	Analog	Op amp output
OPAMPP	60	_	Op amp noninverting input
PWDN	35	Digital input	Power-down; active low
RESET	36	Digital input	System reset; active low
RESV1	31	Digital input	Reserved for future use; must tie to logic low (DGND)
SCLK	40	Digital input	SPI clock
START	38	Digital input	Start conversion
TESTN <sup>(2)</sup>	18	Analog output	Internal test signal
TESTP	17	Analog output	Internal test signal
VCAP1	28	Analog input and output	Analog bypass capacitor
VCAP2	30	_	Analog bypass capacitor
VCAP3	55	_	Analog bypass capacitor
VCAP4	26	Analog output	Analog bypass capacitor
VREFN	25	Analog input	Negative reference voltage
VREFP	24	Analog input and output	Positive reference voltage

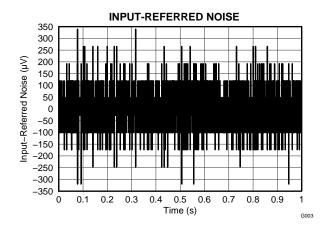
<sup>(1)</sup> Connect unused IN1x to IN8x terminals to AVDD.

<sup>(2)</sup> Connect unused TESTx terminals to AVDD.



#### TYPICAL CHARACTERISTICS

All plots are at  $T_A = +25$ °C, AVDD = 3 V, AVSS = 0 V, DVDD = 1.8 V, internal VREFP = 2.4 V, VREFN = AVSS, external clock = 2.048 MHz, data rate = 8 kSPS, and gain = 1, unless otherwise noted.



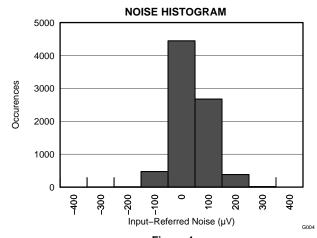
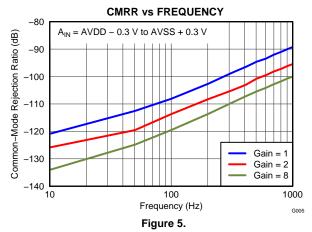
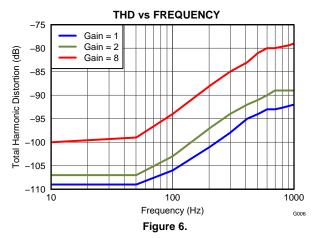


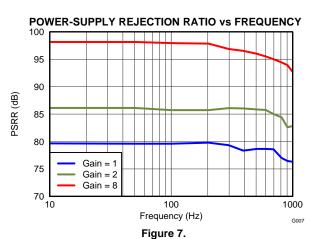
Figure 3.

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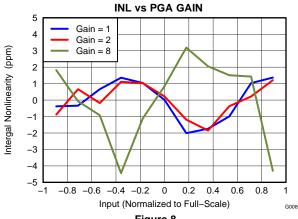
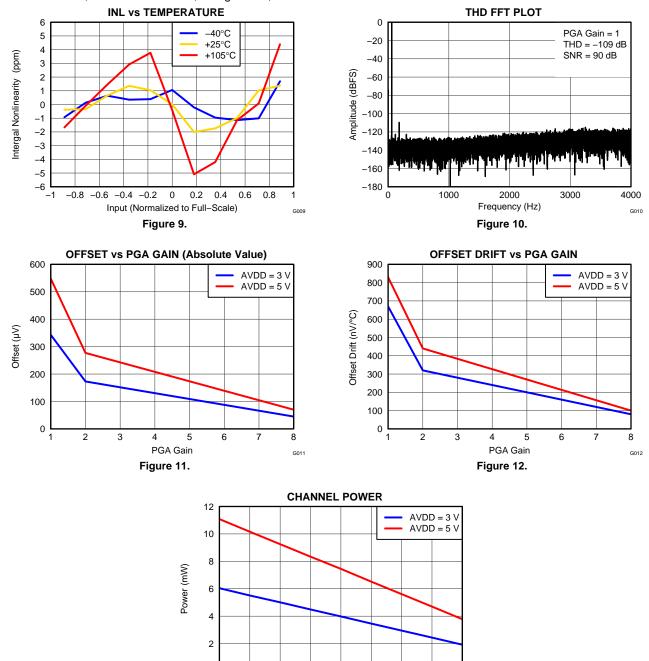


Figure 8.



### TYPICAL CHARACTERISTICS (continued)

All plots are at  $T_A = +25$ °C, AVDD = 3 V, AVSS = 0 V, DVDD = 1.8 V, internal VREFP = 2.4 V, VREFN = AVSS, external clock = 2.048 MHz, data rate = 8 kSPS, and gain = 1, unless otherwise noted.



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Number of Channels Diasbled

Figure 13.

8

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#### **OVERVIEW**

The ADS130E08 is a low-power, multichannel, simultaneously-sampling, 16-bit, delta-sigma ( $\Delta\Sigma$ ) analog-to-digital converter (ADC) with an integrated programmable gain amplifier (PGA). This functionality make the ADS130E08 suitable for industrial power-metering applications.

The ADS130E08 has a highly-programmable multiplexer that allows for temperature, supply, and input short measurements. PGA gain can be chosen from one of three settings (1, 2, and 8). The ADCs in the device offer a data rate of 8 kSPS. Communication to the device is accomplished using an SPI-compatible interface. The device provides four general-purpose IO (GPIO) pins for general use. Multiple devices can be synchronized using the START pin.

The internal reference can be programmed to either 2.4 V or 4 V. Fault detection can be accomplished by using the integrated comparators, with programmable trigger-point settings. A detailed diagram of the ADS130E08 is shown in Figure 14.

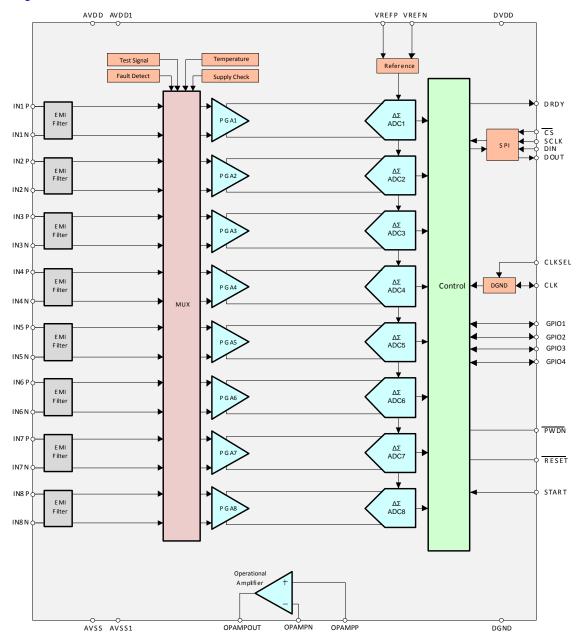


Figure 14. Functional Block Diagram

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#### THEORY OF OPERATION

This section contains details of the ADS130E08 internal functional elements. The analog blocks are discussed first, followed by the digital interface. Blocks implementing power-specific functions are covered towards the end of this document.

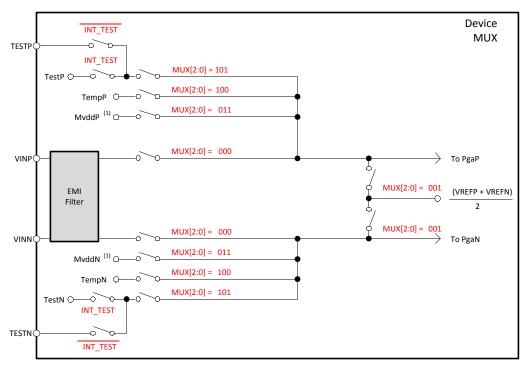
Throughout this document,  $f_{CLK}$  denotes the CLK pin signal frequency,  $t_{CLK}$  denotes the CLK pin signal period,  $f_{DR}$  denotes the output data rate,  $t_{DR}$  denotes the output data time period, and  $f_{MOD}$  denotes the frequency at which the modulator samples the input.

#### **EMI FILTER**

An RC filter at the input acts as an electromagnetic interference (EMI) filter on all channels. The -3-dB filter bandwidth is approximately 3 MHz.

#### **INPUT MULTIPLEXER**

The ADS130E08 input multiplexers are very flexible and provide many configurable signal-switching options. Figure 15 shows a diagram of the multiplexer on a single channel of the device. VINP and VINN are separate for each of the eight blocks. This flexibility allows for significant device and sub-system diagnostics, calibration, and configuration. Switch settings for each channel are selected by writing the appropriate values to the CHnSET register (see the *CHnSET: Individual Channel Settings* (n = 1 to 8) Register in the *Register Map* section for details.)



(1) MVDD monitor voltage supply depends on channel number; see the Supply Measurements (MVDDP, MVDDN) section.

Figure 15. Input Multiplexer Block for One Channel

#### **Device Noise Measurements**

Setting CHnSET[2:0] = 001 sets the common-mode voltage of [(VREFP + VREFN) / 2] to both inputs of the channel. This setting can be used to test inherent device noise in the user system.

### Test Signals (TestP and TestN)

Setting CHnSET[2:0] = 101 provides internally-generated test signals for use in sub-system verification at power-up. Test signals are controlled through register settings (see the *CONFIG2: Configuration Register 2* subsection in the *Register Map* section for details). TEST\_AMP controls the signal amplitude and TEST\_FREQ controls switching at the required frequency. The test signals are multiplexed and transmitted out of the device at the TESTP and TESTN pins. A bit register (CONFIG2.INT\_TEST = 0) deactivates the internal test signals so that the test signal can be driven externally. This feature allows the calibration of multiple devices with the same signal.

### Temperature Sensor (TempP, TempN)

The ADS130E08 contains an on-chip temperature sensor. This sensor uses two internal diodes with one diode having a current density 16x that of the other, as shown in Figure 16. The difference in diode current densities yields a difference in voltage that is proportional to absolute temperature.

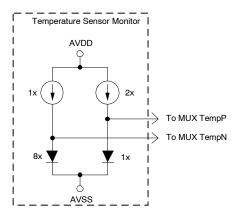


Figure 16. Temperature Sensor Measurement in the Input

As a result of the low thermal resistance of the package to the printed circuit board (PCB), the internal device temperature tracks the PCB temperature closely. Note that self-heating of the ADS130E08 causes a higher reading than the temperature of the surrounding PCB.

The scale factor of Equation 1 converts the temperature reading to degrees Celsius. Before using this equation, the temperature reading code must first be scaled to microvolts.

Temperature (°C) = 
$$\left(\frac{\text{Temperature Reading }(\mu V) - 168,000 \ \mu V}{394 \ \mu V/^{\circ}C}\right) + 25^{\circ}C$$
(1)

### Supply Measurements (MVDDP, MVDDN)

Setting CHnSET[2:0] = 011 sets the channel inputs to different supply voltages of the device. For channels 1, 2, 5, 6, 7, and 8, (MVDDP – MVDDN) is [0.5(AVDD – AVSS)]; for channels 3 and 4, (MVDDP – MVDDN) is DVDD / 4. Note that to avoid saturating the PGA while measuring power supplies, the gain must be set to '1'.

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#### **ANALOG INPUT**

The ADS130E08 analog input is fully differential. Assuming PGA = 1, the input (INP – INN) can span between  $-V_{REF}$  to  $+V_{REF}$ . Refer to Table 3 for an explanation of the correlation between the analog input and the digital codes. There are two general methods of driving the ADS130E08 analog input: single-ended or differential, as shown in Figure 17 and Figure 18. Note that INP and INN are 180°C out-of-phase in the differential input method. When the input is single-ended, the INN input is held at the common-mode voltage, preferably at mid-supply. The INP input swings around the same common voltage and the peak-to-peak amplitude is (common-mode + 1/2  $V_{REF}$ ) and (common-mode – 1/2  $V_{REF}$ ). When the input is differential, the common-mode is given by (INP + INN) / 2. Both INP and INN inputs swing from (common-mode + 1/2  $V_{REF}$ ) to (common-mode – 1/2  $V_{REF}$ ). For optimal performance, it is recommended that the ADS130E08 be used in a differential configuration.

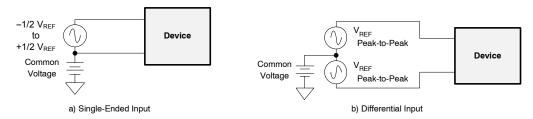


Figure 17. Methods of Driving the ADS130E08: Single-Ended or Differential

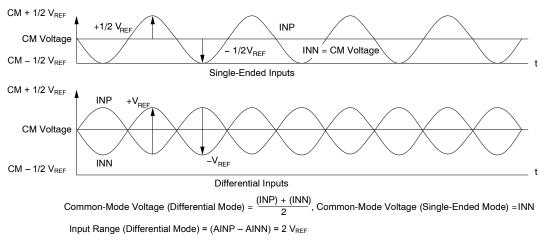


Figure 18. Using the ADS130E08 in Single-Ended and Differential Input Modes

#### **PGA SETTINGS AND INPUT RANGE**

The PGA is a differential input and output amplifier, as shown in Figure 19. The PGA has three gain settings (1, 2, and 8) that can be set by writing to the CHnSET register (see the *CHnSET: Individual Channel Settings (n = 1 to 8)* Register in the *Register Map* section for details). The ADS130E08 has CMOS inputs and, therefore, has negligible current noise. Table 1 shows the typical bandwidth values for various gain settings. Note that Table 1 only shows small-signal bandwidth. For large signals, performance is limited by PGA slew rate.

The PGA resistor string that implements the gain has 120 k $\Omega$  of resistance. This resistance provides a current path across the PGA outputs in the presence of a differential input signal. This current is in addition to the quiescent current specified for the device in the presence of a differential signal at the input.

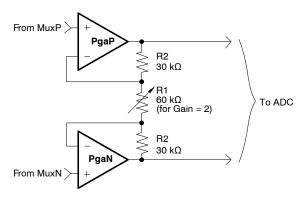


Figure 19. PGA Implementation

Table 1. PGA Gain versus Bandwidth

GAIN	NOMINAL BANDWIDTH AT ROOM TEMPERATURE (kHz)
1	237
2	146
8	48

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### Input Common-Mode Range

The usable input common-mode range of the analog front-end depends on various parameters, including the maximum differential input signal, supply voltage, and PGA gain. Equation 2 describes this range.

$$AVDD - 0.2 - \left(\frac{Gain\ V_{MAX\_DIFF}}{2}\right) > CM > AVSS + 0.2 + \left(\frac{Gain\ V_{MAX\_DIFF}}{2}\right)$$

where:

V<sub>MAX DIFF</sub> = maximum differential signal at the PGA input

$$CM = common-mode range$$
 (2)

For example:

If 
$$V_{DD}$$
 = 3.3 V, gain = 2, and  $V_{MAX\_DIFF}$  = 1000 mV,  
Then 1.2 V < CM < 2.1 V

### Input Differential Dynamic Range

The differential (INP – INN) signal range depends on the analog supply and reference used in the system. Equation 3 shows this range.

$$Max (INP - INN) < \frac{V_{REF}}{Gain} ; Full-Scale Range = \frac{\pm V_{REF}}{Gain} = \frac{2 V_{REF}}{Gain}$$
(3)

For higher dynamic range, a 5-V supply with a 4-V reference (set by the VREF\_4V bit of the CONFIG3: Configuration Register 3) can be used to increase the differential dynamic range.

#### **ADC ΔΣ Modulator**

Each ADS130E08 channel has a 16-bit,  $\Delta\Sigma$  ADC. This converter uses a second-order modulator optimized for low-power applications. The modulator samples the input signal at the rate of  $f_{MOD} = f_{CLK}$  / 8. As in the case of any  $\Delta\Sigma$  modulator, the ADS130E08 noise is shaped until  $f_{MOD}$  / 2, as shown in Figure 20. The on-chip digital decimation filters also provide antialias filtering. This feature of the  $\Delta\Sigma$  converters drastically reduces the complexity of analog antialiasing filters typically required with nyquist ADCs.

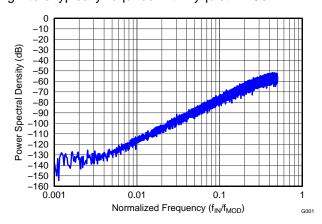


Figure 20. Modulator Noise Spectrum Up To 0.5 × f<sub>MOD</sub>

#### **DIGITAL DECIMATION FILTER**

The digital filter receives the modulator output and decimates the data stream. A fixed sample rate of 8 kSPS, for all eight channels, is provided for simplicity. The digital filter on each channel consists of a third-order sinc filter.

#### Sinc Filter Stage (sinx / x)

The sinc filter is a variable decimation rate, third-order, low-pass filter. Data are supplied to this section of the filter from the modulator at the rate of  $f_{MOD}$ . The sinc filter attenuates the high-frequency noise of the modulator, then decimates the data stream into parallel data. The decimation rate affects the overall data rate of the converter.

Equation 4 shows the scaled Z-domain transfer function of the sinc filter.

$$|H(z)| = \left| \frac{1 - Z^{-N}}{1 - Z^{-1}} \right|^{3}$$
 (4)

The frequency domain transfer function of the sinc filter is shown in Equation 5.

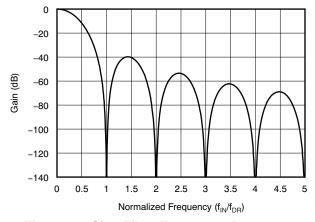
$$H(f) = \frac{\sin\left(\frac{N\pi f}{f_{MOD}}\right)}{N \times \sin\left(\frac{\pi f}{f_{MOD}}\right)}$$

where:

N = decimation ratio (5)



The sinc filter has notches (or zeroes) that occur at the output data rate and multiples thereof. At these frequencies, the filter has infinite attenuation. Figure 21 shows the sinc filter frequency response and Figure 22 shows the sinc filter roll-off. With a step change at the input, the filter takes 3  $t_{DR}$  to settle. After a START signal rising edge, the filter takes  $t_{SETTLE}$  time to output settled data. The settling time of the filters at various data rates is discussed in the START subsection of the SPI Interface section. Figure 23 and Figure 24 show the filter transfer function until  $t_{MOD}$  / 2 and  $t_{MOD}$  / 16, respectively, at different data rates. Figure 25 shows the transfer function extended until 4  $t_{MOD}$ . The ADS130E08 passband repeats at every  $t_{MOD}$ . The input R-C antialiasing filters in the system should be chosen such that any interference in frequencies around multiples of  $t_{MOD}$  is attenuated sufficiently.

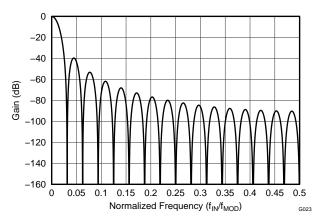


-0.5
-1
-1
-2
-2.5
-3
0 0.05 0.1 0.15 0.2 0.25 0.3 0.35

Normalized Frequency (f<sub>IN</sub>/f<sub>DR</sub>)

Figure 21. Sinc Filter Frequency Response

Figure 22. Sinc Filter Roll-Off



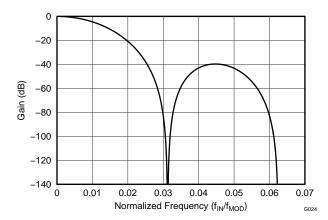


Figure 23. Transfer Function of On-Chip Decimation Filters Until f<sub>MOD</sub> / 2

Figure 24. Transfer Function of On-Chip Decimation Filters Until f<sub>MOD</sub> / 16

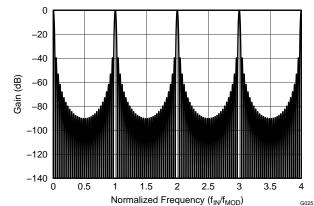
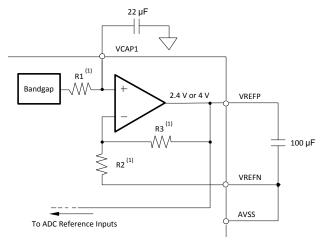


Figure 25. Transfer Function of On-Chip Decimation Filters Until 4  $f_{MOD}$  for DR[2:0] = 000 and DR[2:0] = 110

#### **REFERENCE**

Figure 26 shows a simplified block diagram of the ADS130E08 internal reference. The reference voltage is generated with respect to AVSS. When using the internal voltage reference, connect VREFN to AVSS.



(1) For  $V_{REF} = 2.4 \text{ V}$ :  $R1 = 12.5 \text{ k}\Omega$ ,  $R2 = 25 \text{ k}\Omega$ , and  $R3 = 25 \text{ k}\Omega$ . For  $V_{REF} = 4 \text{ V}$ :  $R1 = 10.5 \text{ k}\Omega$ ,  $R2 = 15 \text{ k}\Omega$ , and  $R3 = 35 \text{ k}\Omega$ .

Figure 26. Internal Reference

The external band-limiting capacitors determine the amount of reference noise contribution. For high-end systems, the capacitor values should be chosen such that the bandwidth is limited to less than 10 Hz so that the reference noise does not dominate system noise. When using a 3-V analog supply, the internal reference must be set to 2.4 V. In case of a 5-V analog supply, the internal reference can be set to 4 V by setting the VREF 4V bit in the CONFIG2: Configuration Register 2.

Alternatively, the internal reference buffer can be powered down and VREFP can be driven externally. Figure 27 shows a typical external reference driver circuitry. Power-down is controlled by the PD REFBUF bit in the CONFIG3: Configuration Register 3. This power-down is also used to share internal references when two devices are cascaded. By default, the device wakes up in external reference mode.

Product Folder Links: ADS130E08



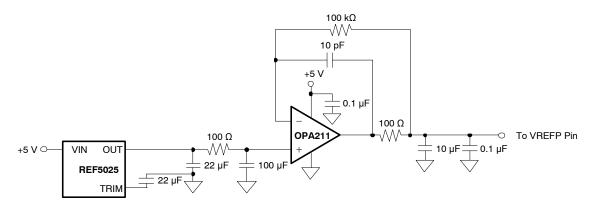


Figure 27. External Reference Driver

#### **CLOCK**

The ADS130E08 provides two device clocking methods: internal and external. Internal clocking is ideally suited for low-power, battery-powered systems. The internal oscillator is trimmed for accuracy at room temperature. Accuracy varies over the specified temperature range; refer to the Electrical Characteristics for details. Clock selection is controlled by the CLKSEL pin and CLK EN register bit.

The CLKSEL pin selects either the internal or external clock. The CLK\_EN bit in the CONFIG1 register enables and disables the oscillator clock to be output in the CLK pin. A truth table for these pins is shown in Table 2. The CLK\_EN bit is useful when multiple devices are used in a daisy-chain configuration. During power-down, the external clock is recommended to be shut down to save power.

Table 2. CLKSEL Pin and CLK\_EN Bit

CLKSEL PIN	CONFIG1.CLK_EN BIT	CLOCK SOURCE	CLK PIN STATUS
0	X	External clock	Input: external clock
1	0	Internal clock oscillator	3-state
1	1	Internal clock oscillator	Output: internal clock oscillator

### **DATA FORMAT**

The ADS130E08 outputs 16 bits of data per channel in binary twos complement format, MSB first. The LSB has a weight of  $[V_{REF} / (2^{15} - 1)]$ . A positive full-scale input produces an output code of 7FFFh and the negative full-scale input produces an output code of 8000h. The output clips at these codes for signals exceeding full-scale. Table 3 summarizes the ideal output codes for different input signals.

Table 3. Ideal Output Code versus Input Signal

INPUT SIGNAL, V <sub>IN</sub> (AINP – AINN)	IDEAL OUTPUT CODE(1)
≥ V <sub>REF</sub>	7FFFh
+V <sub>REF</sub> / (2 <sup>15</sup> – 1)	0001h
0	0000h
-V <sub>REF</sub> / (2 <sup>15</sup> - 1)	FFFFh
$\leq -V_{REF} (2^{15} / 2^{15} - 1)$	8000h

<sup>(1)</sup> Excludes effects of noise, linearity, offset, and gain error.

### **SPI INTERFACE**

The SPI-compatible serial interface consists of four signals:  $\overline{CS}$ , SCLK, DIN, and DOUT. The interface reads conversion data, reads and writes registers, and controls device operation. The  $\overline{DRDY}$  output is used as a status signal to indicate when data are ready.  $\overline{DRDY}$  goes low when new data are available.

## Chip Select (CS)

 $\overline{\text{CS}}$  selects the ADS130E08 for SPI communication.  $\overline{\text{CS}}$  must remain low for the entire serial communication duration. After the serial communication is finished, always wait four or more  $t_{\text{CLK}}$  cycles before taking  $\overline{\text{CS}}$  high. When  $\overline{\text{CS}}$  is taken high, the serial interface is reset, SCLK and DIN are ignored, and  $\overline{\text{DOUT}}$  enters a high-impedance state.  $\overline{\text{DRDY}}$  asserts when data conversion is complete, regardless of whether  $\overline{\text{CS}}$  is high or low.

#### Serial Clock (SCLK)

SCLK is the serial peripheral interface (SPI) serial clock. SCLK shifts commands in and shifts data out from the device. The serial clock features a Schmitt-triggered input and clocks data on the DIN and DOUT pins into and out of the ADS130E08.

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Care should be taken to prevent glitches on SCLK while  $\overline{CS}$  is low. Glitches as small as 1 ns wide could be interpreted as a valid serial clock. After eight serial clock events, the ADS130E08 assumes an instruction must be interrupted and executed. If it is suspected that instructions are being interrupted erroneously, toggle  $\overline{CS}$  high and back low to return the chip to normal operation. Issuing serial clocks in multiples of eight is also recommended. The absolute maximum SCLK limit is specified in the *Serial Interface Timing* table.

For a single device, the minimum speed needed for SCLK depends on the number of channels, number of bits of resolution, and output data rate. (For multiple cascaded devices, see the *Standard Mode* subsection of the *Multiple Device Configuration* section.) For example, at 8 kSPS, the minimum serial clock rate must be 1.3 MHz.

Data can be retrieved either by putting the device in RDATAC mode or by issuing an RDATA command for data on demand. The SCLK rate limitation, as described by Equation 6, applies to RDATAC mode. For the RDATA command, the limitation applies if data must be read in between two consecutive DRDY signals. Equation 6 assumes that there are no other commands issued in between data captures.

$$t_{SCLK} < \frac{t_{DR} - 4 t_{CLK}}{152} \tag{6}$$

### Data Input (DIN)

The data input pin (DIN) is used along with SCLK to communicate with the ADS130E08 (using opcode commands and register data). The device latches data on DIN on the SCLK falling edge.

### **Data Output (DOUT)**

The data output pin (DOUT) is used with SCLK to read conversions and register data from the ADS130E08. Data on DOUT are shifted out on the SCLK rising edge. DOUT goes to a high-impedance state when  $\overline{CS}$  is high. In read data continuous mode (see the *SPI Command Definitions* section for more details), the DOUT output line also indicates when new data are available. This feature can be used to minimize the number of connections between the device and system controller. Figure 28 shows the data output protocol for the ADS130E08.

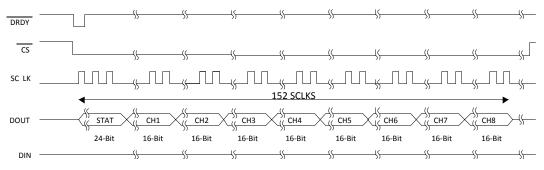


Figure 28. SPI Bus Data Output

#### **Data Retrieval**

Data retrieval can be accomplished in one of two methods. The read data continuous command (see the RDATAC: Read Data Continuous section) can be used to set the device in a mode to read data continuously without sending opcodes. The read data command (see the RDATA: Read Data section) can be used to read just one data output from the device (see the SPI Command Definitions section for more details). Conversion data are read by shifting data out on DOUT. The MSB of the data on DOUT is clocked out on the first SCLK rising edge. DRDY returns to high on the first SCLK falling edge. DIN should remain low for the entire read operation.

The number of bits in the data output depends on the number of channels and the number of bits per channel. For the ADS130E08, the number of data outputs is [(24 status bits + 16 bits × 8 channels) = 152 bits]. The format of the 24 status bits is (1100 + FAULT\_STATP + FAULT\_STATN + bits[7:4] of the *GPIO: General-Purpose IO Register*). The data format for each channel data is twos complement, MSB first. When channels are powered down using user register settings, the corresponding channel output is set to '0'. However, the channel output sequence remains the same.

22 Suk

The ADS130E08 also provides a multiple readback feature. Data can be read out multiple times by simply giving more SCLKs, in which case the MSB data byte repeats after reading the last byte. The DAISY\_IN bit in the CONFIG1: Configuration Register 1 must be set to '1' for multiple readbacks.

### Data Ready (DRDY)

DRDY is an output. When DRDY transitions low, new conversion data are ready. The CS signal has no effect on the data ready signal. DRDY behavior is determined by whether the device is in RDATAC mode or the RDATA command is being used to read data on demand. (See the RDATAC: Read Data Continuous and RDATA: Read Data subsections of the SPI Command Definitions section for further details). When reading data with the RDATA command, the read operation can overlap the next DRDY occurrence without data corruption.

The START pin or the START command is used to place the device either in normal data capture mode or pulse data capture mode. Figure 29 shows the relationship between DRDY, DOUT, and SCLK during data retrieval. DOUT is latched out at the SCLK rising edge; DRDY is pulled high at the SCLK falling edge. Note that DRDY goes high on the first SCLK falling edge, regardless of whether data are being retrieved from the device or a command is being sent through the DIN pin.

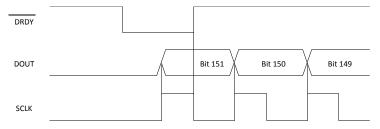


Figure 29.  $\overline{DRDY}$  with Data Retrieval ( $\overline{CS} = 0$ )

#### **GPIO**

The ADS130E08 has a total of four general-purpose digital input and output (GPIO) pins available in the normal mode of operation. The digital IO pins are individually configurable as either inputs or outputs through the GPIOC bits register. The GPIOD bits in the GPIO: General-Purpose IO Register control the level of the pins. When reading the GPIOD bits, the data returned are the logic level of the pins, whether they are programmed as inputs or outputs. When the GPIO pin is configured as an input, a write to the corresponding GPIOD bit has no effect. When configured as an output, a write to the GPIOD bit sets the output value.

If configured as inputs, these pins must be driven (do not float). The GPIO pins are set as inputs after power-on or after a reset. Figure 30 shows the GPIO port structure. The pins should be connected to DGND if not used.

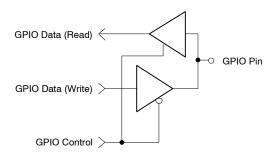


Figure 30. GPIO Port Pin

### Power-Down (PWDN)

When PWDN is pulled low, all on-chip circuitry is powered down. To exit power-down mode, take the PWDN pin high. Upon exiting from power-down mode, the internal oscillator and reference require time to wake up. During power-down, the external clock is recommended to be shut down to save power.

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### Reset (RESET)

There are two methods to reset the ADS130E08: pulling the RESET pin low, or sending the RESET opcode command. When using the RESET pin, take the pin low to force a reset. Make sure to follow the minimum pulse width timing specifications before taking the RESET pin back high. The RESET command takes effect on the eighth SCLK falling edge of the opcode command. On reset, 18 t<sub>CLK</sub> cycles are required to complete initialization of the configuration registers to the default states and start the conversion cycle. Note that an internal RESET is automatically issued to the digital filter whenever the CONFIG1 Register is set to a new value with a WREG command.

#### **START**

The START pin must be set high or the START command sent to begin conversions. When START is low or if the START command has not been sent, the device does not issue a DRDY signal (conversions are halted).

When using the START opcode to control conversions, hold the START pin low. In multiple device configurations the START pin is used to synchronize devices (see the Multiple Device Configuration subsection of the SPI *Interface* section for more details).

### **Settling Time**

The settling time (t<sub>SETTLE</sub>) is the time required for the converter to output fully-settled data when the START signal is pulled high. When START is pulled high, DRDY is also pulled high. The next DRDY falling edge indicates that data are ready. Figure 31 shows the timing diagram and shows the data rate settling time. The settling time depends on f<sub>CLK</sub> and is 1160 t<sub>CLK</sub>. Note that when START is held high and there is a step change in the input signal, 3 t<sub>DR</sub> is required for the filter to settle to the new value. Settled data are available on the fourth DRDY pulse.

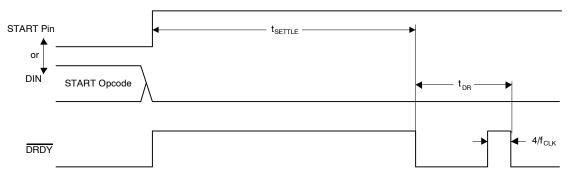
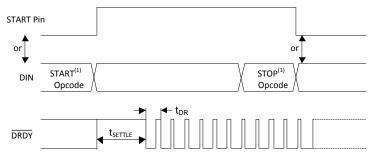


Figure 31. Settling Time



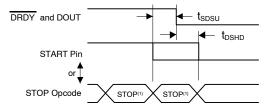
#### **Continuous Mode**

Conversions begin when the START pin is taken high or when the START opcode command is sent. As seen in Figure 32, the DRDY output goes high when conversions are started and then goes low when data are ready. Conversions continue indefinitely until the START pin is taken low or the STOP opcode command is transmitted. When the START pin is pulled low or the stop command is issued, the conversion in progress is allowed to complete. Figure 33 and Table 4 show the required DRDY timing to the START pin and the START and STOP opcode commands when controlling conversions in this mode. To keep the converter running continuously, the START pin can be permanently tied high.



(1) START and STOP opcode commands take effect on the seventh SCLK falling edge.

Figure 32. Continuous Conversion Mode



(1) START and STOP commands take effect on the seventh SCLK falling edge at the end of the opcode transmission.

Figure 33. START to DRDY Timing

Table 4. Timing Characteristics for Figure 33<sup>(1)</sup>

SYMBOL	DESCRIPTION	MIN	UNIT
t <sub>SDSU</sub>	START pin low or STOP opcode to DRDY setup time to halt further conversions	16	1/f <sub>CLK</sub>
t <sub>DSHD</sub>	START pin low or STOP opcode to complete current conversion	16	1/f <sub>CLK</sub>

(1) START and STOP commands take effect on the seventh SCLK falling edge at the end of the opcode transmission.

Product Folder Links: ADS130E08

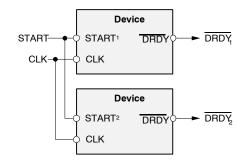


#### **MULTIPLE DEVICE CONFIGURATION**

The ADS130E08 is designed to provide configuration flexibility when <u>multiple</u> devices are used in a system. The serial interface typically needs four signals: DIN, DOUT, SCLK, and  $\overline{CS}$ . With one additional chip select signal per device, multiple devices can be connected together. The number of signals needed to interface n devices is 3 + n.

When using multiple devices, the devices can be synchronized with the START signal. The delay from START to the DRDY signal is fixed for a fixed data rate (see the *START* subsection of the *SPI Interface* section for more details on settling times). Figure 34 shows the behavior of two devices when synchronized with the START signal.

There are two ways to connect multiple devices with an optimal number of interface pins: cascade mode and daisy-chain mode.



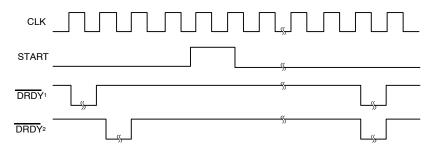


Figure 34. Synchronizing Multiple Converters

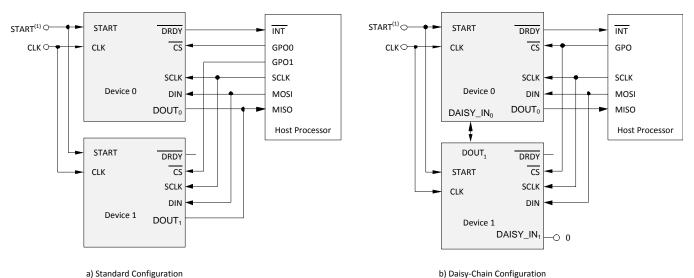
#### **Cascade Mode**

Figure 35a shows a configuration with two devices cascaded together. Both devices are an ADS130E08 device. Together, the devices create a system with 16 channels. DOUT, SCLK, and DIN are shared. Each device has its own chip select. When a device is not selected by the corresponding CS being driven to logic '1', the DOUT of this device is high-impedance. This structure allows the other device to take control of the DOUT bus. This configuration method is suitable for the majority of applications.

#### **Daisy-Chain Mode**

Daisy-chain mode is enabled by setting the DAISY\_IN bit in the CONFIG1: Configuration Register 1. Figure 35b shows the daisy-chain configuration. In this mode SCLK, DIN, and  $\overline{\text{CS}}$  are shared across multiple devices. The DOUT pin of one device is connected to the DAISY\_IN of the other device, thereby creating a chain. One extra SCLK must be issued between each data set. Also, when using daisy-chain mode, the multiple readback feature is not available. Short the DAISY\_IN pin to digital ground if not used. Figure 2 describes the required timing for the ADS130E08 shown in Figure 35. Data from the ADS130E08 appear first on DOUT, followed by a don't care bit, and finally by the status and data words from the second ADS130E08 device.

When all devices in the chain operate in the same register setting, DIN can be shared as well. This configuration reduces the SPI communication signals to four, regardless of the number of devices.



(1) To reduce pin count, set the START pin low and use the START serial command to synchronize and start conversions.

Figure 35. Multiple Device Configurations



Note that from Figure 2, the SCLK rising edge shifts data out of the ADS130E08 on DOUT. The SCLK rising edge is also used to latch data into the device DAISY\_IN pin down the chain. This architecture allows for a faster SCLK rate speed, but also makes the interface sensitive to board-level signal delays. The more devices in the chain, the more challenging it can become to adhere to setup and hold times. An SCLK star-pattern connection to all devices, minimizing DOUT length, and other printed circuit board (PCB) layout techniques helps. Placing delay circuits (such as buffers) between DOUT and DAISY\_IN also helps mitigate this challenge. One other option is to insert a *D* flip-flop between DOUT and DAISY\_IN clocked on an inverted SCLK. Also note that daisy-chain mode requires some software overhead to recombine data bits spread across byte boundaries. Figure 36 shows a timing diagram for daisy-chain mode.

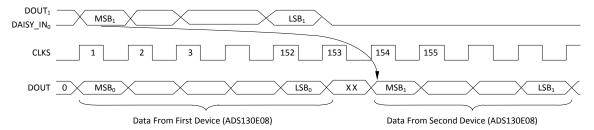


Figure 36. Daisy-Chain Timing

The maximum number of devices that can be daisy-chained depends on the data rate at which the device is operated at. The maximum number of devices can be approximately calculated with Equation 7.

$$N_{\text{DEVICES}} = \frac{f_{\text{SCLK}}}{152 \times f_{\text{DR}}} \tag{7}$$



#### SPI COMMAND DEFINITIONS

The ADS130E08 provides flexible configuration control. The opcode commands summarized in Table 5 control and configure device operation. The opcode commands are stand-alone, except for the register read and write operations that require a second command byte plus data.  $\overline{CS}$  can be taken high or held low between opcode commands but must stay low for the entire command operation (especially for multibyte commands). System opcode commands and the RDATA command are decoded by the ADS130E08 on the seventh SCLK falling edge. The register read and write opcodes are decoded on the eighth SCLK falling edge. Be sure to follow SPI timing requirements when pulling  $\overline{CS}$  high after issuing a command.

**Table 5. Command Definitions** 

COMMAND	DESCRIPTION	FIRST BYTE	SECOND BYTE				
System Comman	nds	T					
WAKEUP	Wake-up from standby mode	0000 0010 (02h)					
STANDBY	Enter standby mode	0000 0100 (04h)					
RESET	Reset the device	0000 0110 (06h)					
START	Start or restart (synchronize) conversions	0000 1000 (08h)	0000 1000 (08h)				
STOP	Stop conversion	0000 1010 (0Ah)					
Data Read Comm	nands						
RDATAC	Enable Read Data Continuous mode. This mode is the default mode at power-up. (1)	0001 0000 (10h)					
SDATAC	Stop Read Data Continuously mode	0001 0001 (11h)					
RDATA	Read data by command; supports multiple readback.	0001 0010 (12h)					
Register Read C	ommands						
RREG	Read <i>n nnnn</i> registers starting at address <i>r rrrr</i>	001 <i>r rrrr</i> (2xh) <sup>(2)</sup>	000 <i>n nnnn</i> <sup>(2)</sup>				
WREG	Write <i>n nnnn</i> registers starting at address <i>r rrrr</i>	010 <i>r rrrr</i> (4xh) <sup>(2)</sup>	000 <i>n nnnn</i> <sup>(2)</sup>				

<sup>(1)</sup> When in RDATAC mode, the RREG command is ignored.

#### **WAKEUP: Exit STANDBY Mode**

This opcode exits the low-power standby mode; see the *STANDBY: Enter STANDBY Mode* subsection of the *SPI Command Definitions* section. Time is required when exiting standby mode (see the Electrical Characteristics for details). **There are no SCLK rate restrictions for this command and it can be issued at any time.** The next command must be sent after a delay of 4 t<sub>CLK</sub> cycles.

#### STANDBY: Enter STANDBY Mode

This opcode command enters the low-power standby mode. All parts of the circuit are shut down except for the reference section. The standby mode power consumption is specified in the Electrical Characteristics. There are no SCLK rate restrictions for this command and it can be issued at any time. Do not send any other commands other than the wakeup command after the device enters standby mode.

#### **RESET**: Reset Registers to Default Values

This command resets the digital filter cycle and returns all register settings to the default values. See the *Reset (RESET)* subsection of the *SPI Interface* section for more details. There are no SCLK rate restrictions for this command and it can be issued at any time. 18 t<sub>CLK</sub> cycles are required to execute the RESET command. Avoid sending any commands during this time.

#### **START: Start Conversions**

This opcode starts data conversions. Tie the START pin low to control conversions by command. If conversions are in progress, this command has no effect. The STOP opcode command is used to stop conversions. If the START command is immediately followed by a STOP command, then a gap of 4  $t_{CLK}$  cycles must be between them. When the START opcode is sent to the device, keep the START pin low until the STOP command is issued. (See the *START* subsection of the *SPI Interface* section for more details.) There are no SCLK rate restrictions for this command and it can be issued at any time.

<sup>(2)</sup> *n nnnn* = number of registers to be read or written – 1. For example, to read or write three registers, set *n nnnn* = 0 (0010). *r rrrr* = starting register address for read and write opcodes.



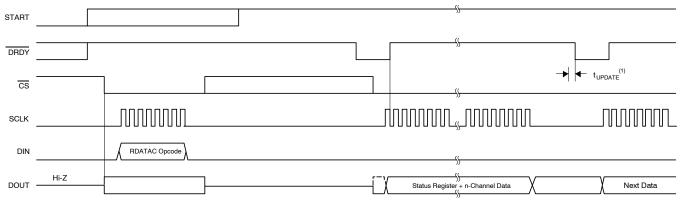
### **STOP: Stop Conversions**

This opcode stops conversions. Tie the START pin low to control conversions by command. When the STOP command is sent, the conversion in progress completes and further conversions are stopped. If conversions are already stopped, this command has no effect. There are no SCLK rate restrictions for this command and it can be issued at any time.

#### **RDATAC: Read Data Continuous**

This opcode enables conversion data output on each DRDY without the need to issue subsequent read data opcodes. This mode places the conversion data in the output register and may be shifted out directly. The read data continuous mode is the device default mode; the device defaults to this mode on power-up.

RDATAC mode is cancelled by the Stop Read Data Continuous command. If the device is in RDATAC mode, an SDATAC command must be issued before any other commands can be sent to the device. There is no SCLK rate restriction for this command. However, the subsequent data-retrieval SCLKs or the SDATAC opcode command should wait at least 4  $t_{CLK}$  cycles for the command to execute. RDATAC timing is shown in Figure 37. As Figure 37 shows, there is a *keep out* zone of 4  $t_{CLK}$  cycles around the  $\overline{D}RDY$  pulse where this command cannot be issued in. If no data are retrieved from the device, DOUT and  $\overline{D}RDY$  behave similarly in this mode. To retrieve data from the device after the RDATAC command is issued, make sure either the START pin is high or the START command is issued. Figure 37 shows the recommended way to use the RDATAC command. RDATAC is ideally-suited for applications such as data loggers or recorders where registers are set once and do not need to be reconfigured.



(1)  $t_{IJPDATE} = 4 / f_{CLK}$ . Do not read data during this time.

Figure 37. RDATAC Usage

#### **SDATAC: Stop Read Data Continuous**

This opcode cancels the Read Data Continuous mode. There is no SCLK rate restriction for this command, but the next command must wait 4  $t_{CLK}$  cycles to execute.

#### **RDATA: Read Data**

Issue this command after  $\overline{DRDY}$  goes low to read the conversion result (in Stop Read Data Continuous mode). There is no SCLK rate restriction for this command, and there is no wait time needed for subsequent commands or data-retrieval SCLKs. To retrieve data from the device after the RDATA command is issued, make sure either the START pin is high or the START command is issued. When reading data with the RDATA command, the read operation can overlap the next  $\overline{DRDY}$  occurrence without data corruption. Figure 38 shows the recommended way to use the RDATA command. RDATA is best suited for systems where register settings must be read or changed often between conversion cycles.

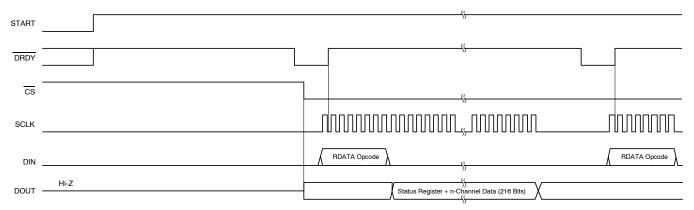


Figure 38. RDATA Usage

#### **Sending Multibyte Commands**

The ADS130E08 serial interface decodes commands in bytes and requires 4  $t_{CLK}$  cycles to decode and execute. Therefore, when sending multibyte commands, a 4- $t_{CLK}$  period must separate the end of one byte (or opcode) and the next.

Assuming CLK is 2.048 MHz, then  $t_{\text{SDECODE}}$  (4  $t_{\text{CLK}}$ ) is 1.96  $\mu$ s. When SCLK is 16 MHz, one byte can be transferred in 500 ns. This byte-transfer time does not meet the  $t_{\text{SDECODE}}$  specification; therefore, a delay must be inserted so the end of the second byte arrives 1.46  $\mu$ s later. If SCLK is 4 MHz, one byte is transferred in 2  $\mu$ s. Because this transfer time exceeds the  $t_{\text{SDECODE}}$  specification, the processor can send subsequent bytes without delay. In this later scenario, the serial port can be programmed to move from single-byte transfers per cycle to multiple bytes.

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#### RREG: Read From Register

This opcode reads register data. The Register Read command is a two-byte opcode followed by the register data output. The first byte contains the command opcode and register address. The second opcode byte specifies the number of registers to read – 1.

First opcode byte: 001*r rrrr*, where *r rrrr* is the starting register address.

Second opcode byte: 000*n nnnn*, where *n nnnn* is the number of registers to read – 1.

The 17th SCLK rising edge of the operation clocks out the MSB of the first register, as shown in Figure 39. When the device is in read data continuous mode, an SDATAC command must be issued before the RREG command can be issued. The RREG command can be issued at any time. However, because this command is a multibyte command, there are SCLK rate restrictions depending on how the SCLKs are issued. See the Serial Clock (SCLK) subsection of the SPI Interface section for more details. Note that  $\overline{\text{CS}}$  must be low for the entire command.

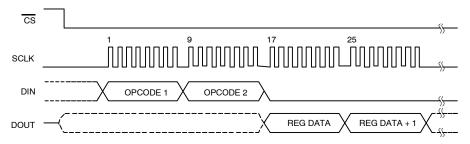


Figure 39. RREG Command Example: Read Two Registers Starting from Register 00h (ID Register) (OPCODE 1 = 0010 0000, OPCODE 2 = 0000 0001)

### **WREG: Write to Register**

This opcode writes register data. The Register Write command is a two-byte opcode followed by the register data input. The first byte contains the command opcode and the register address.

The second opcode byte specifies the number of registers to write -1.

First opcode byte: 010*r rrrr*, where *r rrrr* is the starting register address.

Second opcode byte:  $000n \, nnnn$ , where  $n \, nnnn$  is the number of registers to write -1.

After the opcode bytes, the register data follows (in MSB-first format), as shown in Figure 40. The WREG command can be issued at any time. However, because this command is a multibyte command, there are SCLK rate restrictions depending on how the SCLKs are issued. See the Serial Clock (SCLK) subsection of the SPI Interface section for more details. Note that CS must be low for the entire command.

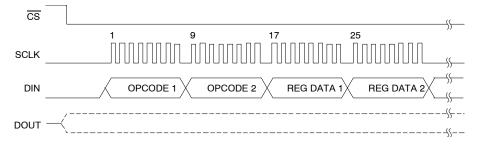


Figure 40. WREG Command Example: Write Two Registers Starting from 00h (ID Register) (OPCODE 1 = 0100 0000, OPCODE 2 = 0000 0001)

### **REGISTER MAP**

Table 6 describes the various ADS130E08 registers.

# Table 6. Register Assignments<sup>(1)</sup>

ADDRESS	REGISTER	RESET VALUE (Hex)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Device Settin	gs (Read-Only Regi	sters)								
00h	ID	52	REV_ID3	REV_ID2	REV_ID1	1	0	DEV_ID1	NU_CH2	NU_CH1
Global Setting	gs Across Channels	<b>i</b>								
01h	CONFIG1	01	0	0	CLK_EN	0	0	0	0	1
02h	CONFIG2	60	0	1	1	INT_TEST	0	TEST_AMP	TEST_FREQ1	TEST_FREQ0
03h	CONFIG3	40	PD_REFBUF	1	VREF_4V	0	OPAMP_REF	PD_OPAMP	0	0
04h	FAULT	00	COMP_TH2	COMP_TH1	COMP_TH0	0	0	0	0	0
Channel-Spec	ific Settings									
05h	CH1SET	10	PD1	GAIN12	GAIN11	GAIN10	0	MUX12	MUX11	MUX10
06h	CH2SET	10	PD2	GAIN22	GAIN21	GAIN20	0	MUX22	MUX21	MUX20
07h	CH3SET	10	PD3	GAIN32	GAIN31	GAIN30	0	MUX32	MUX31	MUX30
08h	CH4SET	10	PD4	GAIN42	GAIN41	GAIN40	0	MUX42	MUX41	MUX40
09h	CH5SET	10	PD5	GAIN52	GAIN51	GAIN50	0	MUX52	MUX51	MUX50
0Ah	CH6SET	10	PD6	GAIN62	GAIN61	GAIN60	0	MUX62	MUX61	MUX60
0Bh	CH7SET	10	PD7	GAIN72	GAIN71	GAIN70	0	MUX72	MUX71	MUX70
0Ch	CH8SET	10	PD8	GAIN82	GAIN81	GAIN80	0	MUX82	MUX81	MUX80
Fault Detect S	Status Registers (Re	ad-Only Reg	isters)							
12h	FAULT_STATP	00	IN8P_FAULT	IN7P_FAULT	IN6P_FAULT	IN5P_FAULT	IN4P_FAULT	IN3P_FAULT	IN2P_FAULT	IN1P_FAULT
13h	FAULT_STATN	00	IN8N_FAULT	IN7N_FAULT	IN6N_FAULT	IN5N_FAULT	IN4N_FAULT	IN3N_FAULT	IN2N_FAULT	IN1N_FAULT
GPIO and Oth	er Registers									
14h	GPIO	0F	GPIOD4	GPIOD3	GPIOD2	GPIOD1	GPIOC4	GPIOC3	GPIOC2	GPIOC1

<sup>(1)</sup> Registers 0Dh, 0Eh, 0Fh, 10h, and 11h must be written as all '0's.



### **User Register Description**

### ID: ID Control Register (Factory-Programmed, Read-Only)

Address = 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REV_ID3	REV_ID2	REV_ID1	1	0	DEV_ID1	NU_CH2	NU_CH1

This register is programmed during device manufacture to indicate device characteristics.

Bits[7:5] REV\_ID[3:1]: Device family identification (read-only)

These factory-programmed bits indicate the device version.

010 = ADS130E08 All others are reserved.

Bit 4 Must be set to '1'
Bit 3 Must be set to '0'

Bits[1:0] DEV\_ID1 and NU\_CH[2:1]: Device identification bits (read-only)

These factory-programmed bits indicate the device version.

010 = ADS130E08 All others are reserved.

### **CONFIG1: Configuration Register 1**

Address = 01h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	CLK_EN	0	0	0	0	1

This register is reserved for device manufacturing.

Bits[7:6] Must be set to '0'

Bit 5 CLK\_EN: CLK connection<sup>(1)</sup>

This bit determines if the internal oscillator signal is connected to the CLK pin when the CLKSEL pin is '1'.

0 = Oscillator clock output disabled (default)

1 = Oscillator clock output enabled

Bits[4:1] Must be set to '0'
Bit 0 Must be set to '1'

(1) Additional power is consumed when driving external devices.



### **CONFIG2: Configuration Register 2**

Address = 02h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	1	1	INT_TEST	0	TEST_AMP	TEST_FREQ1	TEST_FREQ0

This register configures test signal generation. See the *Input Multiplexer* section for more details.

Bit 7 Must be set to '0'

Bits[6:5] Must be set to '1'

Bit 4 INT\_TEST: Test source

This bit determines the test signal source.

Test signals are driven externally (default)
 Test signals are generated internally

Bit 3 Must be set to '0'

Bit 2 TEST\_AMP: Test signal amplitude

This bit determines the Calibration signal amplitude.

 $0 = 1 \times -(VREFP - VREFN) / 2.4 \text{ mV (default)}$ 

 $1 = 2 \times -(VREFP - VREFN) / 2.4 \text{ mV}$ 

Bits[1:0] TEST\_FREQ[1:0]: Test signal frequency

These bits determine the calibration signal frequency.

00 = Pulsed at  $f_{CLK} / 2^{21}$  (default)

01 = Pulsed at  $f_{CLK}$  /  $2^{20}$ 

10 = Not used

11 = At dc

#### **CONFIG3: Configuration Register 3**

Address = 03h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PD_REFBUF	1	VREF_4V	0	OPAMP_REF	PD_OPAMP	0	0

This register configures multireference operation.

Bit 7 PD REFBUF: Power-down reference buffer

This bit determines the power-down reference buffer state.

0 = Power-down internal reference buffer (default)

1 = Enable internal reference buffer

Bit 6 Must be set to '1'

Default is '1' at power-up.

Bit 5 VREF\_4V: Reference voltage

This bit determines the reference voltage, VREFP.

0 = VREFP is set to 2.4 V (default)

1 = VREFP is set to 4 V (only use with a 5-V analog supply)

Bit 4 Must be set to '0'

Bit 3 OPAMP\_REF: Op amp reference

This bit determines whether the op amp noninverting input connects to the OPAMPP pin or to the internally-derived 1/2 supply (AVDD + AVSS) / 2.

0 = Noninverting input connected to the OPAMPP pin (default) 1 = Noninverting input connected to (AVDD + AVSS) / 2

Bit 2 PD\_OPAMP: Power-down op amp

This bit determines the power-down reference buffer state.

0 = Power-down op amp (default)

1 = Enable op amp

Bits[1:0] Must be set to '0'



### FAULT: Fault Detect Control Register

Address = 04h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
COMP_TH2	COMP_TH1	COMP_TH0	0	0	0	0	0

This register configures the fault detection operation.

#### Bits[7:5] COMP\_TH[2:0]: Fault detect comparator threshold

These bits determine the fault detect comparator threshold level setting. See the Fault Detection section for a detailed description.

#### Comparator positive-side threshold

000 = 95% (default)

001 = 92.5%

010 = 90%

011 = 87.5%

100 = 85%

101 = 80%

110 = 75%

111 = 70%

### Comparator negative-side threshold

000 = 5% (default)

001 = 7.5%

010 = 10%

011 = 12.5%

100 = 15%

101 = 20%

110 = 25%

111 = 30%

#### Bits[4:0] Must be set to '0'



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#### CHnSET: Individual Channel Settings (n = 1 to 8)

Address = 05h to 0Ch

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PDn	GAINn2	GAINn1	GAINn0	0	MUXn2	MUXn1	MUXn0

The CH[8:1]SET Control Register configures the power mode, PGA gain, and multiplexer setting channels. See the *Input Multiplexer* section for details. CH[8:2]SET are similar to CH1SET, corresponding to the respective channels (refer to Table 6).

#### Bit 7 PDn: Power-down (n = individual channel number)

This bit determines the channel power mode for the corresponding channel.

0 = Normal operation (default)

1 = Channel power-down

#### Bits[6:4] GAINn[2:0]: PGA gain (n = individual channel number)

These bits determine the PGA gain setting.

000 = Do not use

001 = x1

010 = x2

011 = Do not use

100 = Do not use

101 = x8

110 = Do not use

111 = Do not use

#### Bit 3 Must be set to '0'

#### Bits[2:0] MUXn[2:0]: Channel input (n = individual channel number)

These bits determine the channel input selection.

000 = Normal input (default)

001 = Input shorted (for offset or noise measurements)

010 = Do not use

011 = MVDD for supply measurement

100 = Temperature sensor

101 = Test signal

110 = Do not use

111 = Do not use





#### FAULT\_STATP: Fault Detect Positive Input Status

Address = 12h

BIT 7	BIT 6	BIT 5 BIT 4		BIT 3	BIT 2	BIT 1	BIT 0
IN8P_FAULT	IN7P_FAULT	IN6P_FAULT	IN5P_FAULT	IN4P_FAULT	IN3P_FAULT	IN2P_FAULT	IN1P_FAULT

This register stores the status of whether a fault condition is present on the positive electrode of each channel. See the *Fault Detection* section for details.

#### Bits[7:0] INnP\_FAULT: Input fault status (n = individual channel number)

0 = No fault present (default)

1 = Fault present

#### FAULT\_STATN: Fault Detect Negative Input Status

Address = 13h

BIT 7	BIT 6	BIT 5 BIT 4		BIT 3	BIT 2	BIT 1	BIT 0
IN8N_FAULT	IN7N_FAULT	IN6N_FAULT	IN5N_FAULT	IN4N_FAULT	IN3N_FAULT	IN2N_FAULT	IN1N_FAULT

This register stores the status of whether a fault condition is present on the negative electrode of each channel. See the *Fault Detection* section for details.

#### Bits[7:0] INnN\_FAULT: Input fault status (n = individual channel number)

0 = No fault present (default)

1 = Fault present

#### GPIO: General-Purpose IO Register

Address = 14h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
GPIOD4	GPIOD3	GPIOD2	GPIOD1	GPIOC4	GPIOC3	GPIOC2	GPIOC1

This register controls the action of the three GPIO pins.

#### Bits[7:4] GPIOD[4:1]: GPIO data

These bits are used to read and write data to the GPIO ports.

When reading the register, the data returned correspond to the state of the GPIO external pins, whether they are programmed as inputs or outputs. As outputs, a write to the GPIOD sets the output value. As inputs, a write to the GPIOD has no effect.

#### Bits[3:0] GPIOC[4:1]: GPIO control (corresponding to GPIOD)

These bits determine if the corresponding GPIOD pin is an input or output.

0 = Output

1 = Input (default)

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#### POWER-MONITORING SPECIFIC APPLICATIONS

All ADS130E08 channels are independently configurable, allowing any channel to be selected for voltage or current monitoring. Also, the simultaneously sampling capability of the device allows both current and voltage to be monitored at the same time. The full-scale differential input voltage of each channel is determined by the PGA gain setting (see the CHnSET: Individual Channel Settings section) for the respective channel and V<sub>RFF</sub> (see the CONFIG3: Configuration Register 3 section). Table 7 summarizes the full-scale differential input voltage range for an internal V<sub>RFF</sub>.

Table 7. Full-Scale Billerential input (1 SBI) Voltage Summary											
V <sub>REF</sub>	PGA GAIN	FULL-SCALE DIFFERENTIAL INPUT VOLTAGE (V <sub>PP</sub> )	RMS VOLTAGE [= FSDI / (2√2)] (V <sub>RMS</sub> )								
	1	4.8	1.698								
2.4 V	2	2.4	0.849								
	8	0.6	0.212								
	1	8.0	2.828								
4.0 V	2	4.0	1.414								
	8	1	0.354								

Table 7 Full-Scale Differential Input (FSDI) Voltage Summary

#### **CURRENT SENSING**

Figure 41 shows a simplified diagram of typical configurations used for current sensing with a Rogowski coil, current transformer (CT), or an air coil that outputs a current or voltage. In the case of current-output transformers, the burden resistors (R1) are used for current-to-voltage conversion. The burden resistor output is connected to the ADS130E08 INP and INN inputs through an antialiasing RC filter for current sensing. In the case of voltage-output transformers (such as certain types of Rogowski coils), the transformer output terminals are directly connected to the ADS130E08 INP and INN inputs through an antialiasing RC filter for current sensing. The common-mode bias voltage (AVDD + AVSS) / 2, can be obtained from the ADS130E08 by either configuring the internal op amp in a unity-gain configuration using the R<sub>F</sub> resistor and setting bit 3 of CONFIG3: Configuration Register 3, or it can be generated externally with a simple resistor divider network between the positive and negative supplies.

The resistor R1 value for the current-output transformer, the output voltage (V) for the voltage-output transformer, and the turns ratio of the transformer should be carefully selected so as not to exceed the ADS130E08 FSDI range (see Table 7). Furthermore, these values should not saturate the transformer over the full operating dynamic range of the energy meter. Figure 41a shows differential input current sensing and Figure 41b shows single-ended input sensing.

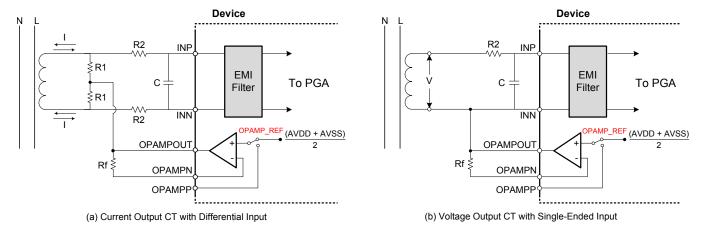


Figure 41. Simplified Current-Sensing Connections

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#### **VOLTAGE SENSING**

Figure 42 shows a simplified diagram of commonly-used differential and single-ended methods of voltage sensing. A resistor divider network is used to step down the line voltage within the acceptable input range of the ADS130E08 and then directly connect to the inputs (INP and INN) through an antialiasing RC filter formed by resistor R3 and capacitor C. The common-mode bias voltage (AVDD + AVSS) / 2, can be obtained from the ADS130E08 by either configuring the internal op amp in a unity-gain configuration using the R<sub>F</sub> resistor and setting bit 3 of CONFIG3: Configuration Register 3, or it can be generated externally by using a simple resistor divider network between the positive and negative supplies.

In either case presented in Figure 42 (Figure 42a for a differential input and Figure 42b for a single-ended input), the line voltage is divided down by a factor of [R2 / (R1 + R2)]. R1 and R2 values must be carefully chosen so that the voltage across the ADS130E08 inputs (INP and INN) does not exceed the ADS130E08 FSDI range (see Table 7) over the full operating dynamic range of the energy meter.

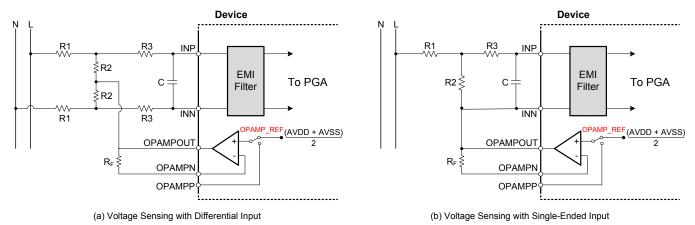


Figure 42. Simplified Voltage Sensing Connections

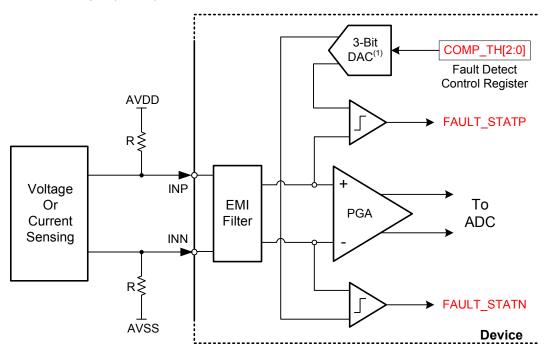
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#### **FAULT DETECTION**

The ADS130E08 has integrated comparators that can be used in conjunction with the external pull-up or pull-down resistors (R) to detect various fault conditions. The basic principle is to compare the input voltage with the voltage set by the 3-bit DAC fault comparator, as shown in Figure 43. The comparator trigger threshold level is set by the COMP\_TH[2:0] bits in the FAULT register. Assuming that the ADS130E08 is powered from a  $\pm 2.5$ -V supply and COMP\_TH[2:0] = 000 (95% and 5%), the high-side trigger threshold is set at  $\pm 2.25$  V [equal to AVSS + (AVDD + AVSS) × 95%] and the low-side threshold is set at  $\pm 2.25$  V [equal to AVSS + (AVDD + AVSS) × 5%]. The threshold calculation formula applies to unipolar as well as bipolar supplies.

A fault condition, such as an input signal going out of a predetermined range, can be detected by setting the appropriate threshold level using the COMP\_TH[2:0] bits. An open-circuit fault at the INP or INN pin can be detected by using the external pull-up and pull-down resistors, which rails the corresponding input when the input circuit breaks, causing the fault comparators to trip. To pinpoint which of the inputs is out of range, the status of the FAULT\_STATP and FAULT\_STATN registers can be read, which is available as part of the output data stream; see the *Data Output (DOUT)* subsection of the *SPI Interface* section.



(1) The configurable 3-bit DAC is common to all channels.

Figure 43. Fault Detect Comparators

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#### QUICK-START GUIDE

#### **PCB LAYOUT**

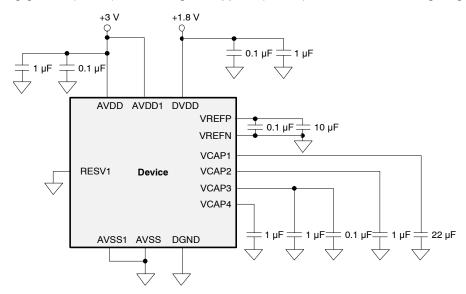
#### **Power Supplies and Grounding**

The ADS130E08 has three supplies: AVDD, AVDD1, and DVDD. Both AVDD and AVDD1 should be as quiet as possible. AVDD1 provides the supply to the charge pump block and has transients at f<sub>CLK</sub>. Therefore, AVDD1 and AVSS1 are recommended to be star-connected to AVDD and AVSS. It is important to eliminate noise from AVDD and AVDD1 that is non-synchronous with the ADS130E08 operation. Each ADS130E08 supply should be bypassed with 10-µF and a 0.1-µF solid ceramic capacitors. It is recommended that placement of the digital circuits (such as DSPs, microcontrollers, and FPGAs) in the system be done such that the return currents on those devices do not cross the ADS130E08 analog return path. The ADS130E08 can be powered from unipolar or bipolar supplies.

The capacitors used for decoupling can be surface-mount, low-cost, low-profile multilayer ceramic capacitors. In most cases the VCAP1 capacitor can also be a multilayer ceramic. However, in systems where the board is subjected to high- or low-frequency vibration, it is recommend that a non-ferroelectric capacitor such as a tantalum or class 1 capacitor (COG or NPO for example) be installed. EIA class 2 and class 3 dielectrics (such as X7R, X5R, and X8R) are ferroelectric. The piezoelectric property of these capacitors can appear as electrical noise coming from the capacitor. When using the internal reference, noise on the VCAP1 node results in performance degradation.

#### Connecting the Device to Unipolar (+3 V or +1.8 V) Supplies

Figure 44 shows the ADS130E08 connected to a unipolar supply. In this example, the analog supply (AVDD) is referenced to analog ground (AVSS) and the digital supplies (DVDD) are referenced to digital ground (DGND).



NOTE: Place the capacitors for supply, reference, and VCAP1 to VCAP4 as close to the package as possible.

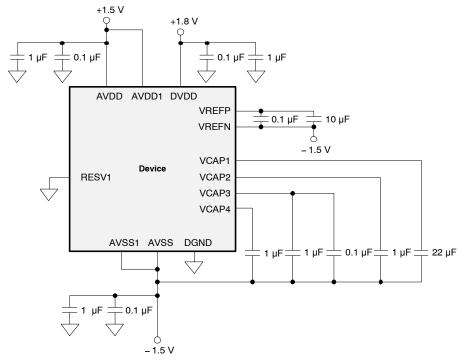
Figure 44. Single-Supply Operation

42 Sub



#### Connecting the Device to Bipolar (±1.5 V or 1.8 V) Supplies

Figure 45 illustrates the ADS130E08 connected to a bipolar supply. In this example, the analog supplies connect to the device analog supply (AVDD). This supply is referenced to the device analog return (AVSS), and the digital supply (DVDD) is referenced to the device digital ground return (DGND).



NOTE: Place the capacitors for supply, reference, and VCAP1 to VCAP4 as close to the package as possible.

Figure 45. Bipolar Supply Operation

#### **Shielding Analog Signal Paths**

As with any precision circuit, careful PCB layout ensures the best performance. It is essential to make short, direct interconnections and avoid stray wiring capacitance—particularly at the analog input pins and AVSS. These analog input pins are high-impedance and extremely sensitive to extraneous noise. The AVSS pin should be treated as a sensitive analog signal and connected directly to the supply ground with proper shielding. Leakage currents between the PCB traces can exceed the ADS130E08 input bias current if shielding is not implemented. Digital signals should be kept as far as possible from the analog input signals on the PCB.

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#### **POWER-UP SEQUENCING**

Before device power-up, all digital and analog inputs must be low. At the time of power-up, all of these signals should remain low until the power supplies have stabilized, as shown in Figure 46. At this time, begin supplying the master clock signal to the CLK pin. Wait for time t<sub>POR</sub>, then transmit a RESET pulse. After releasing RESET, the configuration register must be programmed (see the *CONFIG1: Configuration Register 1* subsection of the *Register Map* section for details). The power-up sequence timing is shown in Table 8.

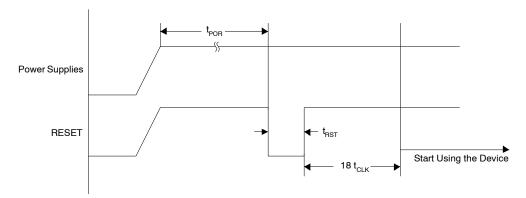


Figure 46. Power-Up Timing Diagram

**Table 8. Power-Up Sequence Timing** 

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t <sub>POR</sub>	Wait after power-up until reset	2 <sup>16</sup>			t <sub>CLK</sub>
t <sub>RST</sub>	Reset low width	2			t <sub>CLK</sub>

#### SETTING THE DEVICE FOR BASIC DATA CAPTURE

This section outlines the procedure to configure the device in a basic state and capture data. This procedure is intended to put the device in a data sheet condition to check if the device is working properly in the user system. This procedure is recommended to be followed initially to get familiar with the device settings. When this procedure is verified, the device can be configured as needed. For details on the timings for commands refer to the appropriate sections in the data sheet. The flow chart of Figure 47 details the initial configuration and setup of the ADS130E08.

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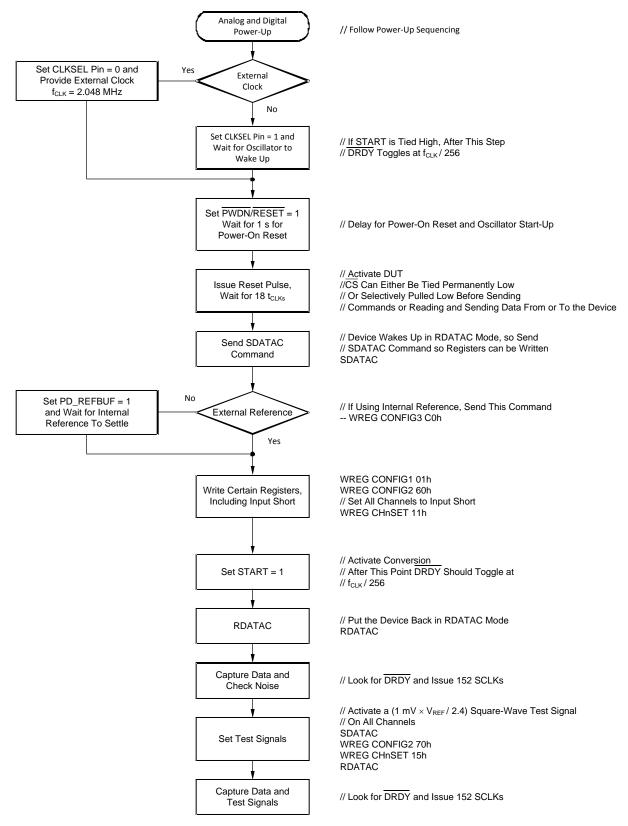


Figure 47. Initial Flow at Power-Up



# **REVISION HISTORY**

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

CI	nanges from Original (July 2012) to Revision A	Page
•	Changed pin out drawing	7
•	Added CLKSEL row to Pin Assignments table	<mark>7</mark>
•	Deleted terminal 52 from DGND row in Pin Assignments table	<mark>7</mark>
•	Added cross-reference to Figure 29 in second paragraph of Data Ready section	23
•	Changed description of GPIO pin connections in GPIO section	23
•	Deleted last sentence in description paragraph in FAULT_STATP and FAULT_STATN sections	38
•	Changed Bits[1:0] to Bits[3:0] in GPIOC description in the GPIO: General-Purpose IO Register section	38

46

www.ti.com 11-Nov-2025

#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
ADS130E08IPAG	Active	Production	TQFP (PAG)   64	160   JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	ADS130E08
ADS130E08IPAG.A	Active	Production	TQFP (PAG)   64	160   JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	ADS130E08
ADS130E08IPAGR	Active	Production	TQFP (PAG)   64	1500   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	ADS130E08
ADS130E08IPAGR.A	Active	Production	TQFP (PAG)   64	1500   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	ADS130E08

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(3)</sup> RoHS values: Yes, No. RoHS Exempt, See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

# **PACKAGE MATERIALS INFORMATION**

www.ti.com 23-May-2025

### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS130E08IPAGR	TQFP	PAG	64	1500	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2

www.ti.com 23-May-2025



#### \*All dimensions are nominal

	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
ı	ADS130E08IPAGR	TQFP	PAG	64	1500	350.0	350.0	43.0	



www.ti.com 23-May-2025

#### **TRAY**



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

#### \*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	Κ0 (μm)	P1 (mm)	CL (mm)	CW (mm)
ADS130E08IPAG	PAG	TQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
ADS130E08IPAG.A	PAG	TQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13

### PAG (S-PQFP-G64)

#### PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-026

# PAG (S-PQFP-G64)

# PLASTIC QUAD FLATPACK



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



# PAG (S-PQFP-G64)

# PLASTIC QUAD FLATPACK



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