











**ADS1018** 



SBAS526D - NOVEMBER 2012 - REVISED SEPTEMBER 2019

# ADS1018 Ultrasmall, Low-Power, SPI™-Compatible, 12-Bit, Analog-to-Digital Converter With Internal Reference and Temperature Sensor

## **Features**

Ultrasmall X2QFN Package 2 mm × 1.5 mm × 0.4 mm

12-Bit Noise-Free Resolution

Wide Supply Range: 2 V to 5.5 V

Low Current Consumption:

Continuous Mode: Only 150 μA

Single-Shot Mode: Automatic Power-Down

Programmable Data Rate: 128 SPS to 3300 SPS

Single-Cycle Settling

Internal Low-Drift Voltage Reference

Internal Temperature Sensor: 2°C (max) Error

Internal Oscillator

Internal PGA

Four Single-Ended or Two Differential Inputs

Specified Temperature: -40°C to +125°C

## **Applications**

- Temperature Measurement:
  - Thermocouple Measurement
  - Cold-Junction Compensation
  - Thermistor Measurement
- Portable Instrumentation
- Factory Automation and Process Controls

## 3 Description

The ADS1018 is a precision, low-power, 12-bit, noisefree, analog-to-digital converter (ADC) that provides all features necessary to measure the most common sensor signals in an ultrasmall, leadless, X2QFN-10 or VSSOP-10 package. The ADS1018 integrates a programmable gain amplifier (PGA), reference, oscillator and high-accuracy temperature sensor. These features, along with a wide powersupply range from 2 V to 5.5 V, make the ADS1018 ideally suited for power- and space-constrained, sensor-measurement applications.

The ADS1018 performs conversions at data rates up to 3300 samples per second (SPS). The PGA offers input ranges from ±256 mV to ±6.144 V, allowing both large and small signals to be measured with high resolution. An input multiplexer (mux) allows measurement of two differential or four single-ended inputs. The high-accuracy temperature sensor is used for system-level temperature monitoring, or coldjunction compensation for thermocouples.

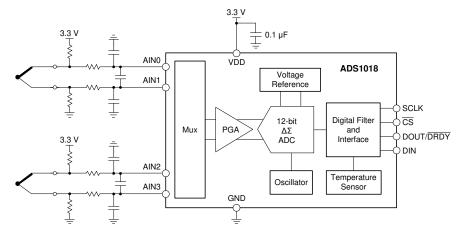
The ADS1018 operates either in continuousconversion mode, or in a single-shot mode that automatically powers down after a conversion. Single-shot mode significantly reduces current consumption during idle periods. Data are transferred through a serial peripheral interface (SPI™).

#### Device Information<sup>(1)</sup>

PART NUMBER	NUMBER PACKAGE BODY SI	
ADS1018	X2QFN (10)	1.50 mm × 2.00 mm
	VSSOP (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

#### **K-Type Thermocouple Measurement** Using Integrated Temperature Sensor for Cold-Junction Compensation





## **Table of Contents**

1	Features 1		8.5 Programming	. 16
2	Applications 1		8.6 Register Maps	. 19
3	Description 1	9	Application and Implementation	21
4	Revision History2		9.1 Application Information	. 21
5	Device Comparison Table 4		9.2 Typical Application	. 26
6	Pin Configuration and Functions4	10	Power Supply Recommendations	29
7	Specifications		10.1 Power-Supply Sequencing	. 29
•	7.1 Absolute Maximum Ratings		10.2 Power-Supply Decoupling	. 29
	7.2 ESD Ratings	11	Layout	30
	7.3 Recommended Operating Conditions		11.1 Layout Guidelines	. 30
	7.4 Thermal Information		11.2 Layout Example	. 31
	7.5 Electrical Characteristics	12	Device and Documentation Support	32
	7.6 Timing Requirements: Serial Interface		12.1 Documentation Support	. 32
	7.7 Switching Characteristics: Serial Interface		12.2 Receiving Notification of Documentation Updates	3 <mark>2</mark>
	7.8 Typical Characteristics		12.3 Community Resources	. 32
8	Detailed Description 10		12.4 Trademarks	. 32
•	8.1 Overview		12.5 Electrostatic Discharge Caution	. 32
	8.2 Functional Block Diagram		12.6 Glossary	. 32
	8.3 Feature Description	13	Mechanical, Packaging, and Orderable	
	8.4 Device Functional Modes		Information	32
	20. 20. Strong Modern M			

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

CI	hanges from Revision C (November 2015) to Revision D	Page
•	Changed maximum VDD voltage from 5.5 V to 7 V in the Absolute Maximum Ratings table	5
•	Changed bit description of Config Register bit 0	20

## Changes from Revision B (October 2013) to Revision C

Page

•	Added ESD Ratings table, Feature Description section, Noise Performance section, Device Functional Modes section, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section	1
•	Changed title, Description section, Features section, and block diagram on front page	1
•	Changed title from Product Family to Device Comparison Table and deleted Package Designator column	4
•	Updated descriptions and changed name of I/O column in Pin Configurations and Functions table	4
•	Changed digital input voltage range and added minimum specification for T <sub>J</sub> in <i>Absolute Maximum Ratings</i> table	5
•	Added Differential input impedance specification in Electrical Characteristics	6
•	Changed Condition statement in Timing Requirements: Serial Interface	8
•	Moved t <sub>CSDOD</sub> , t <sub>DOPD</sub> , and t <sub>CSDOZ</sub> parameters from <i>Timing Requirements</i> to <i>Switching Characteristics</i>	8
•	Moved t <sub>CSDOD</sub> and t <sub>CSDOZ</sub> values from MIN column to MAX column.	8
•	Deleted Figure 7, Noise Plot	
•	Updated Overview section and deleted "Gain = 2/3, 1, 2, 4, 8, or 16" from Functional Block Diagram	
•	Updated Analog Inputs section	12
•	Updated Full-Scale Range (FSR) and LSB Size section	
•	Updated Reset and Power Up section	
•	Updated 32-Bit Data Transmission Cycle section	
•	Updated Register Maps section	
•	Updated Application Information section	

Submit Documentation Feedback

Copyright © 2012–2019, Texas Instruments Incorporated



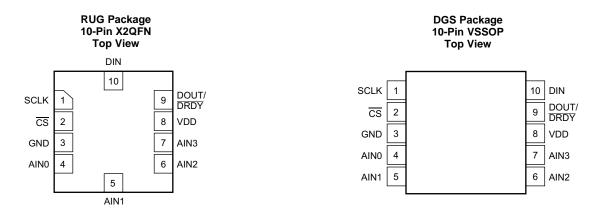
Changes from Original (November 2012) to Revision A	Page
Changed NOP bit description in Table 5: changed bits[2:0] to bits [2:1] and changed Nop bits [2:1] and changed Nop bits [2:1] and changed Nop bits [2:0] to bits [2:1] and changed Nop bits [2:0] to bits [2:1] and changed Nop bits [2:0] to bits [2:0] to bits [2:0] and changed Nop bits [2:0] to bits [2:0] to bits [2:0] and changed Nop bits [2:0] to bits [2:0] to bits [2:0] and changed Nop bits [2:0] to bits [2:0] to bits [2:0] and changed Nop	OP to NOP[1:0]
Changed bit 1 to NOP0 in Table 5	19
Deleted device graphic	1
Changes from Revision A (December 2012) to Revision B	Page
Deleted Thermocouple Measurement With Cold Junction Temperature section, and m     Application section	•
Updated Figure 21	24
www.ti.com SBAS526D – NO	VEMBER 2012-REVISED SEPTEMBER 2019



## 5 Device Comparison Table

DEVICE	RESOLUTION (Bits)	MAXIMUM SAMPLE RATE (SPS)	INPUT CHANNELS Differential (Single-Ended)	PGA	INTERFACE	SPECIAL FEATURES	
ADS1118	16	860	2 (4)	Yes	SPI	Temperature sensor	
ADS1018	12	3300	2 (4)	Yes	SPI	Temperature sensor	
ADS1115	16	860	2 (4)	Yes	I <sup>2</sup> C	Comparator	
ADS1114	16	860	1 (1)	Yes	I <sup>2</sup> C	Comparator	
ADS1113	16	860	1 (1)	No	I <sup>2</sup> C	None	
ADS1015	12	3300	2 (4)	Yes	I <sup>2</sup> C	Comparator	
ADS1014	12	3300	1 (1)	Yes	I <sup>2</sup> C	Comparator	
ADS1013	12	3300	1 (1)	No	I <sup>2</sup> C	None	

# **6 Pin Configuration and Functions**



### **Pin Functions**

	PIN	TYPE	DESCRIPTION	
NO.	NAME	ITPE	DESCRIPTION	
1	SCLK	Digital input	Serial clock input	
2	CS	Digital input	Chip select; active low. Connect to GND if not used.	
3	GND	Supply	round	
4	AIN0	Analog input	nalog input 0. Leave unconnected or tie to VDD if not used.	
5	AIN1	Analog input	nalog input 1. Leave unconnected or tie to VDD if not used.	
6	AIN2	Analog input	nalog input 2. Leave unconnected or tie to VDD if not used.	
7	AIN3	Analog input	Analog input 3. Leave unconnected or tie to VDD if not used.	
8	VDD	Supply	ower supply. Connect a 0.1-µF power-supply decoupling capacitor to GND.	
9	DOUT/DRDY	Digital output	erial data output combined with data ready; active low	
10	DIN	Digital input	Serial data input	



## 7 Specifications

#### 7.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Power-supply voltage	VDD to GND	-0.3	7	V
Analog input voltage	AINO, AIN1, AIN2, AIN3	GND - 0.3	VDD + 0.3	V
Digital input voltage	DIN, DOUT/DRDY, SCLK, CS	GND - 0.3	VDD + 0.3	V
Input current, continuous	Any pin except power supply pins	-10	10	mA
Tomporatura	Junction, T <sub>J</sub>	-40	150	°C
Temperature	Storage, T <sub>stg</sub>	-60	150	10

<sup>(1)</sup> Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 7.2 ESD Ratings

			VALUE	UNIT
,, Electrostatic	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±4000	.,	
V <sub>(ESD)</sub>	discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
SUPPLY					
Power supply	VDD to GND	2		5.5	V
INPUTS <sup>(1)</sup>					
Full-scale input voltage (2)	$V_{IN} = V_{(AINP)} - V_{(AINN)}$	S	ee Table 1		
Absolute input voltage		GND		VDD	V
INPUTS		•		•	
Input voltage		GND		VDD	V
ATURE		·			
Operating ambient temperature	9	-40		125	°C
	9	-40			125
SI F A III A	UPPLY Power supply NPUTS <sup>(1)</sup> Full-scale input voltage <sup>(2)</sup> Absolute input voltage NPUTS Input voltage TURE	Power supply VDD to GND  NPUTS <sup>(1)</sup> Full-scale input voltage <sup>(2)</sup> V <sub>IN</sub> = V <sub>(AINP)</sub> – V <sub>(AINN)</sub> Absolute input voltage  NPUTS  Input voltage  TURE	MIN  UPPLY  Power supply VDD to GND 2  NPUTS <sup>(1)</sup> Full-scale input voltage <sup>(2)</sup> V <sub>IN</sub> = V <sub>(AINP)</sub> - V <sub>(AINN)</sub> Solute input voltage GND  NPUTS  Input voltage GND  TURE	MIN NOM  UPPLY  Power supply VDD to GND 2  NPUTS(1)  Full-scale input voltage(2) V <sub>IN</sub> = V <sub>(AINP)</sub> - V <sub>(AINN)</sub> See Table 1  Absolute input voltage GND  NPUTS  Input voltage GND  TURE	MIN   NOM   MAX

- (1) AINP and AINN denote the selected positive and negative inputs. AINx denotes one of the four available analog inputs.
- 2) This parameter expresses the full-scale range of the ADC scaling. No more than VDD + 0.3 V or 5.5 V (whichever is smaller) must be applied to this device.

#### 7.4 Thermal Information

		ADS	ADS1018		
THERMAL METRIC <sup>(1)</sup>		DGS (VSSOP)	RUG (X2QFN)	UNIT	
		10 PINS	10 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	186.8	245.2	°C/W	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.5	69.3	°C/W	
$R_{\theta JB}$	Junction-to-board thermal resistance	108.4	172	°C/W	
ΨЈТ	Junction-to-top characterization parameter	2.7	8.2	°C/W	
ΨЈВ	Junction-to-board characterization parameter	106.5	170.8	°C/W	
R <sub>0</sub> JC(bot)	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W	

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.



## 7.5 Electrical Characteristics

Maximum and minimum specifications apply from  $T_A = -40^{\circ}\text{C}$  to +125°C. Typical specifications are at  $T_A = 25^{\circ}\text{C}$ . All specifications are at VDD = 3.3 V and FSR = ±2.048 V (unless otherwise noted).

	PARAMETER	TEST CONDITIONS	MIN TYP	MAX	UNIT
ANAL	OG INPUTS			•	
		FSR = ±6.144 V <sup>(1)</sup>	8		
		FSR = ±4.096 V <sup>(1)</sup> , FSR = ±2.048 V	6		MO
	Common-mode input impedance	FSR = ±1.024 V	3		МΩ
		FSR = ±0.512 V, FSR = ±0.256 V	100		
		FSR = ±6.144 V <sup>(1)</sup>	22		
		FSR = ±4.096 V <sup>(1)</sup>	15		МΩ
	Differential input impedance	FSR = ±2.048 V	4.9		IVILI
		FSR = ±1.024 V	2.4		
		FSR = ±0.512 V, FSR = ±0.256 V	710		kΩ
SYST	EM PERFORMANCE				
	Resolution (no missing codes)		12		Bits
DR	Data rate		128, 250, 490, 920, 1600, 2	2400, 3300	SPS
	Data rate variation	All data rates	-10%	10%	
INL	Integral nonlinearity	DR = 128 SPS, FSR = ±2.048 V <sup>(2)</sup>		0.5	LSB
	Offset error	FSR = ±2.048 V, differential inputs	0	±0.5	LCD
	Oliset error	FSR = ±2.048 V, single-ended inputs	±0.25		LSB
	Offset drift	FSR = ±2.048 V	0.002		LSB/°C
	Offset channel match	Match between any two inputs	0.25		LSB
	Gain error <sup>(3)</sup>	FSR = ±2.048 V, T <sub>A</sub> = 25°C	0.05%	0.25%	
		FSR = ±0.256 V	7		
	Gain drift (3)(4)	FSR = ±2.048 V	5	40	ppm/°C
		FSR = ±6.144 V <sup>(1)</sup>	5		
	Gain match <sup>(3)</sup>	Match between any two gains	0.02%	0.1%	
	Gain channel match	Match between any two inputs	0.05%	0.1%	
TEMP	PERATURE SENSOR			·	
	Temperature range		-40	125	°C
	Temperature resolution		0.125		°C/LSB
		$T_A = 0$ °C to 70°C	0.25	±1	°C
	Accuracy	$T_A = -40^{\circ}C \text{ to } +125^{\circ}C$	0.5	±2	
		versus supply	0.125	±1	°C/V

<sup>(1)</sup> This parameter expresses the full-scale range of the ADC scaling. No more than VDD + 0.3 V or 5.5 V (whichever is smaller) must be applied to this device.

Submit Documentation Feedback

Copyright © 2012–2019, Texas Instruments Incorporated

<sup>(2)</sup> Best-fit INL; covers 99% of full-scale.

<sup>(3)</sup> Includes all errors from onboard PGA and voltage reference.

<sup>(4)</sup> Maximum value specified by characterization.



## **Electrical Characteristics (continued)**

Maximum and minimum specifications apply from  $T_A = -40^{\circ}\text{C}$  to +125°C. Typical specifications are at  $T_A = 25^{\circ}\text{C}$ . All specifications are at VDD = 3.3 V and FSR = ±2.048 V (unless otherwise noted).

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGIT	AL INPUTS/OUTPUTS		·			
V <sub>IH</sub>	High-level input voltage		0.7 VDD		VDD	V
$V_{IL}$	Low-level input voltage		GND		0.2 VDD	V
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = 1 mA	0.8 VDD			V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 1 mA	GND		0.2 VDD	V
I <sub>H</sub>	Input leakage, high	V <sub>IH</sub> = 5.5 V	-10		10	μΑ
IL	Input leakage, low	V <sub>IL</sub> = GND	-10		10	μΑ
POWE	R SUPPLY		"		'	
		Power-down, T <sub>A</sub> = 25°C		0.5	2	
	0	Power-down			5	
$I_{VDD}$	Supply current	Operating, T <sub>A</sub> = 25°C		150	200	μА
		Operating			300	
		VDD = 5 V		0.9		
$P_D$	Power dissipation	VDD = 3.3 V		0.5		mW
		VDD = 2 V		0.3		



## 7.6 Timing Requirements: Serial Interface

over operating ambient temperature range and VDD = 2 V to 5.5 V (unless otherwise noted)

		MIN	MAX	UNIT
t <sub>CSSC</sub>	Delay time, CS falling edge to first SCLK rising edge (1)	100		ns
t <sub>SCCS</sub>	Delay time, final SCLK falling edge to $\overline{\text{CS}}$ rising edge	100		ns
t <sub>CSH</sub>	Pulse duration, CS high	200		ns
t <sub>SCLK</sub>	SCLK period	250		ns
t <sub>SPWH</sub>	Pulse duration, SCLK high	100		ns
	Pulse duration, SCLK low <sup>(2)</sup>	100		ns
t <sub>SPWL</sub>	Pulse duration, SCLK low (-)		28	ms
t <sub>DIST</sub>	Setup time, DIN valid before SCLK falling edge	50		ns
t <sub>DIHD</sub>	Hold time, DIN valid after SCLK falling edge	50		ns
t <sub>DOHD</sub>	Hold time, SCLK rising edge to DOUT invalid	0		ns

 $<sup>\</sup>overline{\text{CS}}$  can be tied low permanently in case the serial bus is not shared with any other device. Holding SCLK low longer than 28 ms resets the SPI interface.

## 7.7 Switching Characteristics: Serial Interface

over operating ambient temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP MAX	UNIT
t <sub>CSDOD</sub>	Propagation delay time, CS falling edge to DOUT driven	DOUT load = 20 pF    100 kΩ to GND		100	ns
t <sub>DOPD</sub>	Propagation delay time, SCLK rising edge to valid new DOUT	DOUT load = 20 pF    100 kΩ to GND	0	50	ns
t <sub>CSDOZ</sub>	Propagation delay time, CS rising edge to DOUT high impedance	DOUT load = 20 pF    100 kΩ to GND		100	ns

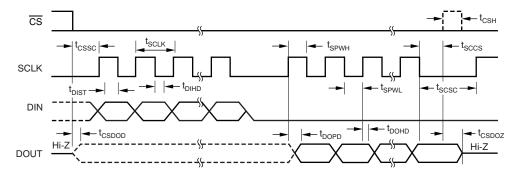


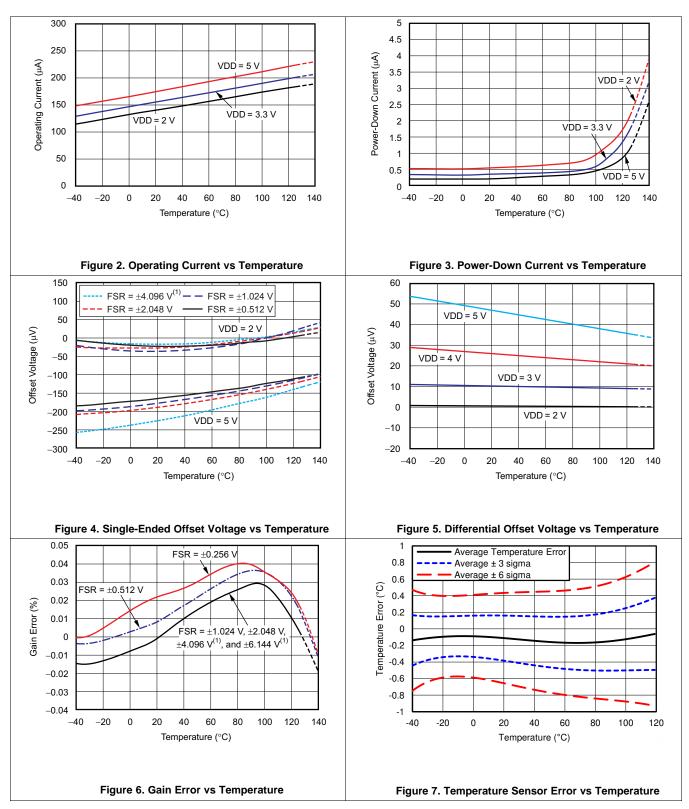
Figure 1. Serial Interface Timing

Submit Documentation Feedback



## 7.8 Typical Characteristics

at T<sub>A</sub> = 25°C, VDD = 3.3 V, and FSR = ±2.048 V (unless otherwise noted)



(1) This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3 V be applied to this device.



## 8 Detailed Description

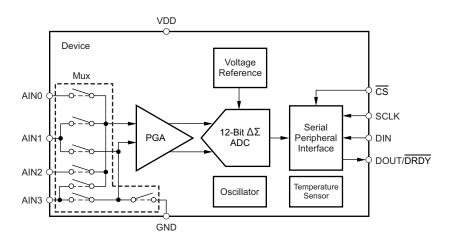
#### 8.1 Overview

The ADS1018 is a very small, low-power, noise-free, 12-bit, delta-sigma ( $\Delta\Sigma$ ) analog-to-digital converter (ADC). The ADS1018 consists of a  $\Delta\Sigma$  ADC core with adjustable gain, an internal voltage reference, a clock oscillator, and an SPI. This device is also a highly linear and accurate temperature sensor. All of these features are intended to reduce required external circuitry and improve performance. The *Functional Block Diagram* section shows the ADS1018 functional block diagram.

The ADS1018 ADC core measures a differential signal,  $V_{IN}$ , that is the difference of  $V_{(AINP)}$  and  $V_{(AINN)}$ . The converter core consists of a differential, switched-capacitor  $\Delta\Sigma$  modulator followed by a digital filter. This architecture results in a very strong attenuation in any common-mode signals. Input signals are compared to the internal voltage reference. The digital filter receives a high-speed bitstream from the modulator and outputs a code proportional to the input voltage.

The ADS1018 has two available conversion modes: single-shot and continuous-conversion. In single-shot mode, the ADC performs one conversion of the input signal upon request and stores the value to an internal conversion register. The device then enters a power-down state. This mode is intended to provide significant power savings in systems that require only periodic conversions or when there are long idle periods between conversions. In continuous-conversion mode, the ADC automatically begins a conversion of the input signal as soon as the previous conversion is completed. The rate of continuous conversion is equal to the programmed data rate. Data can be read at any time and always reflect the most recently completed conversion.

### 8.2 Functional Block Diagram



Submit Documentation Feedback



#### 8.3 Feature Description

## 8.3.1 Multiplexer

The ADS1018 contains an input multiplexer (mux), as shown in Figure 8. Either four single-ended or two differential signals can be measured. Additionally, AIN0, AIN1, and AIN2 can be measured differentially to AIN3. The multiplexer is configured by bits MUX[2:0] in the Config register. When single-ended signals are measured, the negative input of the ADC is internally connected to GND by a switch within the multiplexer.

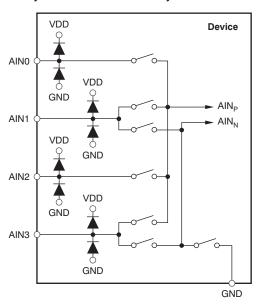


Figure 8. Input Multiplexer

When measuring single-ended inputs, the device does not output negative codes. These negative codes indicate negative differential signals; that is,  $(V_{(AINP)} - V_{(AINN)}) < 0$ . Electrostatic discharge (ESD) diodes to VDD and GND protect the ADS1018 inputs. To prevent the ESD diodes from turning on, keep the absolute voltage on any input within the range given in Equation 1:

$$GND - 0.3 \text{ V} < V_{(A|Nx)} < VDD + 0.3 \text{ V}$$
 (1)

If the voltages on the input pins can possibly violate these conditions, use external Schottky diodes and series resistors to limit the input current to safe values (see the *Absolute Maximum Ratings* table).

Also, overdriving one unused input on the ADS1018 may affect conversions currently taking place on other input pins. If overdriving unused inputs is possible, clamp the signal with external Schottky diodes.



## **Feature Description (continued)**

#### 8.3.2 Analog Inputs

The ADS1018 uses a switched-capacitor input stage where capacitors are continuously charged and then discharged to measure the voltage between AIN<sub>P</sub> and AIN<sub>N</sub>. This frequency at which the input signal is sampled is called the sampling frequency or the modulator frequency ( $f_{(MOD)}$ ). The ADS1018 has a 1-MHz internal oscillator which is further divided by a factor of 4 to generate the modulator frequency at 250 kHz. The capacitors used in this input stage are small, and to external circuitry, the average loading appears resistive. This structure is shown in Figure 9. The resistance is set by the capacitor values and the rate at which they are switched. Figure 10 shows the setting of the switches illustrated in Figure 9. During the sampling phase, switches S<sub>1</sub> are closed. This event charges  $C_{A1}$  to  $V_{(AINP)}$ ,  $C_{A2}$  to  $V_{(AINN)}$ , and  $C_{B}$  to  $(V_{(AINP)} - V_{(AINN)})$ . During the discharge phase, S<sub>1</sub> is first opened and then S<sub>2</sub> is closed. Both  $C_{A1}$  and  $C_{A2}$  then discharge to approximately 0.7 V and  $C_{B}$  discharges to 0 V. This charging draws a very small transient current from the source driving the ADS1018 analog inputs. The average value of this current can be used to calculate the effective impedance ( $Z_{eff}$ ), where  $Z_{eff} = V_{IN} / I_{AVERAGE}$ .

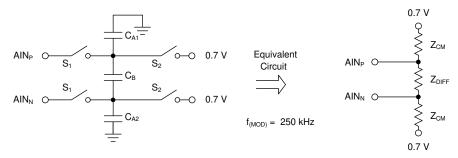


Figure 9. Simplified Analog Input Circuit

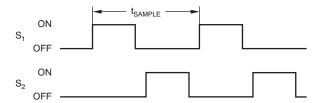


Figure 10. S<sub>1</sub> and S<sub>2</sub> Switch Timing

Common-mode input impedance is measured by applying a common-mode signal to the shorted  $AIN_P$  and  $AIN_N$  inputs and measuring the average current consumed by each pin. The common-mode input impedance changes depending on the full-scale range, but is approximately 6 M $\Omega$  for the default full-scale range. In Figure 9, the common-mode input impedance is  $Z_{CM}$ .

The differential input impedance is measured by applying a differential signal to  $AIN_P$  and  $AIN_N$  inputs where one input is held at 0.7 V. The current that flows through the pin connected to 0.7 V is the differential current and scales with the full-scale range. In Figure 9, the differential input impedance is  $Z_{DIFF}$ .

Make sure to consider the typical value of the input impedance. Unless the input source has a low impedance, the ADS1018 input impedance may affect the measurement accuracy. For sources with high output impedance, buffering may be necessary. Active buffers introduce noise, and also introduce offset and gain errors. Consider all of these factors in high-accuracy applications.

The clock oscillator frequency drifts slightly with temperature; therefore, the input impedances also drift. For most applications, this input impedance drift is negligible, and can be ignored.



## **Feature Description (continued)**

#### 8.3.3 Full-Scale Range (FSR) and LSB Size

A programmable gain amplifier (PGA) is implemented in front of the ADS1018  $\Delta\Sigma$  ADC core. The full-scale range is configured by bits PGA[2:0] in the Config register, and can be set to ±6.144 V, ±4.096 V, ±2.048 V, ±1.024 V, ±0.512 V, or ±0.256 V.

Table 1 shows the FSR together with the corresponding LSB size. Calculate the LSB size from the full-scale voltage by the formula shown in Equation 2. However, make sure that the analog input voltage never exceeds the analog input voltage range limit given in the *Electrical Characteristics*. If VDD greater than 4 V is used, the  $\pm 6.144$ -V full-scale range allows input voltages to extend up to the supply. Note though that in this case, or whenever the supply voltage is less than the full-scale range (for example, VDD = 3.3 V and full-scale range =  $\pm 4.096$  V), a full-scale ADC output code cannot be obtained. This inability means that some dynamic range is lost.

$$LSB = FSR / 2^{12}$$
 (2)

FSR LSB SIZE

±6.144 V<sup>(1)</sup> 3 mV

±4.096 V<sup>(1)</sup> 2 mV

±2.048 V 1 mV

±1.024 V 0.5 mV

±0.512 V 0.25 mV

Table 1. Full-Scale Range and Corresponding LSB Size

0.125 mV

±0.256 V

#### 8.3.4 Voltage Reference

The ADS1018 has an integrated voltage reference. An external reference cannot be used with this device. Errors associated with the initial voltage reference accuracy and the reference drift with temperature are included in the gain error and gain drift specifications in the *Electrical Characteristics*.

#### 8.3.5 Oscillator

The ADS1018 has an integrated oscillator running at 1 MHz. No external clock is required to operate the device. The internal oscillator drifts over temperature and time. The output data rate scales proportionally with the oscillator frequency.

Product Folder Links: ADS1018

Copyright © 2012-2019, Texas Instruments Incorporated

<sup>(1)</sup> This parameter expresses the full-scale range of the ADC scaling. Do not apply more than VDD + 0.3 V to this device.



#### 8.3.6 Temperature Sensor

The ADS1018 offers an integrated precision temperature sensor. To enable the temperature sensor mode, set bit TS\_MODE = 1 in the Config register. Temperature data are represented as a 12-bit result that is left-justified within the 16-bit conversion result. Data are output starting with the most significant byte (MSB). When reading the two data bytes, the first 12 bits are used to indicate the temperature measurement result. One 12-bit LSB equals 0.125°C. Negative numbers are represented in binary twos complement format, as shown in Table 2.

**Table 2. 12-Bit Temperature Data Format** 

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	HEX
128	0 100 0000 0000	400
127.875	0 011 1111 1111	3FF
100	0 011 0010 0000	320
80	0 010 1000 0000	280
75	0 010 0101 1000	258
50	0 001 1001 0000	190
25	0 000 1100 1000	0C8
0.25	0 000 0000 0010	002
0	0 000 0000 0000	000
-0.25	1 111 1111 1110	FFE
-25	1 111 0011 1000	F38
-40	1 110 1100 0000	EC0

#### 8.3.6.1 Converting from Temperature to Digital Codes

#### For positive temperatures:

Twos complement is not performed on positive numbers. Therefore, simply convert the number to binary code in a 12-bit, left justified format with the MSB = 0 to denote the positive sign.

**Example:**  $50^{\circ}$ C /  $(0.125^{\circ}$ C/count) = 400 = 190h =  $0001 \ 1001 \ 0000$ 

#### For negative temperatures:

Generate the twos complement of a negative number by complementing the absolute binary number and adding 1. Then, denote the negative sign with the MSB = 1.

**Example:**  $|-25^{\circ}C|$  / (0.125/count) = 200 = 0C8h = 0000 1100 1000 Twos complement format: 1111 0011 01111 + 1 = 1111 0011 1000

### 8.3.6.2 Converting from Digital Codes to Temperature

To convert from digital codes to temperature, first check whether the MSB is a 0 or a 1. If the MSB is a 0, simply multiply the decimal code by  $0.125^{\circ}$ C to obtain the result. If the MSB = 1, subtract 1 from the result and complement all of the bits. Then, multiply the result by  $-0.125^{\circ}$ C.

**Example:** The device reads back 258h: 258h has an MSB = 0.

 $258h \times 0.125$ °C =  $600 \times 0.125$ °C = +75°C

**Example:** The device reads back F38h: F38h has an MSB = 1.

Subtract 1 and complement the result: F38h → C8h

 $C8h \times (-0.125^{\circ}C) = 200 \times (-0.125^{\circ}C) = -25^{\circ}C$ 



#### 8.4 Device Functional Modes

#### 8.4.1 Reset and Power-Up

When the ADS1018 powers up, the device resets. As part of the reset process, the ADS1018 sets all bits in the Config register to the respective default settings. By default, the ADS1018 enters a power-down state at start-up. The device interface and digital blocks are active, but no data conversions are performed. The initial power-down state of the ADS1018 relieves systems with tight power-supply requirements from encountering a surge during power-up.

#### 8.4.2 Operating Modes

The ADS1018 operates in one of two modes: continuous-conversion or single-shot. The MODE bit in the Config register selects the respective operating mode.

#### 8.4.2.1 Single-Shot Mode and Power-Down

When the MODE bit in the Config register is set to 1, the ADS1018 enters a power-down state, and operates in single-shot mode. This power-down state is the default state for the ADS1018 when power is first applied. Although powered down, the device still responds to commands. The ADS1018 remains in this power-down state until a 1 is written to the single-shot (SS) bit in the Config register. When the SS bit is asserted, the device powers up, resets the SS bit to 0, and starts a single conversion. When conversion data are ready for retrieval, the device powers down again. Writing a 1 to the SS bit while a conversion is ongoing has no effect. To switch to continuous-conversion mode, write a 0 to the MODE bit in the Config register.

#### 8.4.2.2 Continuous-Conversion Mode

In continuous-conversion mode (MODE bit set to 0), the ADS1018 continuously performs conversions. When a conversion completes, the ADS1018 places the result in the Conversion register and immediately begins another conversion. To switch to single-shot mode, write a 1 to the MODE bit in the Config register, or reset the device.

#### 8.4.3 Duty Cycling for Low Power

The noise performance of a  $\Delta\Sigma$  ADC generally improves when lowering the output data rate because more samples of the internal modulator are averaged to yield one conversion result. In applications where power consumption is critical, the improved noise performance at low data rates may not be required. For these applications, the ADS1018 supports duty cycling that can yield significant power savings by periodically requesting high data-rate readings at an effectively lower data rate.

For example, an ADS1018 in power-down state with a data rate set to 3300 SPS can be operated by a microcontroller that instructs a single-shot conversion every 7.8 ms (128 SPS). A conversion at 3300 SPS only requires approximately 0.3 ms; therefore, the ADS1018 enters power-down state for the remaining 7.5 ms. In this configuration, the ADS1018 consumes approximately 1/25 the power that is otherwise consumed in continuous-conversion mode. The duty cycling rate is completely arbitrary and is defined by the master controller. The ADS1018 offers lower data rates that do not implement duty cycling and also offers improved noise performance, if required.



## 8.5 Programming

#### 8.5.1 Serial Interface

The SPI-compatible serial interface consists of either four signals ( $\overline{CS}$ , SCLK, DIN, and DOUT/ $\overline{DRDY}$ ), or three signals (SCLK, DIN, and DOUT/ $\overline{DRDY}$ ), with  $\overline{CS}$  tied low). The interface is used to read conversion data, read from and write to registers, and control device operation.

## 8.5.2 Chip Select (CS)

The chip select pin ( $\overline{\text{CS}}$ ) selects the ADS1018 for SPI communication. This feature is useful when multiple devices share the same serial bus. Keep  $\overline{\text{CS}}$  low for the duration of the serial communication. When  $\overline{\text{CS}}$  is taken high, the serial interface is reset, SCLK is ignored, and DOUT/ $\overline{\text{DRDY}}$  enters a high-impedance state. In this state, DOUT/ $\overline{\text{DRDY}}$  cannot provide data-ready indication. In situations where multiple devices are present and DOUT/ $\overline{\text{DRDY}}$  must be monitored, lower  $\overline{\text{CS}}$  periodically. At this point, the DOUT/ $\overline{\text{DRDY}}$  pin either immediately goes high to indicate that no new data are available, or immediately goes low to indicate that new data are present in the Conversion register and are available for transfer. New data can be transferred at any time without concern of data corruption. When a transmission starts, the current result is locked into the output shift register and does not change until the communication completes. This system avoids any possibility of data corruption.

#### 8.5.3 Serial Clock (SCLK)

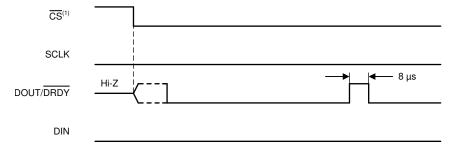
The serial clock pin (SCLK) features a Schmitt-triggered input and is used to clock data on the DIN and DOUT/DRDY pins into and out of the ADS1018. Even though the input has hysteresis, keep SCLK as clean as possible to prevent glitches from accidentally shifting the data. To reset the serial interface, hold SCLK low for 28 ms, and the next SCLK pulse starts a new communication cycle. Use this time-out feature to recover communication when a serial interface transmission is interrupted. When the serial interface is idle, hold SCLK low.

#### 8.5.4 Data Input (DIN)

The data input pin (DIN) is used along with SCLK to send data to the ADS1018. The device latches data on DIN at the SCLK falling edge. The ADS1018 never drives the DIN pin.

## 8.5.5 Data Output and Data Ready (DOUT/DRDY)

The data output and data ready pin (DOUT/DRDY) is used with SCLK to read conversion and register data from the ADS1018. Data on DOUT/DRDY are shifted out on the SCLK rising edge. DOUT/DRDY is also used to indicate that a conversion is complete and new data are available. This pin transitions low when new data are ready for retrieval. DOUT/DRDY is also able to trigger a microcontroller to start reading data from the ADS1018. In continuous-conversion mode, DOUT/DRDY transitions high again 8 µs before the next data ready signal (DOUT/DRDY low) if no data are retrieved from the device. This transition is shown in Figure 11. Complete the data transfer before DOUT/DRDY returns high.



(1)  $\overline{\text{CS}}$  can be held low if the ADS1018 does not share the serial bus with another device. If  $\overline{\text{CS}}$  is low, DOUT/ $\overline{\text{DRDY}}$  asserts low indicating new data are available.

Figure 11. DOUT/DRDY Behavior Without Data Retrieval in Continuous-Conversion Mode

When  $\overline{CS}$  is high,  $\overline{DOUT/DRDY}$  is configured by default with a weak internal pullup resistor. This feature reduces the risk of DOUT/DRDY floating near midsupply and causing leakage current in the master device. To disable this pullup resistor and place the device into a high-impedance state, set the PULL\_UP\_EN bit to 0 in the Config register.



## Programming (continued)

#### 8.5.6 Data Format

The ADS1018 provides 12 bits of data in binary twos complement format that is left justified within the 16-bit data word. A positive full-scale (+FS) input produces an output code of 7FF0h and a negative full-scale (-FS) input produces an output code of 8000h. The output clips at these codes for signals that exceed full-scale. Table 3 summarizes the ideal output codes for different input signals. Figure 12 shows code transitions versus input voltage.

Table 3. Input Signal versus Ideal Output Code

(1) Excludes the effects of noise, INL, offset, and gain errors.

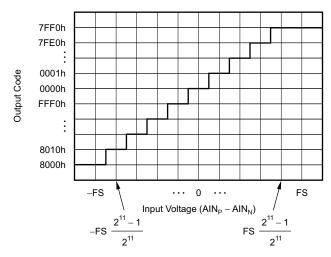


Figure 12. Code Transition Diagram

#### 8.5.7 Data Retrieval

Data is written to and read from the ADS1018 in the same manner for both single-shot and continuous conversion modes, without having to issue any commands. The operating mode for the ADS1018 is selected by the MODE bit in the Config register.

Set the MODE bit to 0 to put the device in continuous-conversion mode. In continuous-conversion mode, the device is constantly starting new conversions even when  $\overline{\text{CS}}$  is high.

Set the MODE bit to 1 for single-shot mode. In single-shot mode, a new conversion only starts by writing a 1 to the SS bit.

The conversion data are always buffered, and retain the current data until replaced by new conversion data. Therefore, data can be read at any time without concern of data corruption. When DOUT/DRDY asserts low, indicating that new conversion data are ready, the conversion data are read by shifting the data out on DOUT/DRDY. The MSB of the data (bit 15) on DOUT/DRDY is clocked out on the first SCLK rising edge. At the same time that the conversion result is clocked out of DOUT/DRDY, new Config register data are latched on DIN on the SCLK falling edge.

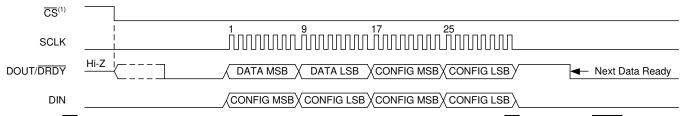
The ADS1018 also offers the possibility of direct readback of the Config register settings in the same data transmission cycle. One complete data transmission cycle consists of either 32 bits (when the Config register data readback is used) or 16 bits (only used when the CS line can be controlled and is not permanently tied low).



#### 8.5.7.1 32-Bit Data Transmission Cycle

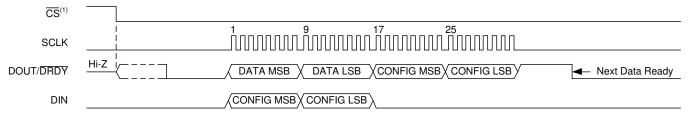
The data in a 32-bit data transmission cycle consist of four bytes: two bytes for the conversion result, and an additional two bytes for the Config register readback. The device always reads the MSB first.

Write the same Config register setting twice during one transmission cycle as shown in Figure 13. If convenient, write the Config register setting once during the first half of the transmission cycle, and then hold the DIN pin either low (as shown in Figure 14) or high during the second half of the cycle. If no update to the Config register is required, hold the DIN pin either low or high during the entire transmission cycle. The Config register setting written in the first two bytes of a 32-bit transmission cycle is read back in the last two bytes of the same cycle.



(1)  $\overline{\text{CS}}$  can be held low if the ADS1018 does not share the serial bus with another device. If  $\overline{\text{CS}}$  is low, DOUT/ $\overline{\text{DRDY}}$  asserts low indicating new data are available.

Figure 13. 32-Bit Data Transmission Cycle With Config Register Readback



(1)  $\overline{\text{CS}}$  can be held low if the ADS1018 does not share the serial bus with another device. If  $\overline{\text{CS}}$  is low, DOUT/ $\overline{\text{DRDY}}$  asserts low indicating new data are available.

Figure 14. 32-Bit Data Transmission Cycle: DIN Held Low

## 8.5.7.2 16-Bit Data Transmission Cycle

If Config register data are not required to be read back, the ADS1018 conversion data can be clocked out in a short 16-bit data transmission cycle, as shown in Figure 15. Take CS high after the 16th SCLK cycle to reset the SPI interface. The next time CS is taken low, data transmission starts with the currently buffered conversion result on the first SCLK rising edge. If DOUT/DRDY is low when data retrieval starts, the conversion buffer is already updated with a new result. Otherwise, if DOUT/DRDY is high, the same result from the previous data transmission cycle is read.

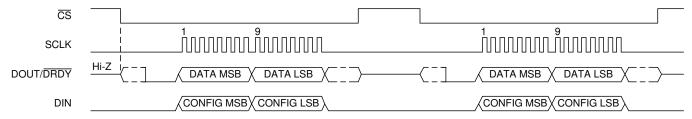


Figure 15. 16-Bit Data Transmission Cycle

Copyright © 2012–2019, Texas Instruments Incorporated Product Folder Links: *ADS1018* 



#### 8.6 Register Maps

The ADS1018 has two registers that are accessible through the SPI. The Conversion register contains the result of the last conversion. The Config register allows the user to change the ADS1018 operating modes and query the status of the devices.

#### 8.6.1 Conversion Register [reset = 0000h]

The 16-bit Conversion register contains the result of the last conversion in binary twos complement format. Following power up, the Conversion register is cleared to 0, and remains 0 until the first conversion is complete. The register format is shown in Figure 16.

Figure 16. Conversion Register

15	14	13	12	11	10	9	8		
D11	D10	D9	D8	D7	D6	D5	D4		
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h		
7	6	5	4	3	2	1	0		
D3	D2	D1	D0						
R-0h	R-0h	R-0h	R-0h	Reserved R-0h					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

#### **Table 4. Conversion Register Field Descriptions**

Bit	Field	Туре	Reset	Description
15:4	D[11:0]	R	000h	12-bit conversion result
3:0	Reserved	R	0h	Always reads back 0h

## 8.6.2 Config Register [reset = 058Bh]

The 16-bit Config register can be used to control the ADS1018 operating mode, input selection, data rate, full-scale range, and temperature sensor mode. The register format is shown in Figure 17.

Figure 17. Config Register

15	14	13	12	11	10	9	8
SS		MUX[2:0]			MODE		
R/W-0h		R/W-0h			R/W-1h		
7	6	5	4	3	2	1	0
	DR[2:0]		TS_MODE	PULL_UP_EN	NOP	[1:0]	Reserved
	R/W-4h		R/W-0h	R/W-1h	R/W	′-1h	R-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

### **Table 5. Config Register Field Descriptions**

Bit	Field	Туре	Reset	Description
				Single-shot conversion start This bit is used to start a single conversion. SS can only be written when in power-down state and has no effect when a conversion is ongoing.
15	SS	R/W	0h	When writing: 0 = No effect 1 = Start a single conversion (when in power-down state) Always reads back 0 (default).



## Table 5. Config Register Field Descriptions (continued)

Bit	Field	Туре	Reset	Description (continued)
	Ticiu	Турс	Reset	Input multiplexer configuration
14:12	MUX[2:0]	R/W	Oh	These bits configure the input multiplexer. $000 = \text{AIN}_{\text{P}} \text{ is AINO and AIN}_{\text{N}} \text{ is AIN1 (default)} \\ 001 = \text{AIN}_{\text{P}} \text{ is AINO and AIN}_{\text{N}} \text{ is AIN3} \\ 010 = \text{AIN}_{\text{P}} \text{ is AIN1 and AIN}_{\text{N}} \text{ is AIN3} \\ 011 = \text{AIN}_{\text{P}} \text{ is AIN2 and AIN}_{\text{N}} \text{ is AIN3} \\ 100 = \text{AIN}_{\text{P}} \text{ is AINO and AIN}_{\text{N}} \text{ is GND} \\ 101 = \text{AIN}_{\text{P}} \text{ is AIN1 and AIN}_{\text{N}} \text{ is GND} \\ 110 = \text{AIN}_{\text{P}} \text{ is AIN2 and AIN}_{\text{N}} \text{ is GND} \\ 111 = \text{AIN}_{\text{P}} \text{ is AIN3 and AIN}_{\text{N}} \text{ is GND}$
11:9	PGA[2:0]	R/W	2h	Programmable gain amplifier configuration These bits configure the programmable gain amplifier. $000 = FSR \text{ is } \pm 6.144 \text{ V}^{(1)}$ $001 = FSR \text{ is } \pm 4.096 \text{ V}^{(1)}$ $010 = FSR \text{ is } \pm 2.048 \text{ V} \text{ (default)}$ $011 = FSR \text{ is } \pm 1.024 \text{ V}$ $100 = FSR \text{ is } \pm 0.512 \text{ V}$ $101 = FSR \text{ is } \pm 0.256 \text{ V}$ $110 = FSR \text{ is } \pm 0.256 \text{ V}$ $111 = FSR \text{ is } \pm 0.256 \text{ V}$
8	MODE	R/W	1h	Device operating mode This bit controls the ADS1018 operating mode.  0 = Continuous-conversion mode 1 = Power-down and single-shot mode (default)
7:5	DR[2:0]	R/W	4h	Data rate These bits control the data-rate setting.  000 = 128 SPS 001 = 250 SPS 010 = 490 SPS 011 = 920 SPS 100 = 1600 SPS (default) 101 = 2400 SPS 110 = 3300 SPS 111 = Not Used
4	TS_MODE	R/W	0h	Temperature sensor mode This bit configures the ADC to convert temperature or input signals.  0 = ADC mode (default) 1 = Temperature sensor mode
3	PULL_UP_EN	R/W	1h	Pullup enable This bit enables a weak internal pullup resistor on the DOUT/DRDY pin only when CS is high. When enabled, an internal 400-kΩ resistor connects the bus line to supply. When disabled, the DOUT/DRDY pin floats.  0 = Pullup resistor disabled on DOUT/DRDY pin 1 = Pullup resistor enabled on DOUT/DRDY pin (default)
2:1	NOP[1:0]	R/W	1h	No operation The NOP[1:0] bits control whether data are written to the Config register or not. For data to be written to the Config register, the NOP[1:0] bits must be 01. Any other value results in a NOP command. DIN can be held high or low during SCLK pulses without data being written to the Config register.  00 = Invalid data; do not update the contents of the Config register 01 = Valid data; update the Config register (default) 10 = Invalid data; do not update the contents of the Config register 11 = Invalid data; do not update the contents of the Config register
	December	В	1 h	Reserved
0	Reserved	R	1h	Writing either 0 or 1 to this bit has no effect. Always reads back 1.

<sup>(1)</sup> This parameter expresses the full-scale range of the ADC scaling. Do not apply more than VDD + 0.3 V to this device.



## 9 Application and Implementation

#### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The ADS1018 is a precision, 12-bit  $\Delta\Sigma$  ADC that offers many integrated features to ease the measurement of the most common sensor types including various type of temperature and bridge sensors. The following sections give example circuits and suggestions for using the ADS1018 in various situations.

#### 9.1.1 Serial Interface Connections

The principle serial interface connections for the ADS1018 are shown in Figure 18.

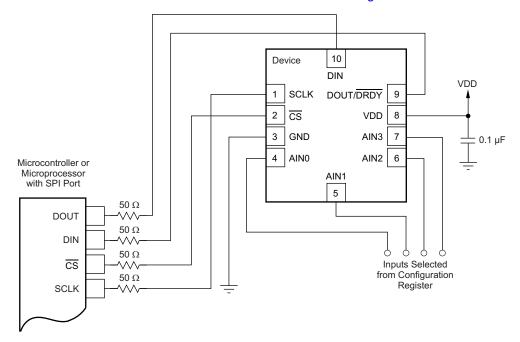


Figure 18. Typical Connections

Most microcontroller SPI peripherals operate with the ADS1018. The interface operates in SPI mode 1 where CPOL = 0 and CPHA = 1, SCLK idles low, and data are launched or changed only on SCLK rising edges; data are latched or read by the master and slave on SCLK falling edges. Details of the SPI communication protocol employed by the ADS1018 can be found in the *Timing Requirements: Serial Interface* section.

It is a good practice to place  $50-\Omega$  resistors in the series path to each of the digital pins to provide some short-circuit protection. Take care to still meet all SPI timing requirements because these additional series resistors along with the bus parasitic capacitances present on the digital signal lines slews the signals.

The fully-differential input of the ADS1018 is ideal for connecting to differential sources (such as thermocouples and thermistors) with a moderately low source impedance. Although the ADS1018 can read fully-differential signals, the device cannot accept negative voltages on either of its inputs because of ESD protection diodes on each pin. When an input exceeds supply or drops below ground, these diodes turn on to prevent any ESD damage to the device.



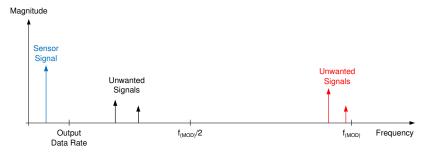
#### 9.1.2 GPIO Ports for Communication

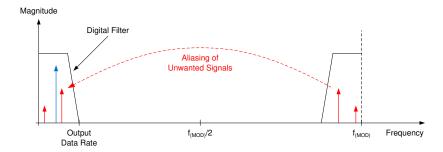
Most microcontrollers have programmable input/output (I/O) pins that can be set in software to act as inputs or outputs. If an SPI controller is not available, the ADS1018 can be connected to GPIO pins and the SPI bus protocol can be simulated. Using GPIO pins to generate the SPI interface requires only that the pins be configured as push or pull inputs or outputs. Furthermore, if the SCLK line is held low for more than 28 ms, communication times out. This condition means that the GPIO ports must be capable of providing SCLK pulses with no more than 28 ms between pulses.

#### 9.1.3 Analog Input Filtering

Analog input filtering serves two purposes: first, to limit the effect of aliasing during the sampling process and second, to reduce external noise from being a part of the measurement.

As with any sampled system, aliasing can occur if proper antialias filtering is not in place. Aliasing occurs when frequency components are present in the input signal that are higher than half the sampling frequency of the ADC (also known as the *Nyquist frequency*). These frequency components fold back and show up in the actual frequency band of interest below half the sampling frequency. The filter response of the digital filter repeats at multiples of the sampling frequency, also known as modulator frequency  $f_{(MOD)}$ , as shown in Figure 19. Signals or noise up to a frequency where the filter response repeats are attenuated to a certain amount by the digital filter depending on the filter architecture. Any frequency components present in the input signal around the modulator frequency or multiples thereof are not attenuated and alias back into the band of interest, unless attenuated by an external analog filter.





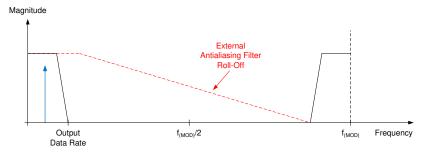


Figure 19. Effect of Aliasing

Submit Documentation Feedback

Copyright © 2012–2019, Texas Instruments Incorporated



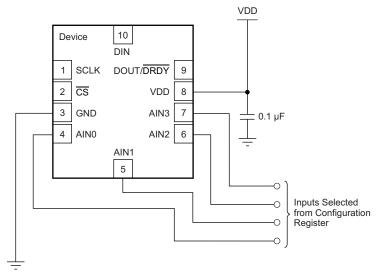
Many sensor signals are inherently band-limited; for example, the output of a thermocouple has a limited rate of change. In this case the sensor signal does not alias back into the pass-band when using a  $\Delta\Sigma$  ADC. However, any noise pickup along the sensor wiring or the application circuitry can potentially alias into the pass band. Power line-cycle frequency and harmonics are one common noise source. External noise can also be generated from electromagnetic interference (EMI) or radio frequency interference (RFI) sources, such as nearby motors and cellular phones. Another noise source typically exists on the printed-circuit-board (PCB) itself in the form of clocks and other digital signals. Analog input filtering helps remove unwanted signals from affecting the measurement result.

A first-order, resistor-capacitor (RC) filter is, in most cases, sufficient to either totally eliminate aliasing, or to reduce the effect of aliasing to a level within the noise floor of the sensor. Ideally, any signal beyond  $f_{(MOD)}$  / 2 is attenuated to a level below the noise floor of the ADC. The digital filter of the ADS1018 attenuates signals to a certain degree. In addition, noise components are usually smaller in magnitude than the actual sensor signal. Therefore, using a first-order RC filter with a cutoff frequency set at the output data rate or ten times higher is generally a good starting point for a system design.

#### 9.1.4 Single-Ended Inputs

Although the ADS1018 has two differential inputs, the device can measure four single-ended signals. Figure 20 shows a single-ended connection scheme. The ADS1018 is configured for single-ended measurement by configuring the mux to measure each channel with respect to ground. Data are then read out of one input based on the selection in the Config register. The single-ended signal can range from 0 V up to positive supply or +FS, whichever is lower. Negative voltages cannot be applied to this circuit because the ADS1018 can only accept positive voltages with respect to ground. The ADS1018 does not lose linearity within the input range.

The ADS1018 offers a differential input voltage range of ±FS. The single-ended circuit shown in Figure 20, however, only uses the positive half of the ADS1018 FS input voltage range because differentially negative inputs are not produced. Because only half of the FS range is used, one bit of resolution is lost. For optimal noise performance, use differential configurations whenever possible. Differential configurations maximize the dynamic range of the ADC and provide strong attenuation of common-mode noise.



NOTE: Digital pin connections omitted for clarity.

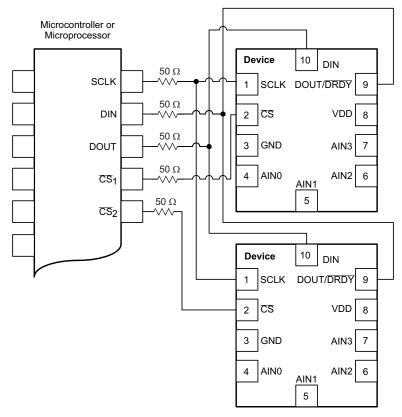
Figure 20. Measuring Single-Ended Inputs

The ADS1018 also allows AIN3 to serve as a common point for measurements by adjusting the mux configuration. AIN0, AIN1, and AIN2 can all be measured with respect to AIN3. In this configuration, the ADS1018 operates with inputs where AIN3 serves as the common point. This ability improves the usable range over the single-ended configuration because negative differential voltages are allowed when GND  $< V_{(AIN3)} < VDD$ ; however, common-mode noise attenuation is not offered.



#### 9.1.5 Connecting Multiple Devices

When connecting multiple ADS1018 devices to a single SPI bus, SCLK, DIN, and DOUT/\overline{DRDY} can be safely shared by using a dedicated chip-select (CS) for each SPI-enabled device. By default, when CS goes high for the ADS1018, DOUT/DRDY is pulled up to VDD by a weak pullup resistor. This feature prevents DOUT/DRDY from floating near midrail and causing excess current leakage on a microcontroller input. If the PULL\_UP\_EN bit in the Config register is set to 0, the DOUT/DRDY pin enters a 3-state mode when CS transitions high. The ADS1018 cannot issue a data-ready pulse on DOUT/DRDY when CS is high. To evaluate when a new conversion is ready from the ADS1018 when using multiple devices, the master can periodically drop CS to the ADS1018. When CS goes low, the DOUT/DRDY pin immediately drives either high or low. If the DOUT/DRDY line drives low on a low CS, new data are currently available for clocking out at any time. If the DOUT/DRDY line drives high, no new data are available and the ADS1018 returns the last read conversion result. Valid data can be retrieved from the ADS1018 at anytime without concern of data corruption. If a new conversion becomes available during data transmission, that conversion is not available for readback until a new SPI transmission is initiated.



NOTE: Power and input connections omitted for clarity.

Figure 21. Connecting Multiple ADS1018s



#### 9.1.6 Pseudo Code Example

The flow chart in Figure 22 shows a pseudo-code sequence with the required steps to set up communication between the device and a microcontroller to take subsequent readings from the ADS1018. As an example, the default Config register settings are changed to set up the device for FSR =  $\pm 0.512$  V, continuous-conversion mode, and a 920-SPS data rate.

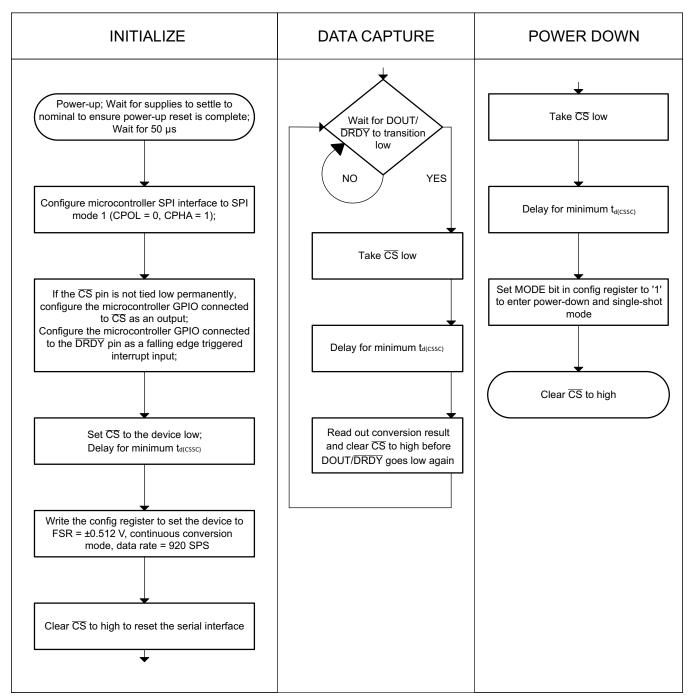


Figure 22. Pseudo-Code Example Flowchart



## 9.2 Typical Application

Figure 23 shows the basic connections for an independent, two-channel thermocouple measurement system when using the internal high-precision temperature sensor for cold-junction compensation. Apart from the thermocouples, the only external circuitry required are biasing resistors; first-order, low-pass, antialiasing filters; and a power-supply decoupling capacitor.

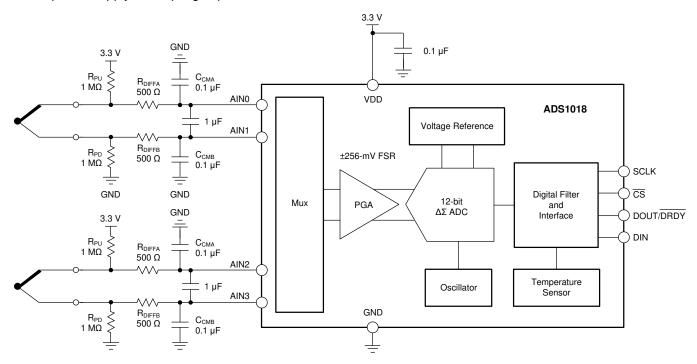


Figure 23. Two-Channel Thermocouple Measurement System

#### 9.2.1 Design Requirements

Table 6 lists the design parameters for this application.

 DESIGN PARAMETER
 VALUE

 Supply voltage
 3.3 V 

 Full-scale range
  $\pm 0.256 \text{ V}$  

 Update rate
  $\geq 100 \text{ readings per second}$  

 Thermocouple type
 K

 Temperature measurement range
  $-200^{\circ}\text{C to } +1250^{\circ}\text{C}$  

 Measurement accuracy at  $T_A = 25^{\circ}\text{C}^{(1)}$   $\pm 2.7^{\circ}\text{C}$ 

**Table 6. Design Parameters** 

#### 9.2.2 Detailed Design Procedure

The biasing resistors ( $R_{PU}$  and  $R_{PD}$ ) serve two purposes. The first purpose is to set the common-mode voltage of the thermocouple to within the specified voltage range of the device. The second purpose is to offer a weak pullup and pulldown to detect an open thermocouple lead. When one of the thermocouple leads fails open, the positive input is pulled to VDD and the negative input is pulled to GND. The ADC consequently reads a full-scale value that is outside the normal measurement range of the thermocouple voltage to indicate this failure condition. When choosing the values of the biasing resistors, take care so that the biasing current does not degrade measurement accuracy. The biasing current flows through the thermocouple and can cause self-heating and additional voltage drops across the thermocouple leads. Typical values for the biasing resistors range from 1  $M\Omega$  to 50  $M\Omega$ .

<sup>(1)</sup> With offset calibration, and no gain calibration. Measurement does not account for thermocouple inaccuracy.



Although the device digital filter attenuates high-frequency components of noise, provide a first-order, passive RC filter at the inputs to further improve performance. The differential RC filter formed by  $R_{\text{DIFFA}}$ ,  $R_{\text{DIFFB}}$ , and the differential capacitor  $C_{\text{DIFF}}$  offers a cutoff frequency that is calculated using Equation 3. While the digital filter of the ADS1018 strongly attenuates high-frequency components of noise, provide a first-order, passive RC filter to further suppress high-frequency noise and avoid aliasing. Care must be taken when choosing the filter resistor values because the input currents flowing into and out of the device cause a voltage drop across the resistors. This voltage drop shows up as an additional offset error at the ADC inputs. Limit the filter resistor values to below 1 k $\Omega$  for best performance.

$$f_C = 1 / [2\pi \times (R_{DIFFA} + R_{DIFFB}) \times C_{DIFF}]$$
(3)

Two common-mode filter capacitors ( $C_{CMA}$  and  $C_{CMB}$ ) are also added to offer attenuation of high-frequency, common-mode noise components. Differential capacitor  $C_{DIFF}$  must be at least an order of magnitude (10x) larger than these common-mode capacitors because mismatches in the common-mode capacitors can convert common-mode noise into differential noise.

The highest measurement resolution is achieved when the largest potential input signal is slightly lower than the FSR of the ADC. From the design requirement, the maximum thermocouple voltage ( $V_{TC}$ ) occurs at a thermocouple temperature ( $T_{TC}$ ) of 1250°C. At this temperature,  $V_{TC} = 50.644$  mV, as defined in the tables published by the National Institute of Standards and Technology (NIST) using a cold-junction temperature ( $T_{CJ}$ ) of 0°C. A thermocouple produces an output voltage that is proportional to the temperature difference between the thermocouple tip and the cold junction. If the cold junction is at a temperature below 0°C, the thermocouple produces a voltage larger than 50.644 mV. The isothermal block area is constrained by the operating temperature range of the device. Therefore, the isothermal block temperature is limited to -40°C. A K-type thermocouple at  $T_{TC} = 1250$ °C produces an output voltage of  $V_{TC} = 50.644$  mV - (-1.527 mV) = 52.171 mV when referenced to a cold-junction temperature of  $T_{CJ} = -40$ °C. The device offers a full-scale range of  $\pm 0.256$  V and that is what is used in this application example.

The device integrates a high-precision temperature sensor that can be used to measure the temperature of the cold junction. The temperature sensor mode is enabled by setting bit TS\_MODE = 1 in the Config register. The accuracy of the overall temperature sensor depends on how accurately the ADS1018 can measure the cold junction, and hence, careful component placement and PCB layout considerations must be employed for designing an accurate thermocouple system. The ADS1118 Evaluation Module provides a good starting point and offers an example to achieve good cold-junction compensation performance. The ADS1118 Evaluation Module uses the same schematic as shown in Figure 23, except with only one thermocouple channel connected. Refer to the application note, *Precision Thermocouple Measurement With the ADS1118*, SBAA189, for details on how to optimize your component placement and layout to achieve good cold-junction compensation performance.

The calculation procedure to achieve cold-junction compensation can be done in several ways. A typical way is to interleave readings between the thermocouple inputs and the temperature sensor. That is, acquire one on-chip temperature result,  $T_{CJ}$ , for every thermocouple ADC voltage measured,  $V_{TC}$ . To account for the cold junction, first convert the temperature sensor reading within the ADS1018 to a voltage  $(V_{CJ})$  that is proportional to the thermocouple currently being used. This process is generally accomplished by performing a reverse lookup on the table used for the thermocouple voltage-to-temperature conversion. Adding these two voltages yields the thermocouple-compensated voltage  $(V_{Actual})$ , where  $V_{Actual} = V_{CJ} + V_{TC}$ . Then,  $V_{Actual}$  is converted to a temperature  $(T_{Actual})$  using the same NIST lookup table. A block diagram showing this process is given in Figure 24. Refer to application note SBAA189 for a detailed explanation of this method.



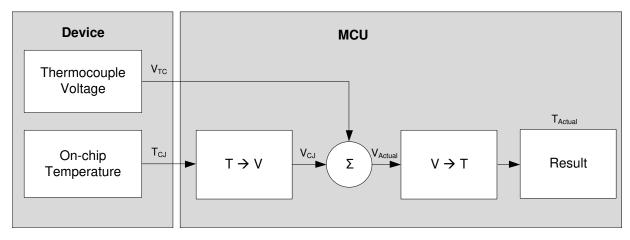
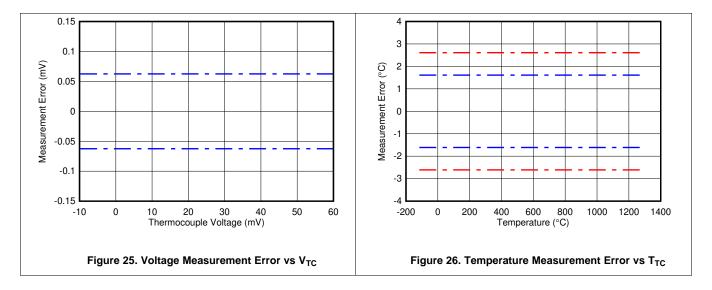


Figure 24. Software-Flow Block Diagram

Figure 25 and Figure 26 show the expected measurement results. A system offset calibration is performed at  $T_{TC}$  = 25°C that equates to  $V_{TC}$  = 0 V when  $T_{CJ}$  = 25°C. The dashed blue lines in Figure 25 show the maximum error guard band due to ADC gain and nonlinearity error. The dashed blue lines in Figure 26 show the corresponding temperature measurement error guard band calculated from the data in Figure 25 using the NIST tables. The dashed red lines in Figure 26 include the guard band for the temperature sensor inaccuracy (±1°C), in addition to the device gain and nonlinearity error. Note that the results in Figure 25 and Figure 26 do not account for the thermocouple inaccuracy that must also be considered while designing a thermocouple measurement system.

#### 9.2.3 Application Curves



Submit Documentation Feedback

Copyright © 2012–2019, Texas Instruments Incorporated



## 10 Power Supply Recommendations

The device requires a single power supply, VDD, to power both the analog and digital circuitry of the device.

## 10.1 Power-Supply Sequencing

Wait approximately 50 µs after VDD is stabilized before communicating with the device to allow the power-up reset process to complete.

#### 10.2 Power-Supply Decoupling

Good power-supply decoupling is important to achieve optimum performance. VDD must be decoupled with at least a  $0.1-\mu F$  capacitor, as shown in Figure 27. The  $0.1-\mu F$  bypass capacitor supplies the momentary bursts of extra current required from the supply when the ADS1018 is converting. Place the bypass capacitor as close to the power-supply pin of the device as possible using low-impedance connections. For best performance, use multilayer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

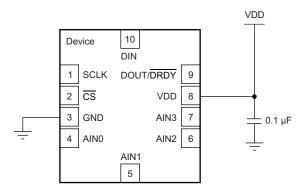


Figure 27. Power-Supply Decoupling



## 11 Layout

### 11.1 Layout Guidelines

Use best design practices when laying out a printed-circuit-board (PCB) for both analog and digital components. This recommendation generally means that the layout separates analog components [such as ADCs, amplifiers, references, digital-to-analog converters (DACs), and analog muxes] from digital components [such as microcontrollers, complex programmable logic devices (CPLDs), field-programmable gate arrays (FPGAs), radio frequency (RF) transceivers, universal serial bus (USB) transceivers, and switching regulators]. An example of good component placement is shown in Figure 28. Although Figure 28 provides a good example of component placement, the best placement for each application is unique to the geometries, components, and PCB fabrication capabilities employed. That is, there is no single layout that is perfect for every design and careful consideration must always be used when designing with any analog component.

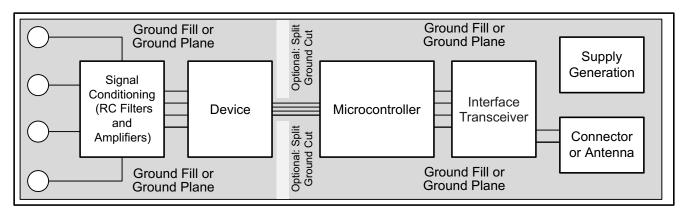


Figure 28. System Component Placement

The use of split analog and digital ground planes is not necessary for improved noise performance (although for thermal isolation this option is a worthwhile consideration). However, the use of a solid ground plane or ground fill in PCB areas with no components is essential for optimum performance. If the system being used employs a split digital and analog ground plane, TI generally recommends that the ground planes be connected together as close to the device as possible. A two-layer board is possible using common grounds for both analog and digital grounds. Additional layers can be added to simplify PCB trace routing. Ground fill may also reduce EMI and RFI issues.

For best system performance, keep digital components, especially RF portions, as far as practically possible from analog circuitry in a given system. Additionally, minimize the distance that digital control traces run through analog areas and avoid placing these traces near sensitive analog components. Digital return currents usually flow through a ground path that is as close to the digital path as possible. If a solid ground connection to a plane is not available, these currents may find paths back to the source that interfere with analog performance. The implications that layout has on the temperature-sensing functions are much more significant than for ADC functions.

Bypass supply pins to ground with a low-ESR ceramic capacitor. The optimum placement of the bypass capacitors is as close as possible to the supply pins. The ground-side connections of the bypass capacitors must be low-impedance connections for optimum performance. The supply current flows through the bypass capacitor terminal first and then to the supply pin to make the bypassing most effective.

Analog inputs with differential connections must have a capacitor placed differentially across the inputs. Use high-quality differential capacitors. The best ceramic-chip capacitors are COG (NPO), with stable properties and low-noise characteristics. Thermally isolate a copper region around the thermocouple input connections to create a thermally-stable cold junction. Obtaining acceptable performance with alternate layout schemes is possible as long as the above guidelines are followed.

See Figure 29 and Figure 30 for layout examples of the X2QFN and VSSOP packages.



## 11.2 Layout Example

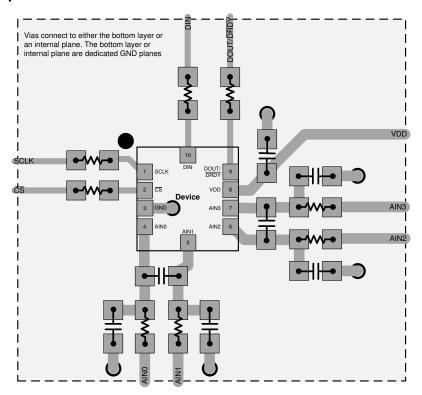


Figure 29. X2QFN Package

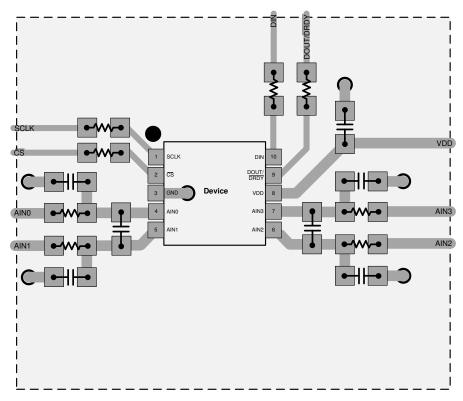


Figure 30. VSSOP Package

Copyright © 2012–2019, Texas Instruments Incorporated

Submit Documentation Feedback



## 12 Device and Documentation Support

## 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, Precision Thermocouple Measurement with the ADS1118 application reports
- Texas Instruments, ADS1118EVM User Guide and Software Tutorial user guide
- Texas Instruments, 430BOOST-ADS1118 BoosterPack user guide
- Texas Instruments, ADS1118 Boosterpack quick start
- Texas Instruments, A Glossary of Analog-to-Digital Specifications and Performance Characteristics application report

#### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 12.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

#### 12.4 Trademarks

E2E is a trademark of Texas Instruments.

SPI is a trademark of Motorola.

All other trademarks are the property of their respective owners.

#### 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.6 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

www.ti.com 10-Nov-2025

#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
	, ,	.,			. ,	(4)	(5)		
ADS1018IDGSR	Active	Production	VSSOP (DGS)   10	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BTNQ
ADS1018IDGSR.A	Active	Production	VSSOP (DGS)   10	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BTNQ
ADS1018IDGSR.B	Active	Production	VSSOP (DGS)   10	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BTNQ
ADS1018IDGST	Active	Production	VSSOP (DGS)   10	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BTNQ
ADS1018IDGST.A	Active	Production	VSSOP (DGS)   10	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BTNQ
ADS1018IDGST.B	Active	Production	VSSOP (DGS)   10	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BTNQ
ADS1018IRUGR	Active	Production	X2QFN (RUG)   10	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDZ
ADS1018IRUGR.A	Active	Production	X2QFN (RUG)   10	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDZ
ADS1018IRUGR.B	Active	Production	X2QFN (RUG)   10	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDZ
ADS1018IRUGT	Active	Production	X2QFN (RUG)   10	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDZ
ADS1018IRUGT.A	Active	Production	X2QFN (RUG)   10	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDZ
ADS1018IRUGT.B	Active	Production	X2QFN (RUG)   10	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDZ
ADS1018IRUGTG4	Active	Production	X2QFN (RUG)   10	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDZ
ADS1018IRUGTG4.A	Active	Production	X2QFN (RUG)   10	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDZ
ADS1018IRUGTG4.B	Active	Production	X2QFN (RUG)   10	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDZ

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

## **PACKAGE OPTION ADDENDUM**

www.ti.com 10-Nov-2025

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF ADS1018:

Automotive: ADS1018-Q1

NOTE: Qualified Version Definitions:

Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## **PACKAGE MATERIALS INFORMATION**

www.ti.com 18-Jun-2025

## TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1018IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
ADS1018IDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
ADS1018IRUGR	X2QFN	RUG	10	3000	180.0	8.4	1.75	2.25	0.55	4.0	8.0	Q1
ADS1018IRUGT	X2QFN	RUG	10	250	180.0	8.4	1.75	2.25	0.55	4.0	8.0	Q1
ADS1018IRUGTG4	X2QFN	RUG	10	250	180.0	8.4	1.75	2.25	0.55	4.0	8.0	Q1



www.ti.com 18-Jun-2025



#### \*All dimensions are nominal

7 th difference at a free final final							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1018IDGSR	VSSOP	DGS	10	2500	367.0	367.0	38.0
ADS1018IDGST	VSSOP	DGS	10	250	213.0	191.0	35.0
ADS1018IRUGR	X2QFN	RUG	10	3000	210.0	185.0	35.0
ADS1018IRUGT	X2QFN	RUG	10	250	210.0	185.0	35.0
ADS1018IRUGTG4	X2QFN	RUG	10	250	210.0	185.0	35.0

1.5 x 2, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.





NOTES: All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
  C. QFN (Quad Flatpack No-Lead) package configuration.
  D. This package complies to JEDEC MO-288 variation X2EFD.



## RUG (R-PQFP-N10)



- NOTES: A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
  - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
  - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.





SMALL OUTLINE PACKAGE



#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-187, variation BA.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



### IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale, TI's General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025