ADC122S706 Dual 12-Bit, 500 kSPS to 1 MSPS, Simultaneous Sampling A/D Converter

Check for Samples: ADC122S706

FEATURES

- **True Simultaneous Sampling Differential Inputs**
- **Guaranteed Performance from 500 kSPS to 1 MSPS**
- **External Reference**
- **Wide Input Common-Mode Voltage Range**
- **Single or Dual High-Speed Serial Data Outputs**
- **Operating Temperature Range of −40°C to +105°C**
- **SPI™/QSPI™/MICROWIRE/DSP Compatible Serial Interface**

APPLICATIONS

- **Motor Control**
- **Power Meters/Monitors**
- **Multi-Axis Positioning Systems**
- **Instrumentation and Control Systems**
- **Data Acquisition Systems**
- **Medical Instruments**
- **Direct Sensor Interface**

KEY SPECIFICATIONS

- **Conversion Rate: 500 kSPS to 1 MSPS**
- **INL: ±1 LSB (Max)**
- **DNL: ±0.95 LSB (Max)**
- **SNR: 71 dBc (Min)**
- **THD: -72 dBc (Min)**
- **ENOB: 11.25 Bits (Min)**
- **Power Consumption at 1 MSPS**
  - **Converting, V_A = 5V, V_D = 3V: 20 mW (Typ)**
  - **Converting, V_A = 5V, V_D = 5V: 25 mW (Typ)**
  - **Power-Down: 3 µW (Typ)**

DESCRIPTION

The ADC122S706 is a dual 12-bit, 500 kSPS to 1 MSPS simultaneous sampling Analog-to-Digital (A/D) converter. The analog inputs on both channels are sampled simultaneously to preserve their relative phase information to each other. The converter is based on a successive-approximation register architecture where the differential nature of the analog inputs is maintained from the internal track-and-hold circuits throughout the A/D converter to provide excellent common-mode signal rejection. The ADC122S706 features an external reference that can be varied from 1.0V to V_A.

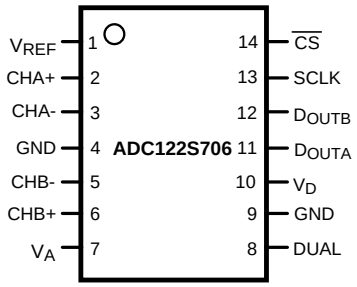
The ADC122S706 offers dual high-speed serial data outputs that are binary 2's complement and are compatible with several standards, such as SPI™, QSPI™, MICROWIRE, and many common DSP serial interfaces. Channel A's conversion result is outputted on D_{OUTA} while Channel B's conversion result is outputted on D_{OUTB}. This feature makes the ADC122S706 an excellent replacement for systems using two distinct ADCs in a simultaneous sampling application. The serial clock (SCLK) and chip select bar ($\overline{CS}$) are shared by both channels. For lower power consumption, a single serial data output mode is externally selectable.

The ADC122S706 may be operated with independent analog (V_A) and digital (V_D) supplies. V_A can range from 4.5V to 5.5V and V_D can range from 2.7V to V_A. With the ADC122S706 operating with a V_A of 5V and a V_D of 3V, the power consumption at 1 MSPS is typically 25 mW. Operating in power-down mode, the power consumption of the ADC122S706 decreases to 3 µW. The differential input, low power consumption, and small size make the ADC122S706 ideal for direct connection to sensors in motor control applications.

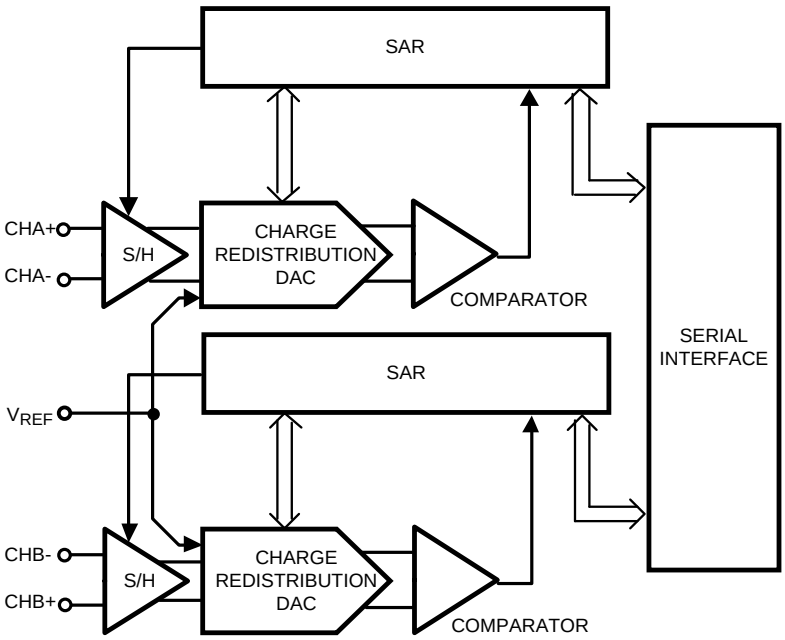
Operation is guaranteed over the industrial temperature range of −40°C to +105°C and clock rates of 8 MHz to 16 MHz. The ADC122S706 is available in a 14-lead TSSOP package.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Connection Diagram



Block Diagram



PIN DESCRIPTIONS

Pin No.	Symbol	Description
1	V_{REF}	Voltage Reference Input. A voltage reference between 1V and V_A must be applied to this input. V_{REF} must be decoupled to GND with a minimum ceramic capacitor value of 0.1 µF. A bulk capacitor value of 1.0 µF to 10 µF in parallel with the 0.1 µF is recommended for enhanced performance.
2	CHA+	Non-Inverting Input for Channel A. CHA+ is the positive analog input for the differential signal applied to Channel A.
3	CHA−	Inverting Input for Channel A. CHA− is the negative analog input for the differential signal applied to Channel A.
4	GND	Ground. GND is the ground reference point for all signals applied to the ADC122S706.
5	CHB−	Inverting Input for Channel B. CHB− is the negative analog input for the differential signal applied to Channel B.
6	CHB+	Non-Inverting Input for Channel B. CHB+ is the positive analog input for the differential signal applied to Channel B.
7	V_A	Analog Power Supply input. A voltage source between 4.5V and 5.5V must be applied to this input. V_A must be decoupled to GND with a ceramic capacitor value of 0.1 µF in parallel with a bulk capacitor value of 1.0 µF to 10 µF.
8	DUAL	Applying a logic high to this pin causes the conversion result of Channel A to be output on D_{OUTA} and the conversion result of Channel B to be output on D_{OUTB}. Grounding this pin causes the conversion result of Channel A and B to be output on D_{OUTA}, with the result of Channel A being output first. D_{OUTB} is in a high impedance state when DUAL is grounded.
9	GND	Ground. GND is the ground reference point for all signals applied to the ADC122S706.
10	V_D	Digital Power Supply input. A voltage source between 2.7V and V_A must be applied to this input. V_D must be decoupled to GND with a ceramic capacitor value of 0.1 µF in parallel with a bulk capacitor value of 1.0 µF to 10 µF.
11	D_{OUTA}	Serial Data Output for Channel A. With DUAL at a logic high state, the conversion result for Channel A is provided on D_{OUTA}. The serial data output word is comprised of 4 null bits and 12 data bits (MSB first). During a conversion, the data is outputted on the falling edges of SCLK and is generally valid on the rising edges. With DUAL at a logic low state, the conversion result of Channel A and B is outputted on D_{OUTA}.
12	D_{OUTB}	Serial Data Output for Channel B. With DUAL at a logic high state, the conversion result for Channel B is provided on D_{OUTB}. The serial data output word is comprised of 4 null bits and 12 data bits (MSB first). During a conversion, the data is outputted on the falling edges of SCLK and is generally valid on the rising edges. With DUAL at a logic low state, D_{OUTB} is in a high impedance state.
13	SCLK	Serial Clock. SCLK is used to control data transfer and serves as the conversion clock.
14	$\overline{CS}$	Chip Select Bar. $\overline{CS}$ is active low. The ADC122S706 is in Normal Mode when $\overline{CS}$ is LOW and Power-Down Mode when $\overline{CS}$ is HIGH. A conversion begins on the fall of $\overline{CS}$.

Absolute Maximum Ratings[1][2][3]

Analog Supply Voltage V_A		−0.3V to 6.5V
Digital Supply Voltage V_D		−0.3V to (V_A +0.3V) max 6.5V
Voltage on Any Pin to GND		−0.3V to (V_A +0.3V)
Input Current at Any Pin[4]		±10 mA
Package Input Current[4]		±50 mA
Power Consumption at T_A = 25°C		See[5]
ESD Susceptibility[6]	Human Body Model	2500V
	Machine Model	250V
	Charge Device Model	1000V
Junction Temperature		+150°C
Storage Temperature		−65°C to +150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the maximum Operating Ratings is not recommended.
(2) All voltages are measured with respect to GND = 0V, unless otherwise specified.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < GND or V_{IN} > V_A), the current at that pin should be limited to 10 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to five.
(5) The absolute maximum junction temperature ($T_J$max) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula $P_D MAX = (T_J max - T_A)/\theta_{JA}$. The values for maximum power dissipation listed above will be reached only when the ADC122S706 is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Such conditions should always be avoided.
(6) Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is a 220 pF capacitor discharged through 0 Ω. Charge device model simulates a pin slowly acquiring charge (such as from a device sliding down the feeder in an automated assembler) then rapidly being discharged.

Operating Ratings[1][2]

Operating Temperature Range	−40°C ≤ T_A ≤ +105°C
Supply Voltage, V_A	+4.5V to +5.5V
Supply Voltage, V_D	+2.7V to V_A
Reference Voltage, V_{REF}	1.0V to V_A
Input Common-Mode Voltage, V_{CM}	See Figure 46
Digital Input Pins Voltage Range	0 to V_D
Clock Frequency	8 MHz to 16 MHz
Differential Analog Input Voltage	$-V_{REF}$ to $+V_{REF}$

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(2) All voltages are measured with respect to GND = 0V, unless otherwise specified.

Package Thermal Resistance[1][2]

Package	θ_{JA}
14-lead TSSOP	121°C / W

(1) Soldering process must comply with TI's Reflow Temperature Profile specifications. Refer to www.ti.com/packaging.
(2) Reflow temperature profiles are different for lead-free packages.

ADC122S706 Converter Electrical Characteristics[1]

The following specifications apply for V_A = +4.5V to 5.5V, V_D = +2.7V to V_A, V_{REF} = 2.5V, f_{SCLK} = 8 to 16 MHz, DUAL = V_D, f_{IN} = 100 kHz, C_L = 25 pF, unless otherwise noted. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}**; all other limits are at T_A = 25°C.

Symbol	Parameter	Conditions		Typical	Limits	Units[2]
STATIC CONVERTER CHARACTERISTICS						
	Resolution with No Missing Codes				**12**	Bits
INL	Integral Non-Linearity			±0.5	**±1**	LSB (max)
	Integral Non-Linearity Matching			0.02		LSB
DNL	Differential Non-Linearity			±0.4	**±0.95**	LSB (max)
	Differential Non-Linearity Matching			0.02		LSB
OE	Offset Error			0.2	**±3**	LSB (max)
	Offset Error Matching			0.1		LSB
GE	Positive Gain Error			−2	**±5**	LSB (max)
	Positive Gain Error Matching			0.2		LSB
	Negative Gain Error			3	**±8**	LSB (max)
	Negative Gain Error Matching			0.2		LSB
DYNAMIC CONVERTER CHARACTERISTICS						
SINAD	Signal-to-Noise Plus Distortion Ratio	f_{IN} = 100 kHz, −0.1 dBFS		72.5	**69.5**	dBc (min)
SNR	Signal-to-Noise Ratio	f_{IN} = 100 kHz, −0.1 dBFS		73.2	**71**	dBc (min)
THD	Total Harmonic Distortion	f_{IN} = 100 kHz, −0.1 dBFS		−83	**−72**	dBc (max)
SFDR	Spurious-Free Dynamic Range	f_{IN} = 100 kHz, −0.1 dBFS		84	**72**	dBc (min)
ENOB	Effective Number of Bits	f_{IN} = 100 kHz, −0.1 dBFS		11.8	**11.25**	bits (min)
FPBW	−3 dB Full Power Bandwidth	Output at 70.7%FS with FS Input	Differential Input	26		MHz
			Single-Ended Input	22		MHz
ISOL	Channel-to-Channel Isolation	f_{IN} < 1 MHz		−90		dBc
ANALOG INPUT CHARACTERISTICS						
V_{IN}	Differential Input Range				**$-V_{REF}$**	V (min)
					$+V_{REF}$	V (max)
I_{DCL}	DC Leakage Current	$V_{IN} = V_{REF}$ or $V_{IN} = -V_{REF}$			**±1**	µA (max)
C_{INA}	Input Capacitance	In Track Mode		20		pF
		In Hold Mode		3		pF
CMRR	Common Mode Rejection Ratio	See Specification Definitions		−90		dB
V_{REF}	Reference Voltage Range				**1.0**	V (min)
					V_A	V (max)
DIGITAL INPUT CHARACTERISTICS						
V_{IH}	Input High Voltage				**2.4**	V (min)
V_{IL}	Input Low Voltage				**0.8**	V (max)
I_{IN}	Input Current[3]	V_{IN} = 0V or V_A			**±1**	µA (max)
C_{IND}	Input Capacitance			2	**4**	pF (max)
DIGITAL OUTPUT CHARACTERISTICS						
V_{OH}	Output High Voltage	I_{SOURCE} = 200 µA		V_D − 0.02	**V_D − 0.2**	V (min)
		I_{SOURCE} = 1 mA		V_D − 0.09		V
V_{OL}	Output Low Voltage	I_{SINK} = 200 µA		0.01	**0.4**	V (max)
		I_{SINK} = 1 mA		0.08		V
I_{OZH}, I_{OZL}	TRI-STATE Leakage Current	Force 0V or V_A			**±1**	µA (max)
C_{OUT}	TRI-STATE Output Capacitance	Force 0V or V_A		2	**4**	pF (max)
	Output Coding			Binary 2'S Complement		

(1) Data sheet min/max specification limits are guaranteed by design, test, or statistical analysis.
(2) Tested limits are guaranteed to TI's AOQL (Average Outgoing Quality Level).
(3) The digital input pin, DUAL, has a leakage current of ±5 µA.

ADC122S706 Converter Electrical Characteristics[1] (continued)

The following specifications apply for V_A = +4.5V to 5.5V, V_D = +2.7V to V_A, V_{REF} = 2.5V, f_{SCLK} = 8 to 16 MHz, DUAL = V_D, f_{IN} = 100 kHz, C_L = 25 pF, unless otherwise noted. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}**; all other limits are at T_A = 25°C.

Symbol	Parameter	Conditions	Typical	Limits	Units[2]
POWER SUPPLY CHARACTERISTICS					
V_A	Analog Supply Voltage			**4.5**	V (min)
				5.5	V (max)
V_D	Digital Supply Voltage			**2.7**	V (min)
				V_A	V (max)
I_{VA} (Conv)	Analog Supply Current, Continuously Converting (Dual Data Output Mode)	f_{SCLK} = 16 MHz, f_S = 1 MSPS, f_{IN} = 100 kHz, V_A = 5V, DUAL = V_D	3.3	**4.2**	mA (max)
	Analog Supply Current, Continuously Converting (Single Data Output Mode)	f_{SCLK} = 16 MHz, f_S = 500 kSPS, f_{IN} = 100 kHz, V_A = 5V, DUAL = 0V	1.8	**2.9**	mA (max)
I_{VD} (Conv)	Digital Supply Current, Continuously Converting (Dual Data Output Mode)	f_{SCLK} = 16 MHz, f_S = 1 MSPS, f_{IN} = 100 kHz, V_D = 5V, DUAL = 5V	1.7	**2.0**	mA (max)
		f_{SCLK} = 16 MHz, f_S = 1 MSPS, f_{IN} = 100 kHz, V_D = 3V, DUAL = 3V	1.0	**1.3**	mA (max)
	Digital Supply Current, Continuously Converting (Single Data Output Mode)	f_{SCLK} = 16 MHz, f_S = 500 kSPS, f_{IN} = 100 kHz, V_D = 5V, DUAL = 0V	0.9	**1.2**	mA (max)
		f_{SCLK} = 16 MHz, f_S = 500 kSPS, f_{IN} = 100 kHz, V_D = 3V, DUAL = 0V	0.6	**0.7**	mA (max)
I_{VREF} (Conv)	Reference Current, Continuously Converting (Dual Data Output Mode)	f_{SCLK} = 16 MHz, f_S = 1 MSPS, V_{REF} = 2.5V, DUAL = V_D	90	**105**	µA (max)
	Reference Current, Continuously Converting (Single Data Output Mode)	f_{SCLK} = 16 MHz, f_S = 500 kSPS, V_{REF} = 2.5V, DUAL = 0V	45	**60**	µA (max)
I_{VA} (PD)	Analog Supply Current, Power Down Mode ($\overline{CS}$ high)	f_{SCLK} = 16 MHz, V_A = 5.0V	10		µA
		f_{SCLK} = 0, V_A = 5.0V[4]	0.5	**1**	µA (max)
I_{VD} (PD)	Digital Supply Current, Power Down Mode ($\overline{CS}$ high)	f_{SCLK} = 16 MHz, V_D = 5.0V	10		µA
		f_{SCLK} = 0[4]	0.1	**0.2**	µA (max)
I_{VREF} (PD)	Reference Current, Power Down Mode ($\overline{CS}$ high)	f_{SCLK} = 16 MHz	0.05		µA
		f_{SCLK} = 0[4]	0.05	**0.1**	µA (max)
PWR (Conv)	Power Consumption, Continuously Converting (Dual Data Output Mode)	f_{SCLK} = 16 MHz, f_S = 1 MSPS, f_{IN} = 100 kHz, V_A = V_D = 5V, V_{REF} = 2.5V, DUAL = V_D	25	**31.3**	mW (max)
		f_{SCLK} = 16 MHz, f_S = 1 MSPS, f_{IN} = 100 kHz, V_A = 5V, V_D = 3V, V_{REF} = 2.5V, DUAL = V_D	20	**25.2**	mW (max)
	Power Consumption, Continuously Converting (Single Data Output Mode)	f_{SCLK} = 16 MHz, f_S = 500 kSPS, f_{IN} = 100 kHz, V_A = V_D = 5V, V_{REF} = 2.5V, DUAL = 0V	13.6	**20.6**	mW (max)
		f_{SCLK} = 16 MHz, f_S = 500 kSPS, f_{IN} = 100 kHz, V_A = 5V, V_D = 3V, V_{REF} = 2.5V, DUAL = 0V	10.9	**16.8**	mW (max)
PWR (PD)	Power Consumption, Power Down Mode ($\overline{CS}$ high)	f_{SCLK} = 16 MHz, V_A = V_D = 5.0V, V_{REF} = 2.5V	100		µW
		f_{SCLK} = 0, V_A = V_D = 5.0V, V_{REF} = 2.5V	3.1	**6.5**	µW (max)
PSRR	Power Supply Rejection Ratio	See the Specification Definitions	−85		dB
AC ELECTRICAL CHARACTERISTICS					
f_{SCLK}	Maximum Clock Frequency		20	**16**	MHz (min)
f_{SCLK}	Minimum Clock Frequency		0.8	**8**	MHz (max)
f_S	Maximum Sample Rate[5]		1.25	**1**	MSPS (min)
t_{ACQ}	Track/Hold Acquisition Time			**3**	SCLK cycles
t_{CONV}	Conversion Time			**12**	SCLK cycles
t_{AD}	Aperture Delay		6		ns

(4) Data sheet min/max specification limits are guaranteed by design, test, or statistical analysis.
(5) While the maximum sample rate is f_{SCLK}/16, the actual sample rate may be lower than this by having the $\overline{CS}$ rate slower than f_{SCLK}/16.

ADC122S706 Timing Specifications(1)

The following specifications apply for V_A = +4.5V to 5.5V, V_D = +2.7V to V_A, V_{REF} = 2.5V, f_{SCLK} = 8 MHz to 16 MHz, C_L = 25 pF, unless otherwise noted. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}**: all other limits T_A = 25°C.

Symbol	Parameter	Conditions	Typical	Limits	Units
t_{CSSU}	$\overline{CS}$ Setup Time prior to an SCLK rising edge	V_D = +2.7V to 3.6V	5	**11**	ns (min)
			1/ f_{SCLK}	**1/ f_{SCLK} - 3**	ns (max)
		V_D = +4.5V to 5.5V	4	**7**	ns (min)
			1/ f_{SCLK}	**1/ f_{SCLK} - 3**	ns (max)
t_{EN}	D_{OUT} Enable Time after the falling edge of $\overline{CS}$	V_D = +2.7V to 3.6V	22	**39**	ns (max)
		V_D = +4.5V to 5.5V	9	**20**	ns (max)
t_{DH}	D_{OUT} Hold time after an SCLK Falling edge		9	**6**	ns (min)
t_{DA}	D_{OUT} Access time after an SCLK Falling edge	V_D = +2.7V to 3.6V	24	**39**	ns (max)
		V_D = +4.5V to 5.5V	20	**26**	ns (max)
t_{DIS}	D_{OUT} Disable Time after the rising edge of $\overline{CS}$(2)		10	**20**	ns (max)
t_{CH}	SCLK High Time			**25**	ns (min)
t_{CL}	SCLK Low Time			**25**	ns (min)
t_r	D_{OUT} Rise Time		7		ns
t_f	D_{OUT}Fall Time		7		ns

(1) Data sheet min/max specification limits are guaranteed by design, test, or statistical analysis.
(2) t_{DIS} is the time for D_{OUT} to change 10%.

Timing Diagrams

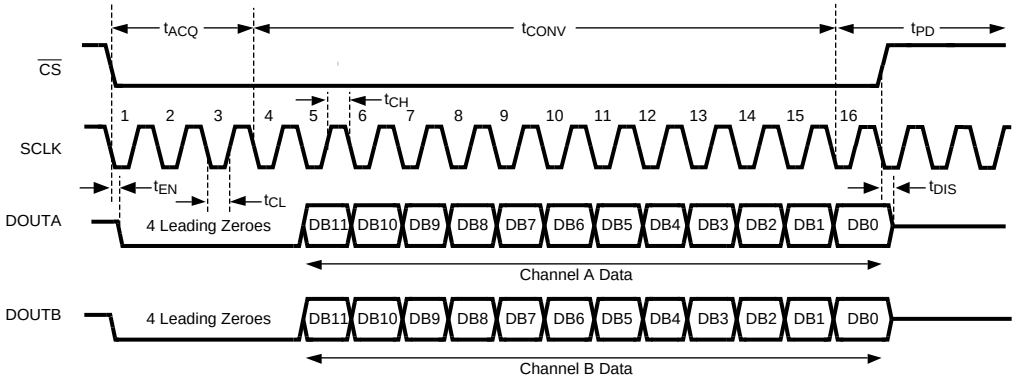


Figure 1. ADC122S706 Single Conversion Timing Diagram (DUAL Data Output Mode)

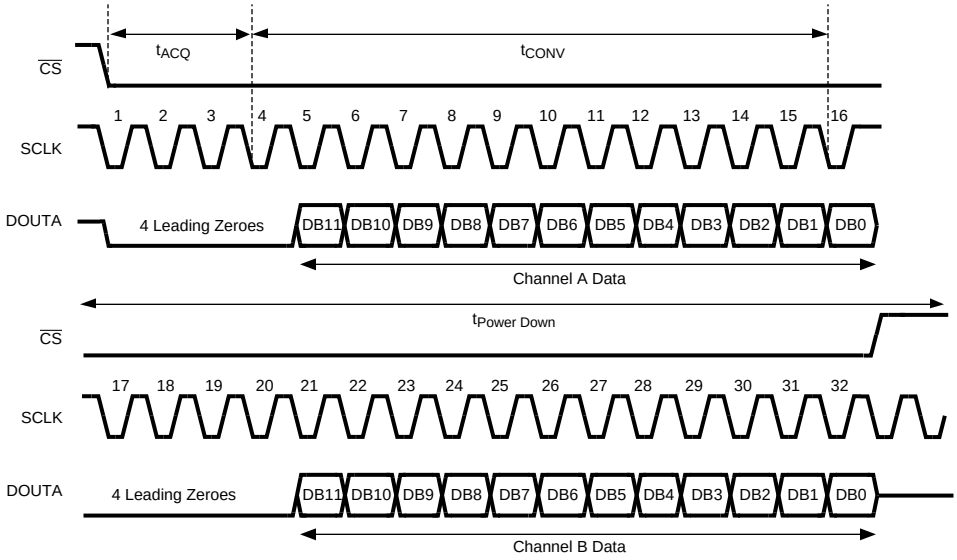


Figure 2. ADC122S706 Single Conversion Timing Diagram (SINGLE Data Output Mode)

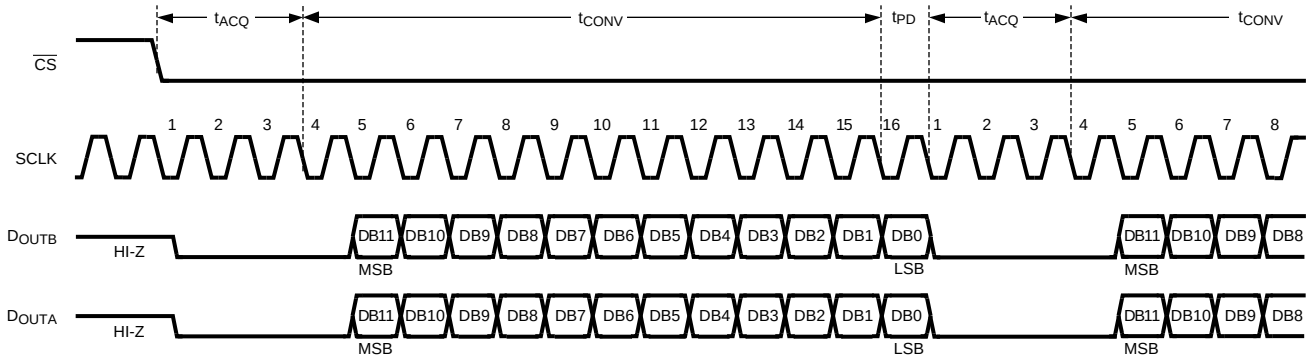


Figure 3. ADC122S706 Continuous Conversion Timing Diagram (DUAL Data Output Mode)

Figure 4. D_{OUT} Rise and Fall Times

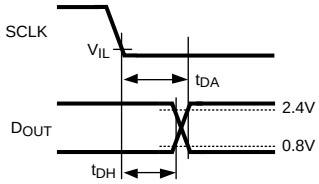


Figure 5. D_{OUT} Hold and Access Times

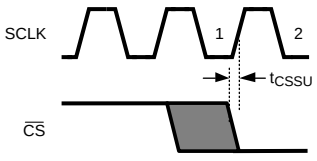


Figure 6. Valid $\overline{CS}$ Assertion Times

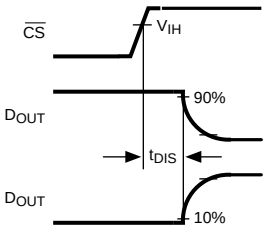


Figure 7. Voltage Waveform for t_{DIS}

Specification Definitions

APERTURE DELAY is the time between the fourth falling edge of SCLK and the time when the input signal is acquired or held for conversion.

COMMON MODE REJECTION RATIO (CMRR) is a measure of how well in-phase signals common to both input pins are rejected.

To calculate CMRR, the change in output offset is measured while the common mode input voltage is changed from 2V to 3V.

$$\text{CMRR} = 20 \text{ LOG } (\Delta \text{ Common Input} / \Delta \text{ Output Offset}) \quad (1)$$

CONVERSION TIME is the time required, after the input voltage is acquired, for the ADC to convert the input voltage to a digital word.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

DUTY CYCLE is the ratio of the time that a repetitive digital waveform is high to the total time of one period. The specification here refers to the SCLK.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as (SINAD − 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from negative full scale (½ LSB below the first code transition) through positive full scale (½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

MISSING CODES are those output codes that will never appear at the ADC outputs. The ADC122S706 is guaranteed not to have any missing codes.

NEGATIVE FULL-SCALE ERROR is the difference between the differential input voltage at which the output code transitions from negative full scale to the next code and $-V_{REF}$ + 0.5 LSB.

NEGATIVE GAIN ERROR is the difference between the negative full-scale error and the offset error.

OFFSET ERROR is the difference between the differential input voltage at which the output code transitions from code 000h to 001h and 1/2 LSB.

POSITIVE FULL-SCALE ERROR is the difference between the differential input voltage at which the output code transitions to positive full scale and V_{REF} minus 1.5 LSB.

POSITIVE GAIN ERROR is the difference between the positive full-scale error and the offset error.

POWER SUPPLY REJECTION RATIO (PSRR) is a measure of how well a change in supply voltage is rejected. PSRR is calculated from the ratio of the change in offset error for a given change in supply voltage, expressed in dB. For the ADC122S706, V_A is changed from 4.5V to 5.5V.

$$\text{PSRR} = 20 \text{ LOG } (\Delta\text{Offset} / \Delta V_A) \quad (2)$$

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or d.c.

SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD) Is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the desired signal amplitude to the amplitude of the peak spurious spectral component, where a spurious spectral component is any signal present in the output spectrum that is not present at the input and may or may not be a harmonic.

TOTAL HARMONIC DISTORTION (THD) is the ratio of the rms total of the first five harmonic components at the output to the rms level of the input signal frequency as seen at the output, expressed in dB. THD is calculated as

$$THD = 20 \cdot \log_{10} \sqrt{\frac{A_{f2}^2 + \cdots + A_{f6}^2}{A_{f1}^2}} \quad (3)$$

where A_{f1} is the RMS power of the input frequency at the output and A_{f2} through A_{f6} are the RMS power in the first 5 harmonic frequencies.

THROUGHPUT TIME is the minimum time required between the start of two successive conversion.

Typical Performance Characteristics

$V_A = V_D = 5.0V$, $V_{REF} = 2.5V$, $T_A = +25°C$, $f_{SAMPLE} = 1$ MSPS, $f_{SCLK} = 16$ MHz, DUAL = V_D, $f_{IN} = 100$ kHz unless otherwise stated.

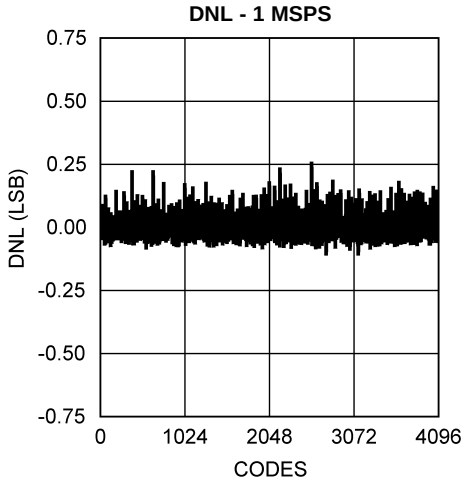


Figure 8.

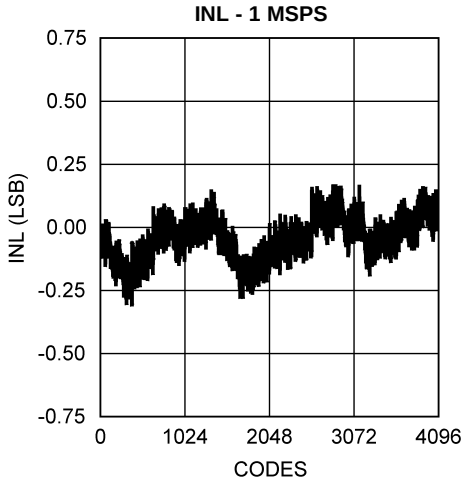


Figure 9.

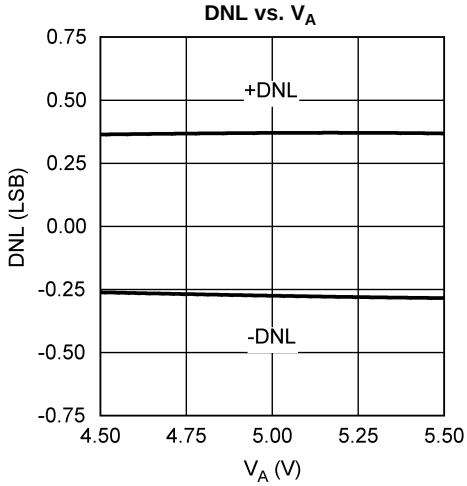


Figure 10.

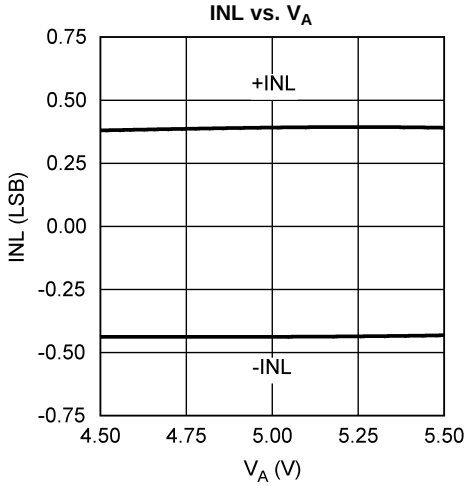


Figure 11.

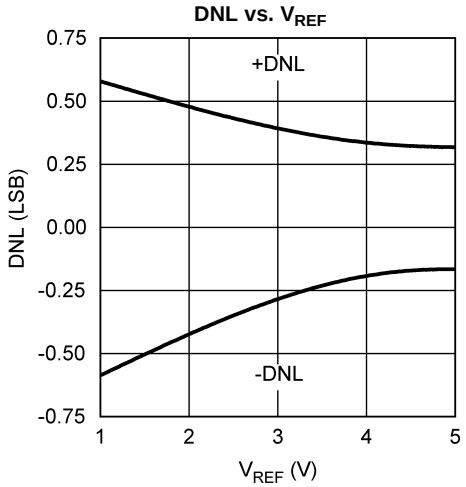


Figure 12.

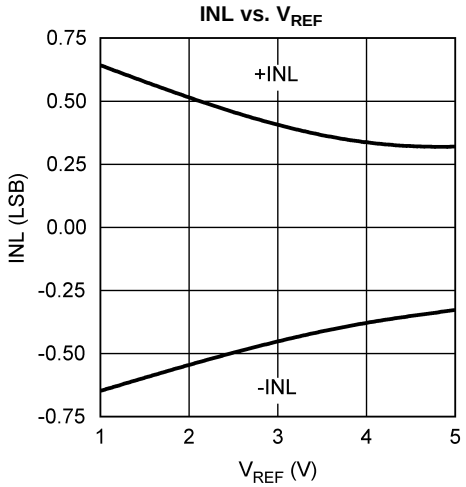


Figure 13.

Typical Performance Characteristics (continued)

V_A = V_D = 5.0V, V_{REF} = 2.5V, T_A = +25°C, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 16 MHz, DUAL = V_D, f_{IN} = 100 kHz unless otherwise stated.

DNL vs. SCLK FREQUENCY

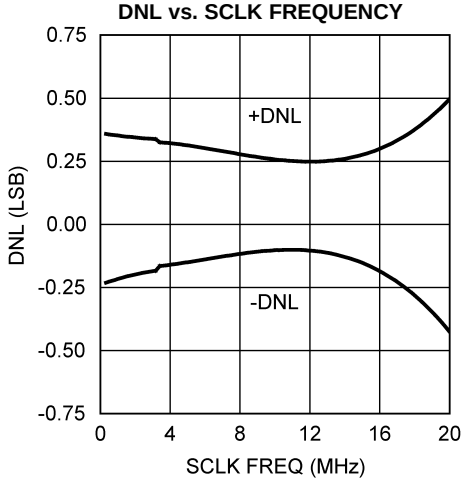


Figure 14.

INL vs. SCLK FREQUENCY

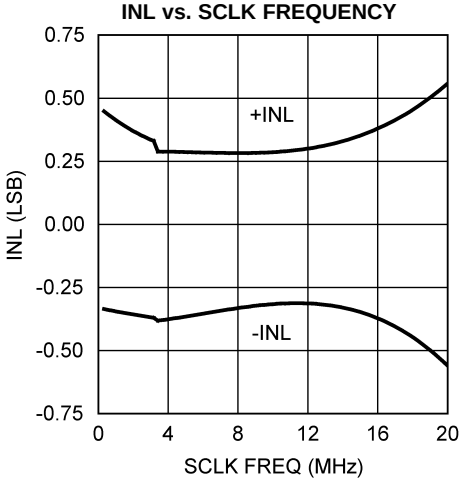


Figure 15.

DNL vs. TEMPERATURE

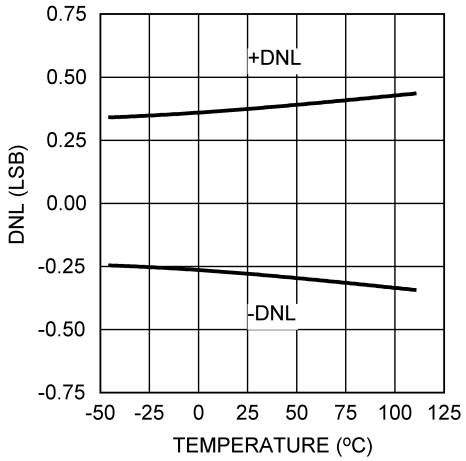


Figure 16.

INL vs. TEMPERATURE

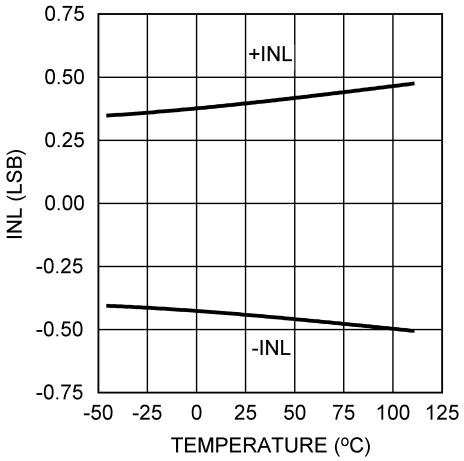


Figure 17.

SINAD vs. V_A

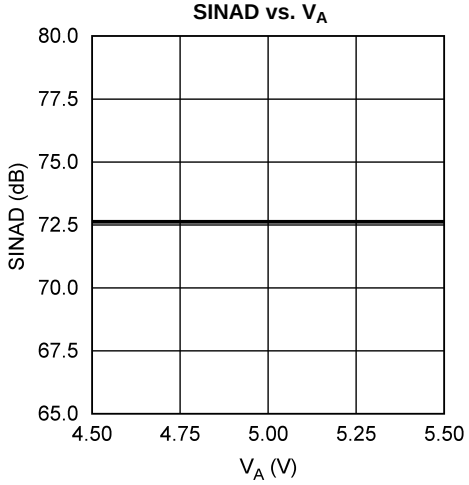


Figure 18.

THD vs. V_A

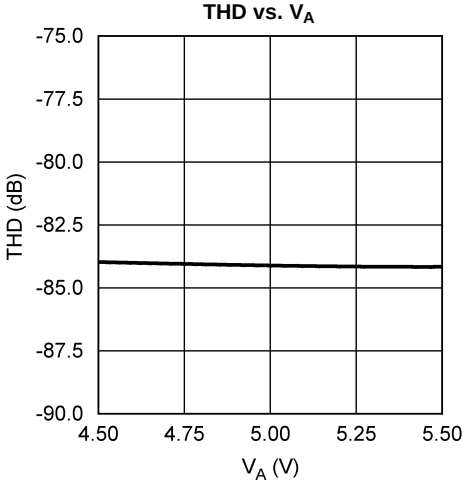


Figure 19.

Typical Performance Characteristics (continued)

$V_A = V_D = 5.0V$, $V_{REF} = 2.5V$, $T_A = +25°C$, $f_{SAMPLE} = 1$ MSPS, $f_{SCLK} = 16$ MHz, DUAL = V_D, $f_{IN} = 100$ kHz unless otherwise stated.

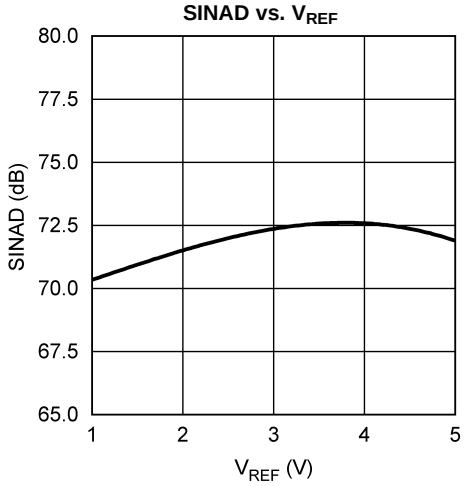


Figure 20.

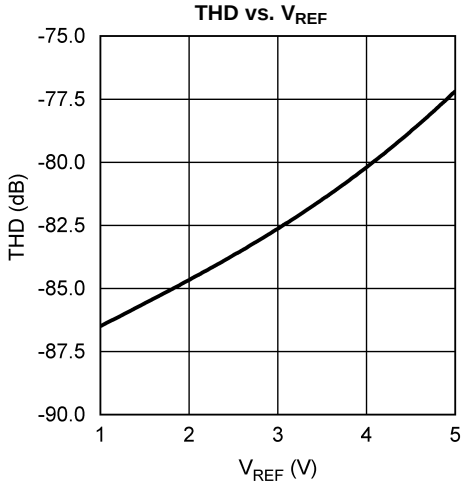


Figure 21.

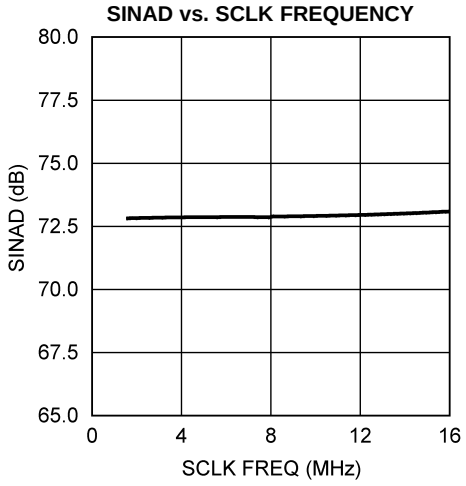


Figure 22.

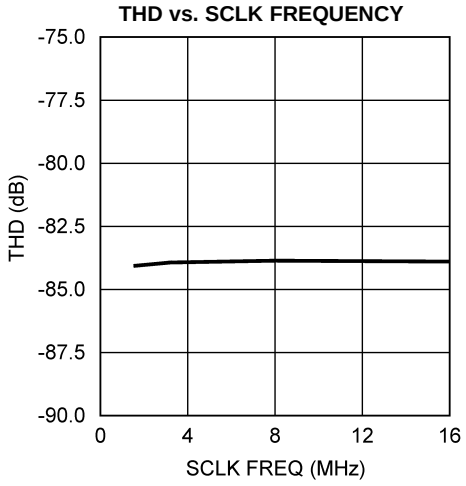


Figure 23.

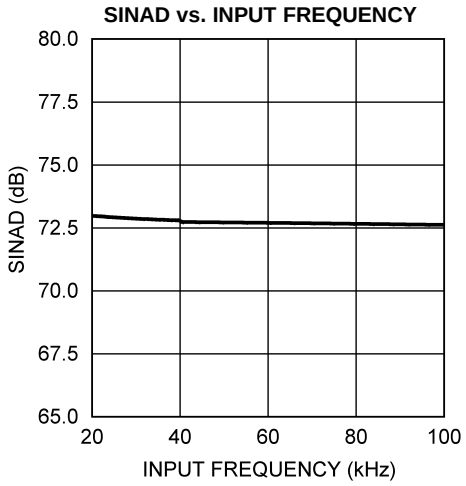


Figure 24.

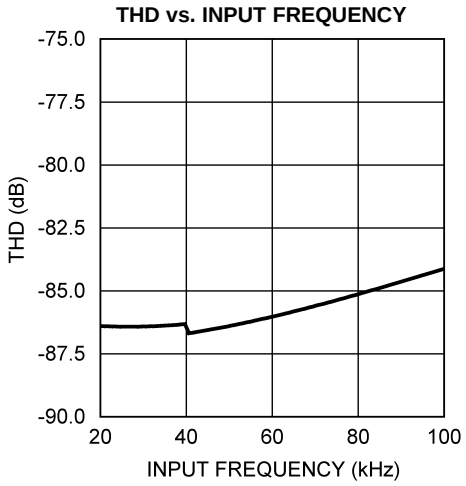


Figure 25.

Typical Performance Characteristics (continued)

V_A = V_D = 5.0V, V_{REF} = 2.5V, T_A = +25°C, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 16 MHz, DUAL = V_D, f_{IN} = 100 kHz unless otherwise stated.

SINAD vs. TEMPERATURE

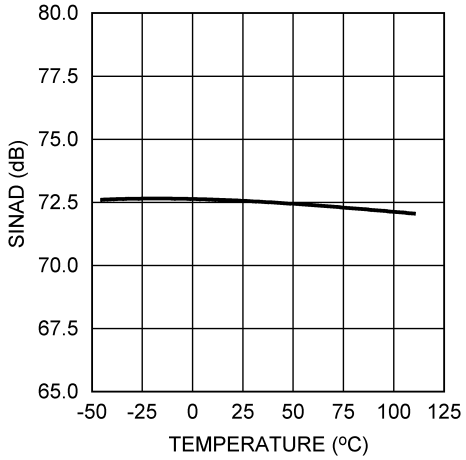


Figure 26.

THD vs. TEMPERATURE

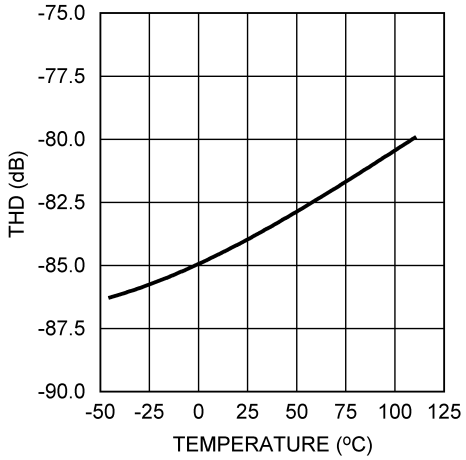


Figure 27.

V_A CURRENT vs. V_A

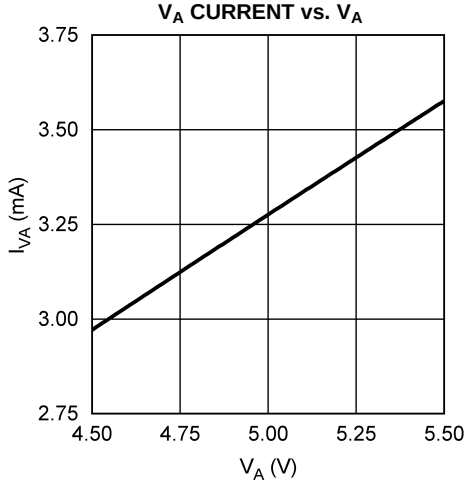


Figure 28.

V_A CURRENT vs. SCLK FREQ

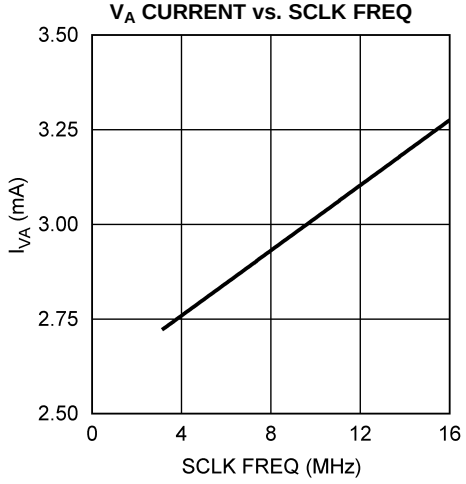


Figure 29.

V_A CURRENT vs. TEMPERATURE

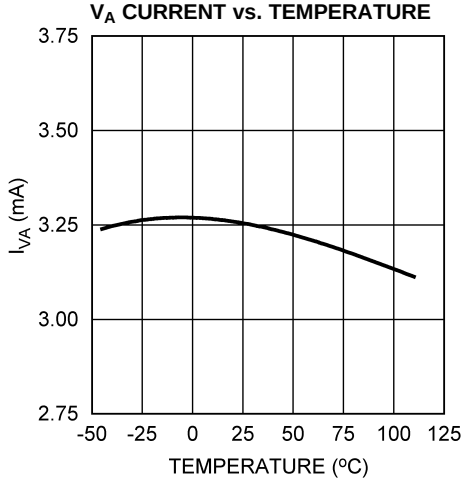


Figure 30.

V_{REF} CURRENT vs. SCLK FREQ

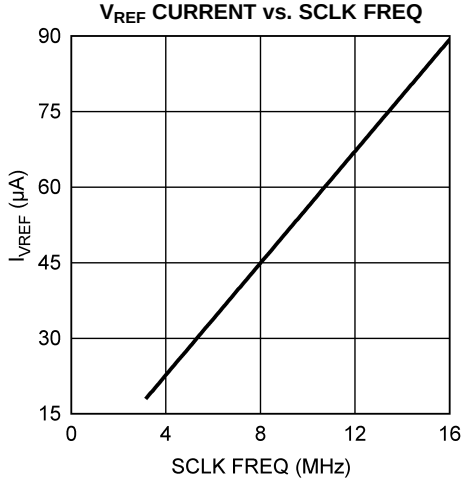


Figure 31.

Typical Performance Characteristics (continued)

V_A = V_D = 5.0V, V_{REF} = 2.5V, T_A = +25°C, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 16 MHz, DUAL = V_D, f_{IN} = 100 kHz unless otherwise stated.

V_{REF} CURRENT vs. TEMP

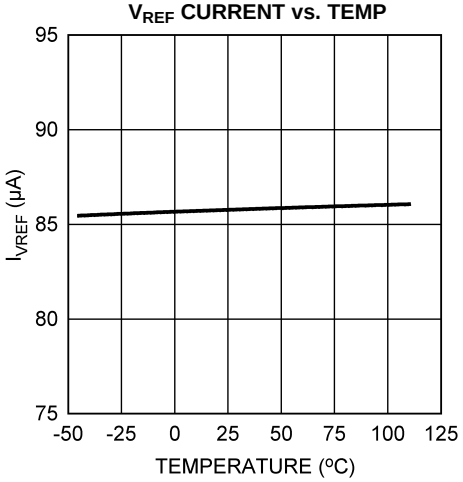


Figure 32.

V_D CURRENT vs. SCLK FREQ

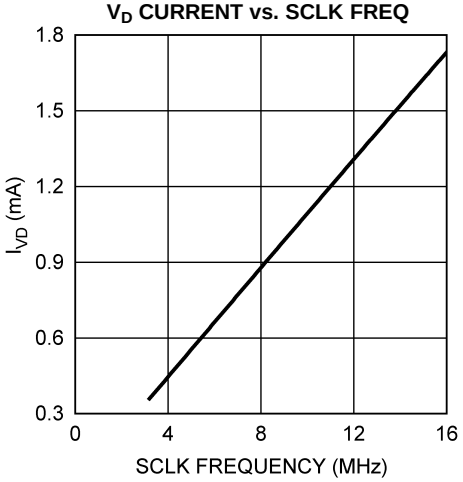


Figure 33.

V_D CURRENT vs. TEMP

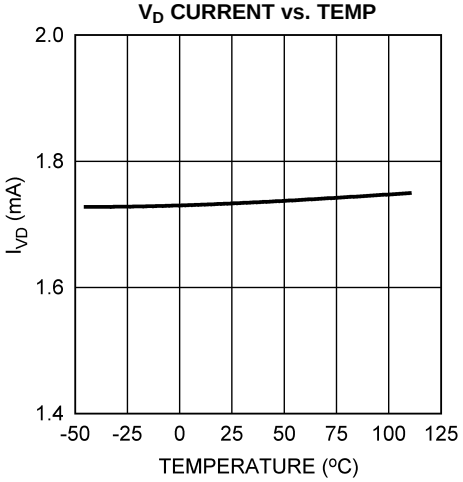


Figure 34.

V_A CURRENT vs. V_A (SINGLE D_{OUT})

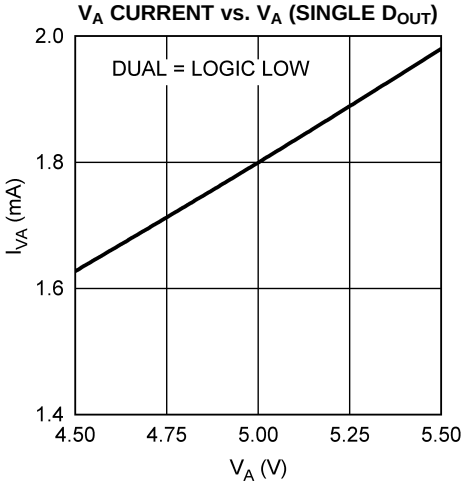


Figure 35.

V_A CURRENT vs. SCLK FREQ (SINGLE D_{OUT})

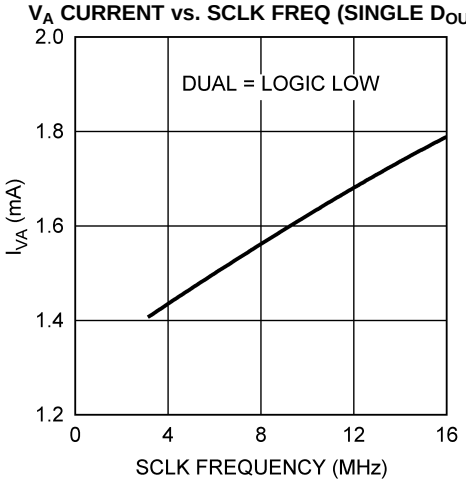


Figure 36.

V_A CURRENT vs. TEMP (SINGLE D_{OUT})

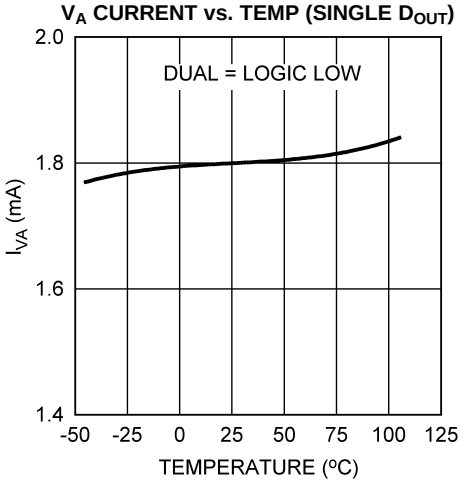


Figure 37.

Typical Performance Characteristics (continued)

$V_A = V_D = 5.0V$, $V_{REF} = 2.5V$, $T_A = +25°C$, $f_{SAMPLE} = 1$ MSPS, $f_{SCLK} = 16$ MHz, DUAL = V_D, $f_{IN} = 100$ kHz unless otherwise stated.

V_{REF} CURRENT vs. SCLK (SINGLE D_{OUT})

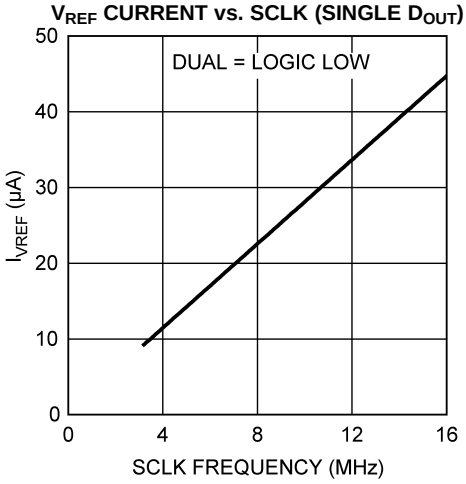


Figure 38.

V_{REF} CURRENT vs. TEMP (SINGLE D_{OUT})

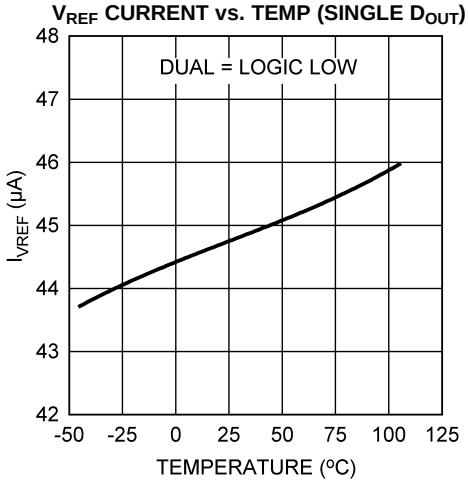


Figure 39.

V_D CURRENT vs. SCLK (SINGLE D_{OUT})

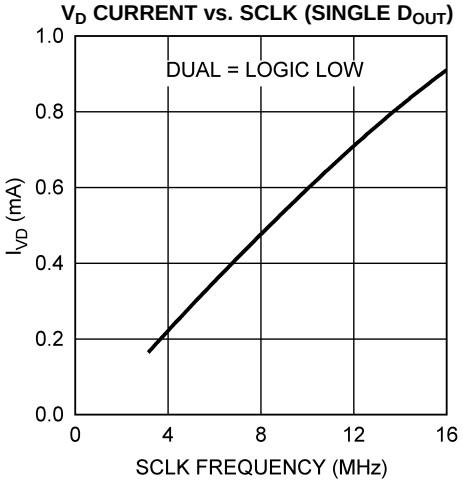


Figure 40.

V_D CURRENT vs. TEMP (SINGLE D_{OUT})

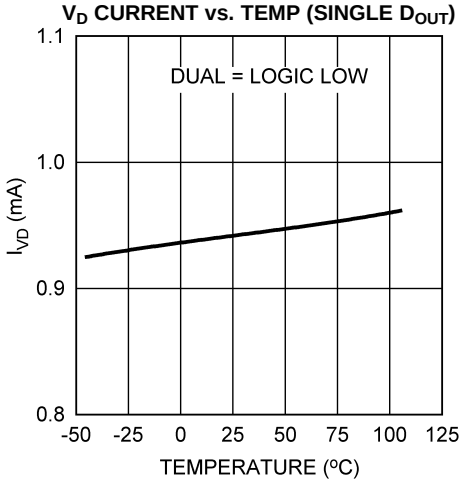


Figure 41.

CMRR vs. CM RIPPLE FREQ

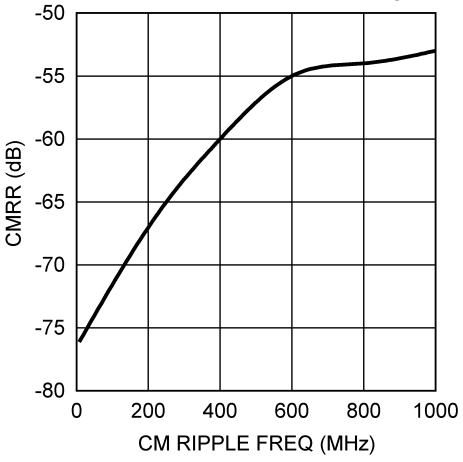


Figure 42.

SPECTRAL RESPONSE - 1 MSPS

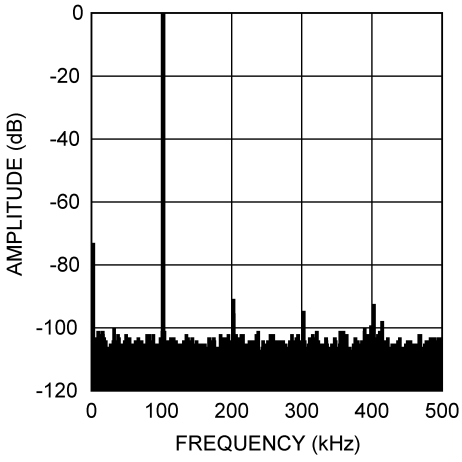


Figure 43.

FUNCTIONAL DESCRIPTION

The ADC122S706 is a dual 12-bit, simultaneous sampling Analog-to-Digital (A/D) converter. The converter is based on a successive-approximation register (SAR) architecture where the differential nature of the analog inputs is maintained from the internal track-and-hold circuits throughout the A/D converter. The analog inputs on both channels are sampled simultaneously to preserve their relative phase information to each other. The architecture and process allow the ADC122S706 to acquire and convert dual analog signals at sample rates up to 1 MSPS while consuming very little power.

The ADC122S706 operates from independent analog and digital supplies. The analog supply (V_A) can range from 4.5V to 5.5V and the digital supply (V_D) can range from 2.7V to V_A. The ADC122S706 utilizes an external reference. The external reference can be any voltage between 1V and V_A. The value of the reference voltage determines the range of the analog input, while the reference input current depends upon the conversion rate.

Analog inputs are presented at the inputs of Channel A and Channel B. Upon initiation of a conversion, the differential input at these pins is sampled on the internal capacitor array. The inputs are disconnected from the internal circuitry while a conversion is in progress.

The ADC122S706 requires an external clock. The duty cycle of the clock is essentially unimportant, provided the minimum clock high and low times are met. The minimum clock frequency is set by internal capacitor leakage. Each conversion requires 16 SCLK cycles to complete. If less than 12 bits of conversion data are required, $\overline{CS}$ can be brought high at any point during the conversion.

The ADC122S706 offers dual high-speed serial data outputs that are binary 2's complement and are compatible with several standards, such as SPI™, QSPI™, MICROWIRE, and many common DSP serial interfaces. Channel A's conversion result is outputted on D_{OUTA} while Channel B's conversion result is outputted on D_{OUTB}. This feature makes the ADC122S706 an excellent replacement for systems using two distinct ADCs in a simultaneous sampling application. The serial clock (SCLK) and chip select bar ($\overline{CS}$) are shared by both channels. The digital conversion of channel A and B is clocked out by the SCLK input and is provided serially, most significant bit first, at D_{OUTA} and D_{OUTB}, respectively. The digital data that is provided at D_{OUTA} and D_{OUTB} is that of the conversion currently in progress. With $\overline{CS}$ held low after the conversion is complete, the ADC122S706 continuously converts the analog inputs. For lower power consumption, a single serial data output mode is externally selectable. This feature makes the ADC122S706 an excellent replacement for two independent ADCs that are part of a daisy chain configuration.

REFERENCE INPUT

The externally supplied reference voltage sets the analog input range. The ADC122S706 will operate with a reference voltage in the range of 1V to V_A.

Operation with a reference voltage below 1V is also possible with slightly diminished performance. As the reference voltage (V_{REF}) is reduced, the range of acceptable analog input voltages is reduced. Assuming a proper common-mode input voltage, the differential peak-to-peak input range is limited to twice V_{REF}. See Input Common Mode Voltage for more details. Reducing the value of V_{REF} also reduces the size of the least significant bit (LSB). The size of one LSB is equal to twice the reference voltage divided by 4096. When the LSB size goes below the noise floor of the ADC122S706, the noise will span an increasing number of codes and overall performance will suffer. For example, dynamic signals will have their SNR degrade, while D.C. measurements will have their code uncertainty increase. Since the noise is Gaussian in nature, the effects of this noise can be reduced by averaging the results of a number of consecutive conversions.

Additionally, since offset and gain errors are specified in LSB, any offset and/or gain errors inherent in the A/D converter will increase in terms of LSB size as the reference voltage is reduced.

The reference input and the analog inputs are connected to the capacitor array through a switch matrix when the input is sampled. Hence, the current requirements at the reference and at the analog inputs are a series of transient spikes that occur at a frequency dependent on the operating sample rate of the ADC122S706.

The reference current changes only slightly with temperature. See Figure 38 and Figure 39 in Typical Performance Characteristics for additional details.

ANALOG SIGNAL INPUTS

The ADC122S706 has dual differential inputs where the effective input voltage that is digitized is CHA+ minus CHA− (DIFFINA) and CHB+ minus CHB− (DIFFINB). As is the case with all differential input A/D converters, operation with a fully differential input signal or voltage will provide better performance than with a single-ended input. However, the ADC122S706 can be presented with a single-ended input.

The current required to recharge the input sampling capacitor will cause voltage spikes at the + and − inputs. Do not try to filter out these noise spikes. Rather, ensure that the transient settles out during the acquisition period (three SCLK cycles after the fall of $\overline{CS}$).

Differential Input Operation

With a fully differential input voltage or signal, a positive full scale output code (0111 1111 1111b or 7FFh) will be obtained when DIFFINA or DIFFINB is greater than or equal to V_{REF} − 1.5 LSB. A negative full scale code (1000 0000 0000b or 800h) will be obtained when DIFFINA or DIFFINB is greater than or equal to $-V_{REF}$ + 0.5 LSB. This ignores gain, offset and linearity errors, which will affect the exact differential input voltage that will determine any given output code. Figure 44 shows the ADC122S706 being driven by a full-scale differential source.

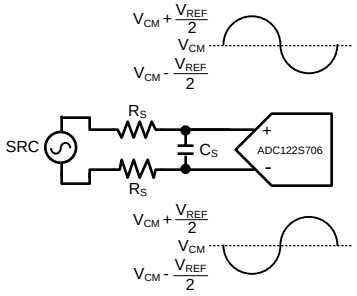


Figure 44. Differential Input

Single-Ended Input Operation

For single-ended operation, the non-inverting inputs of the ADC122S706 can be driven with a signal that has a maximum to minimum value range that is equal to or less than twice the reference voltage. The inverting inputs should be biased at a stable voltage that is halfway between these maximum and minimum values. In order to utilize the entire dynamic range of the ADC122S706, the reference voltage is limited at V_A / 2. This allows the non-inverting inputs the maximum swing range of ground to V_A. Figure 45 shows the ADC122S706 being driven by a full-scale single-ended source.

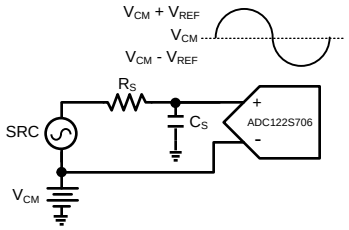


Figure 45. Single-Ended Input

Since the design of the ADC122S706 is optimized for a differential input, the performance degrades slightly when driven with a single-ended input. Linearity characteristics such as INL and DNL typically degrade by 0.1 LSB and dynamic characteristics such as SINAD typically degrades by 2 dB. Note that single-ended operation should only be used if the performance degradation (compared with differential operation) is acceptable.

Input Common Mode Voltage

The allowable input common mode voltage (V_{CM}) range depends upon the supply and reference voltages used for the ADC122S706. The ranges of V_{CM} are depicted in Figure 46 and Figure 47. Equations for calculating the minimum and maximum common mode voltages for differential and single-ended operation are shown in Table 1.

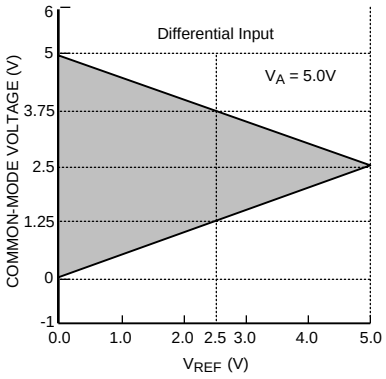


Figure 46. V_{CM} range for Differential Input operation

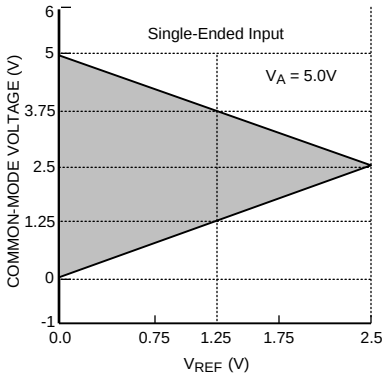


Figure 47. V_{CM} range for single-ended operation

Table 1. Allowable V_{CM} Range

Input Signal	Minimum V_{CM}	Maximum V_{CM}
Differential	V_{REF} / 2	$V_A - V_{REF}$ / 2
Single-Ended	V_{REF}	$V_A - V_{REF}$

SERIAL DIGITAL INTERFACE

The ADC122S706 communicates via a synchronous serial interface as shown in Timing Diagrams. $\overline{CS}$, chip select, initiates conversions and frames the serial data transfers. SCLK (serial clock) controls both the conversion process and the timing of the serial data. D_{OUTA} and D_{OUTB} are the serial data output pins, where the conversion results of Channel A and Channel B are sent as serial data streams, MSB first.

A serial frame is initiated on the falling edge of $\overline{CS}$ and ends on the rising edge of $\overline{CS}$. The ADC122S706's data output pins are in a high impedance state when $\overline{CS}$ is high and are active when $\overline{CS}$ is low; thus $\overline{CS}$ acts as an output enable. A timing diagram for a single conversion is shown in Figure 1.

During the first three cycles of SCLK, the ADC122S706 is in acquisition mode (t_{ACQ}), tracking the input voltage. For the next twelve SCLK cycles (t_{CONV}), the conversion is accomplished and the data is clocked out. SCLK falling edges one through four clock out leading zeros while falling edges five through sixteen clock out the conversion result, MSB first. If there is more than one conversion in a frame (continuous conversion mode), the ADC122S706 will re-enter acquisition mode on the falling edge of SCLK after the N*16th rising edge of SCLK and re-enter the conversion mode on the N*16+4th falling edge of SCLK as shown in Figure 3. "N" is an integer value.

The ADC122S706 can enter acquisition mode under three different conditions. The first condition involves $\overline{CS}$ going low (asserted) with SCLK high. In this case, the ADC122S706 enters acquisition mode on the first falling edge of SCLK after $\overline{CS}$ is asserted. In the second condition, $\overline{CS}$ goes low with SCLK low. Under this condition, the ADC122S706 automatically enters acquisition mode and the falling edge of $\overline{CS}$ is seen as the first falling edge of SCLK. In the third condition, $\overline{CS}$ and SCLK go low simultaneously and the ADC122S706 enters acquisition mode. While there is no timing restriction with respect to the falling edges of $\overline{CS}$ and the falling edge of SCLK, see Figure 6 for setup and hold time requirements for the falling edge of $\overline{CS}$ with respect to the rising edge of SCLK.

$\overline{CS}$ Input

The $\overline{CS}$ (chip select bar) is an active low input that is TTL and CMOS compatible. The ADC122S706 is in conversion mode when $\overline{CS}$ is low and power-down mode when $\overline{CS}$ is high. As a result, $\overline{CS}$ frames the conversion window. The falling edge of $\overline{CS}$ marks the beginning of a conversion and the rising edge of $\overline{CS}$ marks the end of a conversion window. Multiple conversions can occur within a given conversion frame with each conversion requiring sixteen SCLK cycles. This is referred to as continuous conversion mode and is shown in Figure 3 of Timing Diagrams.

Proper operation requires that the fall of $\overline{CS}$ not occur simultaneously with a rising edge of SCLK. If the fall of $\overline{CS}$ occurs during the rising edge of SCLK, the data might be clocked out one bit early. Whether or not the data is clocked out early depends upon how close the $\overline{CS}$ transition is to the SCLK transition, the device temperature, and characteristics of the individual device. To ensure that the MSB is always clocked out at a given time (the 5th falling edge of SCLK), it is essential that the fall of $\overline{CS}$ always meet the timing requirement specified in Timing Specifications.

SCLK Input

The SCLK (serial clock) serves two purposes in the ADC122S706. It is used by the ADC as the conversion clock and it is used as the serial clock to output the conversion results. This SCLK input is CMOS compatible. Internal settling time requirements limit the maximum clock frequency while internal capacitor leakage limits the minimum clock frequency. The ADC122S706 offers guaranteed performance with the clock rates indicated in the electrical table.

Data Output(s)

The ADC122S706 enables system designers two options for receiving converted data from the ADC122S706. Data can be received from separate data output pins (D_{OUTA} and D_{OUTB}) or from a single data output line. These options are controlled by the digital input pin DUAL. With the DUAL pin set to a logic high level, the dual high-speed serial outputs are enabled. Channel A's conversion result is outputted on D_{OUTA} while Channel B's conversion result is outputted on D_{OUTB}. With the DUAL pin set to a logic low level, the conversion result of Channel A and Channel B is outputted on D_{OUTA}, with the result of Channel A being outputted before the result of Channel B. The D_{OUTB} pin is in a high impedance state during this condition. See Figure 1 and Figure 2 in Timing Diagrams for more details on DUAL and SINGLE DOUT mode.

The output data format of the ADC122S706 is two's complement, as shown in Table 2. This table indicates the ideal output code for the given input voltage and does not include the effects of offset, gain error, linearity errors, or noise. Each data bit is output on the falling edge of SCLK.

Table 2. Ideal Output Code vs. Input Voltage

Analog Input, (+IN) − (−IN)	2's Complement Binary Output	2's Comp. Hex Code	2's Comp. Dec Code
V_{REF} − 1.5 LSB	0111 1111 1111	7FF	2047
+ 0.5 LSB	0000 0000 0001	001	1
− 0.5 LSB	0000 0000 0000	000	0
0V − 1.5 LSB	1111 1111 1111	FFF	−1
$-V_{REF}$ + 0.5 LSB	1000 0000 0000	800	−2048

While data is output on the falling edges of SCLK, receiving systems have the option of capturing the data on the subsequent rising or falling edge of SCLK. The maximum specification for t_{DA} (D_{OUT} access time after an SCLK falling edge) is provided for two power supply ranges. If the system is operating at the maximum clock frequency of 16 MHz and a V_D supply voltage of 3V, it would be necessary for the receiver to capture data on the subsequent falling edge of SCLK in order to guarantee performance over the entire temperature range. Operating at a V_D supply voltage of 5V or an SCLK frequency less than 10 MHz allows data to be captured on either edge of SCLK. If a receiving system is going to capture data on the subsequent falling edge of SCLK, it is important to make sure that the minimum hold time after an SCLK falling edge (t_{DH}) is acceptable. See Figure 5 for D_{OUT} hold and access times.

D_{OUT} is enabled on the falling edge of $\overline{CS}$ and disabled on the rising edge of $\overline{CS}$. If $\overline{CS}$ is raised prior to the 16th falling edge of SCLK, the current conversion is aborted and D_{OUT} will go into its high impedance state. A new conversion will begin when $\overline{CS}$ is taken LOW.

Applications Information

OPERATING CONDITIONS

We recommend that the following conditions be observed for operation of the ADC122S706:

$-40°C \le T_A \le +105°C$

$+4.5V \le V_A \le +5.5V$

$+2.7V \le V_D \le V_A$

$1V \le V_{REF} \le V_A$

$8\ MHz \le f_{SCLK} \le 16\ MHz$

V_{CM}: See Input Common Mode Voltage

POWER CONSUMPTION

The architecture, design, and fabrication process allow the ADC122S706 to operate at conversion rates up to 1 MSPS while consuming very little power. The ADC122S706 consumes the least amount of power while operating in power down mode. For applications where power consumption is critical, the ADC122S706 should be operated in power down mode as often as the application will tolerate. To further reduce power consumption, stop the SCLK while $\overline{CS}$ is high.

Short Cycling

Short cycling refers to the process of halting a conversion after the last needed bit is outputted. Short cycling can be used to lower the power consumption in those applications that do not need a full 12-bit resolution, or where an analog signal is being monitored until some condition occurs. For example, it may not be necessary to use the full 12-bit resolution of the ADC122S706 as long as the signal being monitored is within certain limits. In some circumstances, the conversion could be terminated after the first few bits. This will lower power consumption in the converter since the ADC122S706 spends more time in power down mode and less time in the conversion mode.

Short cycling is accomplished by pulling $\overline{CS}$ high after the last required bit is received from the ADC122S706 output. This is possible because the ADC122S706 places the latest converted data bit on D_{OUT} as it is generated. If only 8-bits of the conversion result are needed, for example, the conversion can be terminated by pulling $\overline{CS}$ high after the 8th bit has been clocked out.

Burst Mode Operation

Normal operation of the ADC122S706 requires the SCLK frequency to be sixteen times the sample rate and the $\overline{CS}$ rate to be the same as the sample rate. However, in order to minimize power consumption in applications requiring sample rates below 500 kSPS, the ADC122S706 should be run with an SCLK frequency of 16 MHz and a $\overline{CS}$ rate as slow as the system requires. When this is accomplished, the ADC122S706 is operating in burst mode. The ADC122S706 enters into power down mode at the end of each conversion, minimizing power consumption. This causes the converter to spend the longest possible time in power down mode. Since power consumption scales directly with conversion rate, minimizing power consumption requires determining the lowest conversion rate that will satisfy the requirements of the system.

Single DOUT mode

With the DUAL pin connected to a logic low level, the ADC122S706 is operating in single DOUT mode. In single DOUT mode, the conversion result of Channel A and Channel B are both output on D_{OUTA} (see Figure 2). Operating in this mode causes the maximum conversion rate to be reduced to 500kSPS while operating with an SCLK frequency of 16 MHz. This is a result of the conversion window changing from 16 clock cycles to 32 clock cycles to receive the conversion result of Channel A and Channel B. Since the conversion of Channel A and Channel B are still performed simultaneously, the ADC122S706 still enters a power down state on the 16th falling edge of SCLK. The increased time spent in power down mode causes the power consumption of the ADC122S706 to reduce nearly by a factor of two. See the Power Supply Characteristics Table for more details.

POWER SUPPLY CONSIDERATIONS AND PCB LAYOUT

For best performance, care should be taken with the physical layout of the printed circuit board. This is especially true with a low reference voltage or when the conversion rate is high. At high clock rates there is less time for settling, so it is important that any noise settles out before the conversion begins.

Analog and Digital Power Supplies

Any ADC architecture is sensitive to spikes on the power supply, reference, and ground pins. These spikes may originate from switching power supplies, digital logic, high power devices, and other sources. Power to the ADC122S706 should be clean and well bypassed. A 0.1 µF ceramic bypass capacitor and a 1 µF to 10 µF capacitor should be used to bypass the ADC122S706 supply, with the 0.1 µF capacitor placed as close to the ADC122S706 package as possible.

Since the ADC122S706 has both an analog and a digital supply pin, the user has three options. The first option is to tie the analog and digital supply pins together and power them with the same power supply. This is the most cost effective way of powering the ADC122S706 but it is also the least ideal. As stated previously, noise from the digital supply pin can couple into the analog supply pin and adversely affect performance. The other two options involve the user powering the analog and digital supply pins with separate supply voltages. These supply voltages can have the same amplitude or they can be different. The only design constraint is that the digital supply voltage be less than the analog supply voltage. This is not usually a problem since many applications prefer a digital interface of 3V while operating the analog section of the ADC122S706 at 5V. Operating the digital supply pin at 3V as apposed to 5V offers two advantages. It lowers the power consumption of the ADC122S706 and it decreases the noise created by charging and discharging the capacitance of the digital interface pins.

Voltage Reference

The reference source must have a low output impedance and needs to be bypassed with a minimum capacitor value of 0.1 µF. A larger capacitor value of 1 µF to 10 µF placed in parallel with the 0.1 µF is preferred. While the ADC122S706 draws very little current from the reference on average, there are higher instantaneous current spikes at the reference input.

The reference input of the ADC122S706, like all A/D converters, does not reject noise or voltage variations. Keep this in mind if the reference voltage is derived from the power supply. Any noise and/or ripple from the supply that is not rejected by the external reference circuitry will appear in the digital results. The use of an active reference source is recommended. The LM4040 and LM4050 shunt reference families and the LM4132 and LM4140 series reference families are excellent choices for a reference source.

PCB Layout

Capacitive coupling between the noisy digital circuitry and the sensitive analog circuitry can lead to poor performance. The solution is to keep the analog circuitry separated from the digital circuitry and the clock lines short as possible. Digital circuits create substantial supply and ground current transients. The logic noise generated could have significant impact upon system noise performance. To avoid performance degradation of the ADC122S706 due to supply noise, avoid using the same supply for the VA and VREF of the ADC122S706 that is used for digital circuitry on the board.

Generally, analog and digital lines should cross each other at 90° to avoid crosstalk. However, to maximize accuracy in high resolution systems, avoid crossing analog and digital lines altogether. It is important to keep clock lines as short as possible and isolated from ALL other lines, including other digital lines. In addition, the clock line should also be treated as a transmission line and be properly terminated. The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input pins and ground or to the reference input pin and ground should be connected to a very clean point in the ground plane.

A single, uniform ground plane and the use of split power planes are recommended. The power planes should be located within the same board layer. All analog circuitry (input amplifiers, filters, reference components, etc.) should be placed over the analog power plane. All digital circuitry and I/O lines should be placed over the digital power plane. Furthermore, the GND pin on the ADC122S706 and all the components in the reference circuitry and input signal chain that are connected to ground should be connected to the ground plane at a quiet point. Avoid connecting these points too close to the ground point of a microprocessor, microcontroller, digital signal processor, or other high power digital device.

APPLICATION CIRCUITS

The following figures are examples of the ADC122S706 in typical application circuits. These circuits are basic and will generally require modification for specific circumstances.

Data Acquisition

Figure 48 shows a basic low cost, low power data acquisition circuit. The analog and digital supply pins are powered by the system +5V supply and the 2.5V reference voltage is generated by the LM4040-2.5 shunt reference.

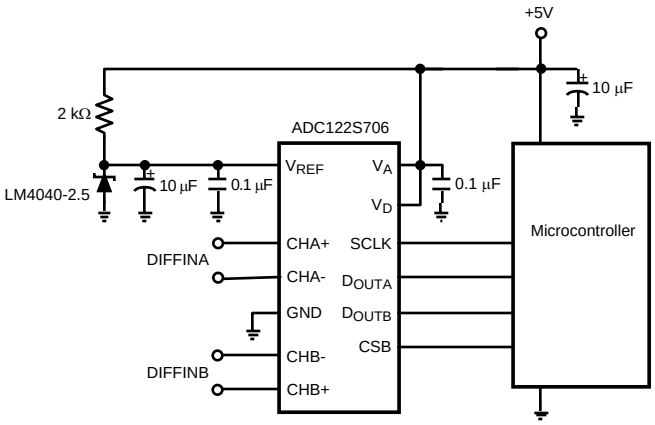


Figure 48. Low cost, low power Data Acquisition System

Current Sensing Application

Figure 49 shows an example of interfacing a pair of current transducers to the ADC122S706. The current transducers convert an input current into a voltage that is converted by the ADC. Since the output voltage of the current transducers are single-ended and centered around a common-mode voltage of 2.5V, the ADC122S706 is configured with the output of the transducer driving the non-inverting inputs and the common-mode output voltage of the transducer driving the inverting input. The output of the transducer has an output range of ±2V around the common-mode voltage of 2.5V. As a result, a series reference voltage of 2.0V is connected to the ADC122S706. This will allow all of the codes of the ADC122S706 to be available for the application. This configuration of the ADC122S706 is referred to as a single-ended application of a differential ADC. All of the elements in the application are conveniently powered by the same +5V power supply, keeping circuit complexity and cost to a minimum.

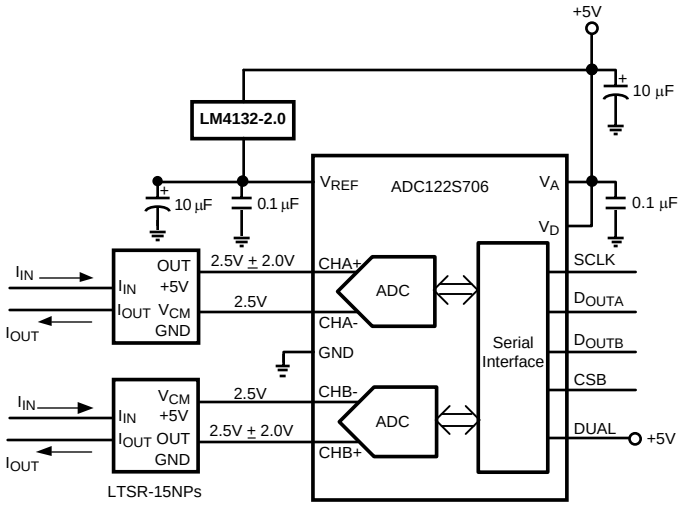


Figure 49. Interfacing the ADC122S706 to a Current Transducer

Bridge Sensor Application

Figure 50 shows an example of interfacing the ADC122S706 to a pair of bridge sensors. The application assumes that the bridge sensors require buffering and amplification to fully utilize the dynamic range of the ADC and thus optimize the performance of the entire signal path. The amplification stage for each ADC input consists of a pair of opamps from the LMP7704. The amplification stage offers the benefit of high input impedance and potentially high amplification. On the other hand, it offers no common-mode rejection of noise coming from the bridge sensors. The application circuit assumes the bridge sensors are powered from the same +5V power supply voltage as the analog supply pin on the ADC122S706. This has the benefit of providing the ideal common-mode input voltage for the ADC122S706 while keeping design complexity and cost to a minimum. The LM4132-4.1, a 4.1V series reference, is used as the reference voltage in the application.

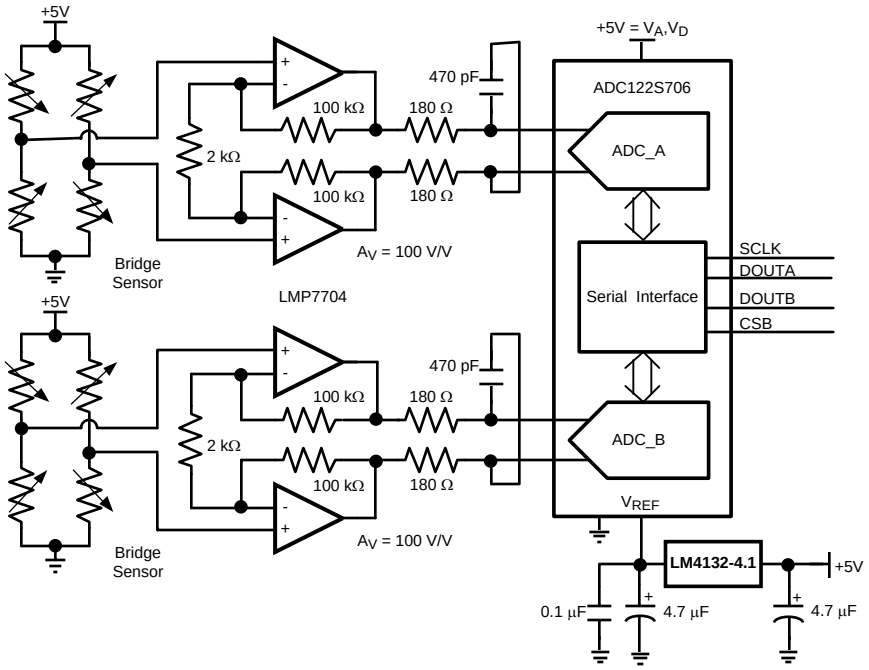


Figure 50. Interfacing the ADC122S706 to Bridge Sensors

REVISION HISTORY

Changes from Original (March 2013) to Revision A **Page**

- Changed layout of National Data Sheet to TI format 24

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADC122S706CIMT/NO.A	Active	Production	TSSOP (PW) | 14	94 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 105	2S706 CIMT
ADC122S706CIMT/NOPB	Active	Production	TSSOP (PW) | 14	94 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 105	2S706 CIMT
ADC122S706CIMTX/NO.A	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	2S706 CIMT
ADC122S706CIMTX/NOPB	Active	Production	TSSOP (PW) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 105	2S706 CIMT

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

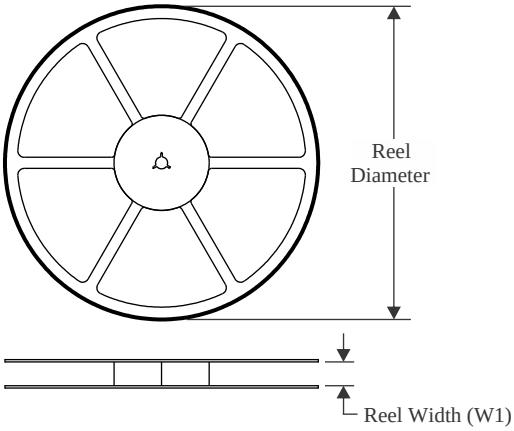
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

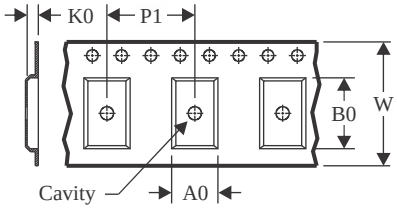
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

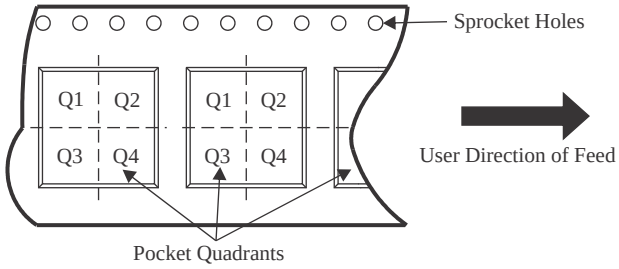


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

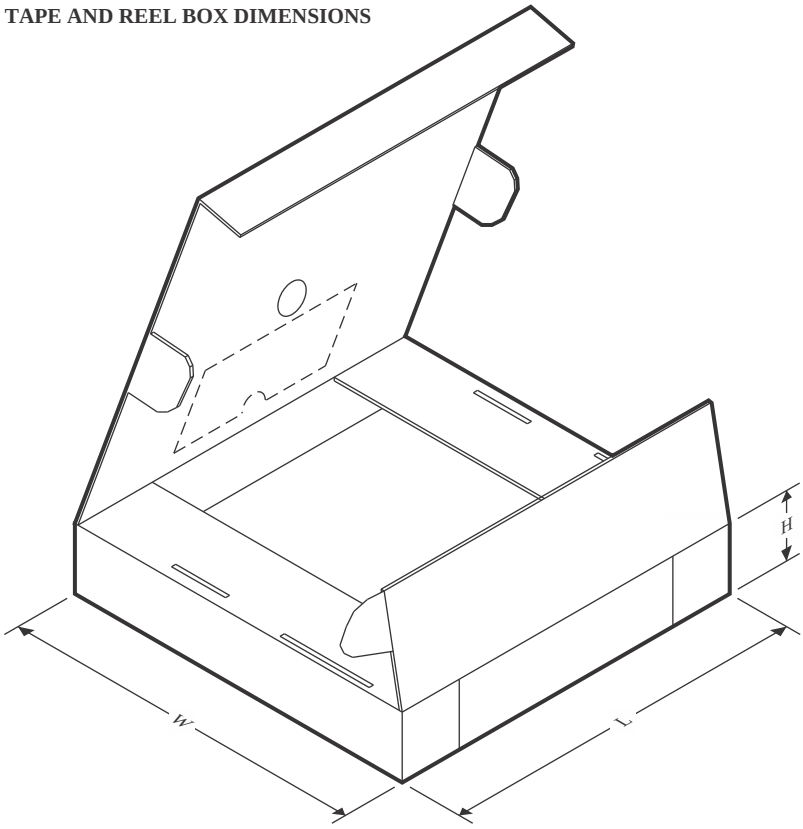
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC122S706CIMTX/ NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

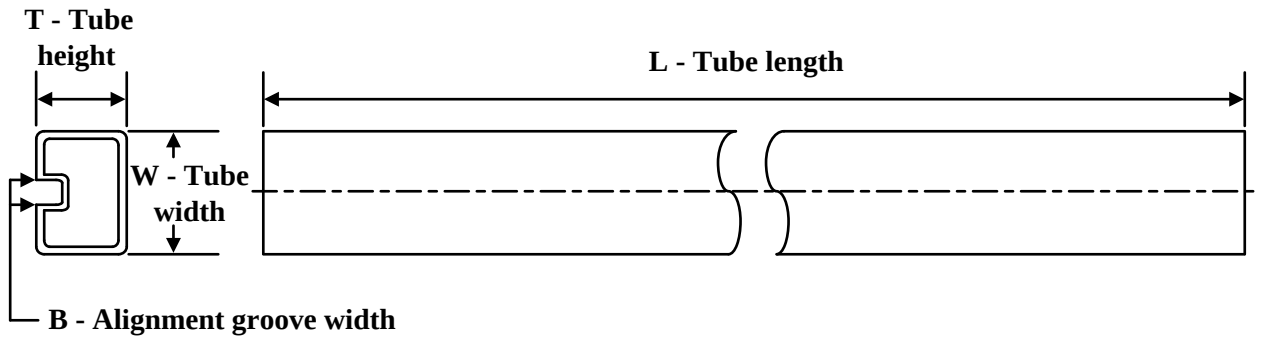
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC122S706CIMTX/ NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

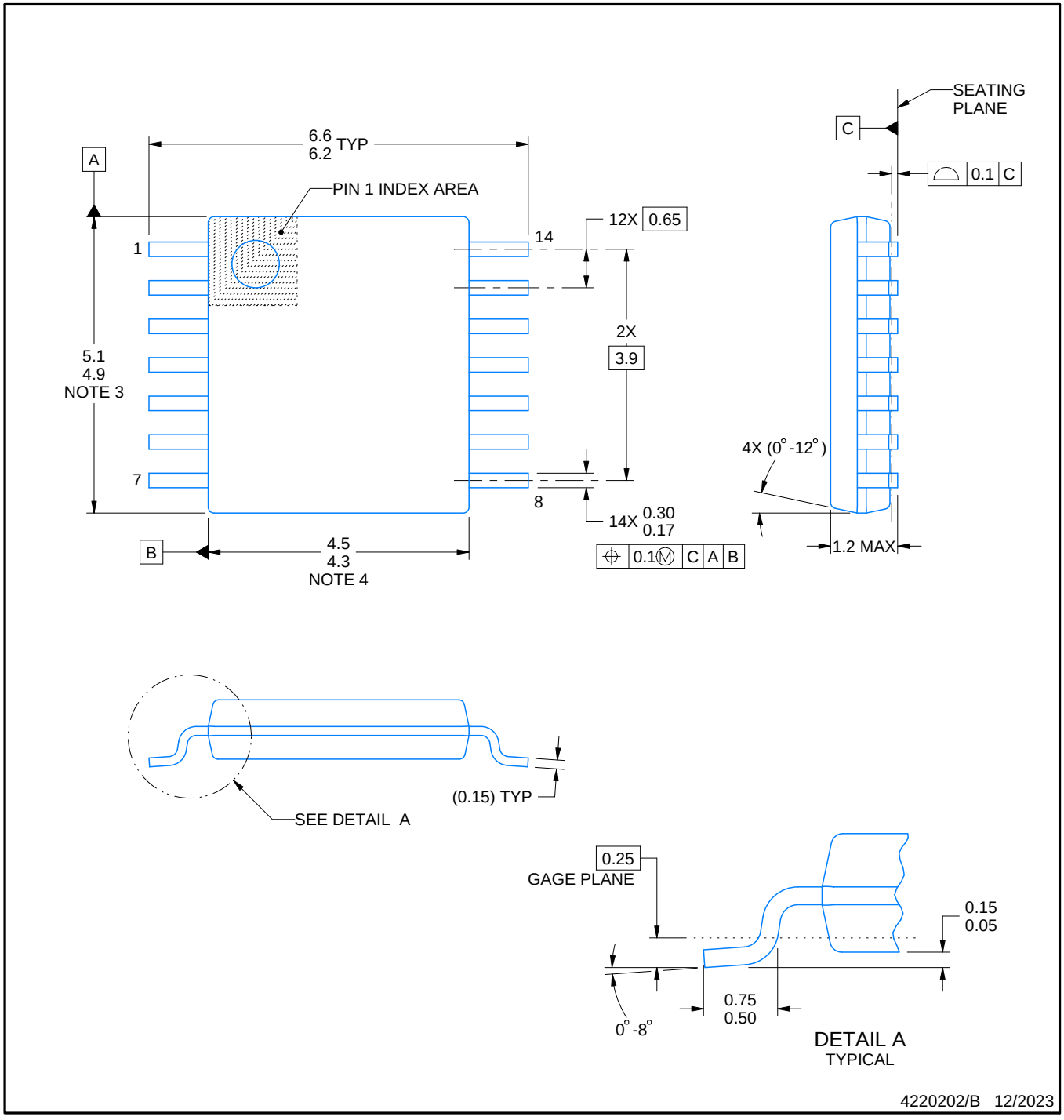
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ADC122S706CIMT/NO.A	PW	TSSOP	14	94	495	8	2514.6	4.06
ADC122S706CIMT/NOPB	PW	TSSOP	14	94	495	8	2514.6	4.06

PACKAGE OUTLINE

PW0014A

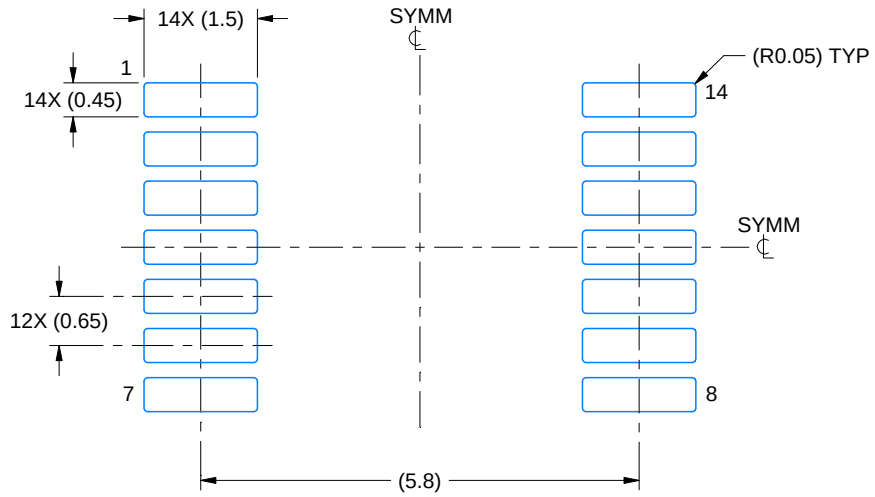
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

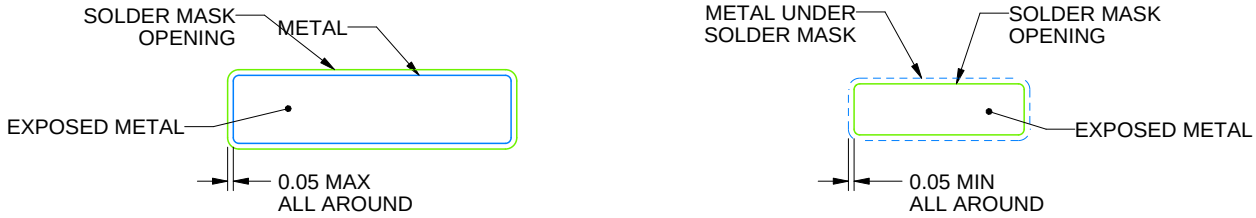


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

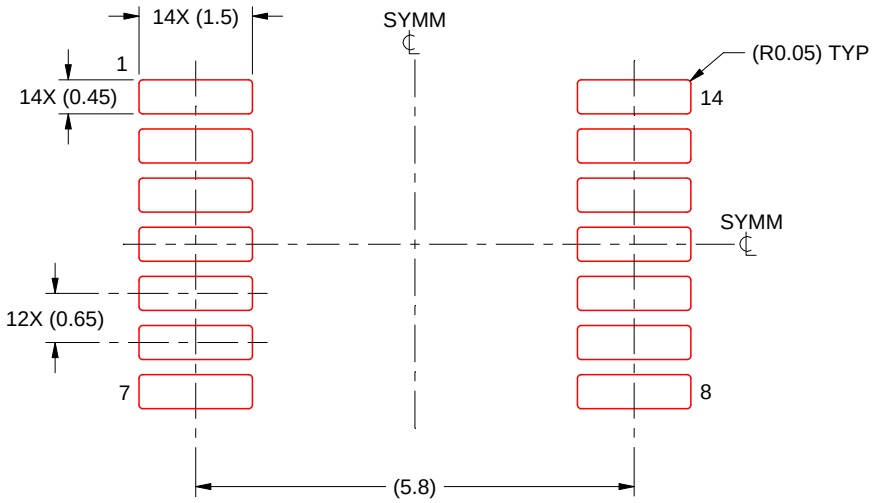


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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