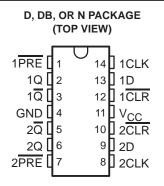
74ACT11074 DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

SCAS498A - DECEMBER 1986 - REVISED APRIL 1996

- Inputs Are TTL-Voltage Compatible
- Center-Pin V_{CC} and GND Configurations to Minimize High-Speed Switching Noise
- **EPIC™** (Enhanced-Performance Implanted CMOS) 1-µm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- **Package Options Include Plastic** Small-Outline (D) and Shrink Small-Outline (DB) Packages, and Standard Plastic 300-mil DIPs (N)



description

This device contains two independent positive-edge-triggered D-type flip-flops. A low level at the preset (PRE) or clear (CLR) input sets or resets the outputs regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the data (D) input meeting the setup-time requirements are transferred to the outputs on the low-to-high transition of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

The 74ACT11074 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

	INP	UTS		OUTPUTS			
PRE	CLR	CLK	D	Q	Q		
L	Н	Х	Χ	Н	L		
Н	L	X	Χ	L	Н		
L	L	X	Χ	H [†]	H [†]		
Н	Н	\uparrow	Н	Н	L		
Н	Н	\uparrow	L	L	Н		
Н	Н	L	Χ	Q ₀	\overline{Q}_0		

[†]This configuration is unstable; that is, it does not persist when either PRE or CLR returns to its inactive (high) level.



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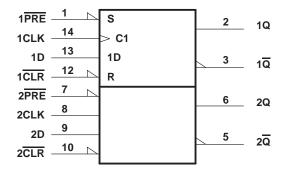
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logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		0.5 V to 6 V
Input voltage range, V _I (see Note 1)		$5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, VO (see Note 1)		$5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)		±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})		±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})		±50 mA
Continuous current through V _{CC} or GND		±100 mA
Maximum power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 2)): D package	1.25 W
	DB package	0.5 W
	N package	1.1 W
Storage temperature range, T _{stq}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. The maximum package power dissipation is calculated using a junction temperature of 150 °C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions

		MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	V
VIH	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
VI	Input voltage	0	VCC	V
Vo	Output voltage	0	VCC	V
loh	High-level output current		-24	mA
loL	Low-level output current		24	mA
Δt/Δν	Input transition rise or fall rate	0	10	ns/V
TA	Operating free-air temperature	-40	85	°C



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	Vaa	T,	4 = 25°C	;	MIN	MAX	UNIT
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	IVIIIV	IVIAA	UNIT
	Jour 50 "A	4.5 V	4.4			4.4		
	IOH = -50 μA	5.5 V	5.4			5.4		
Voн	Jan 24 mA	4.5 V	3.94			3.8		V
	IOH = -24 mA	5.5 V	4.94			4.8		
	$I_{OH} = -75 \text{ mA}^{\dagger}$	5.5 V				3.85		
	I _{OL} = 50 μA	4.5 V			0.1		0.1	
	10L = 30 μΑ	5.5 V			0.1		0.1	
VOL	le 24 mA	4.5 V			0.36		0.44	V
	I _{OL} = 24 mA	5.5 V			0.36		0.44	
	$I_{OL} = 75 \text{ mA}^{\dagger}$	5.5 V					1.65	
lį	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4		40	μΑ
Δl _{CC} ‡	One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V			0.9		1	mA
Ci	V _I = V _{CC} or GND	5 V		3.5				pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended ranges of supply voltage and free-air temperature (unless otherwise noted) (see Figure 1)

			T _A = 2	25°C	MIN	MAX	UNIT	
			MIN	MAX	IVIIIV	IVIAA	UNIT	
fclock	Clock frequency		0	100	0	100	MHz	
	Pulse duration	PRE or CLR low			5		no	
t _w	ruise duration	CLK low or high	5		5		ns	
	Oct on these hartests OLIVA	Data high or low	4.5		4.5			
t _{su}	Setup time before CLK↑	PRE or CLR inactive	active 2		2		ns	
t _h	Hold time after CLK↑		0		0		ns	

switching characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	T,	_Δ = 25°C	;	MIN	MAX	UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	IVIIIN		UNIT
f _{max}			100	125		100		MHz
t _{PLH}	PRE or CLR	0 0 7 0	1.5	5.7	8.9	1.5	9.6	no
^t PHL	PRE OF CLR	Q or Q	1.5	6.6	11.3	1.5	12.5	ns
t _{PLH}	CLK	Q or $\overline{\mathbb{Q}}$	1.5	6	8.5	1.5	9.4	20
t _{PHL}	CLN	QUIQ	1.5	5.7	8	1.5	8.8	ns

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

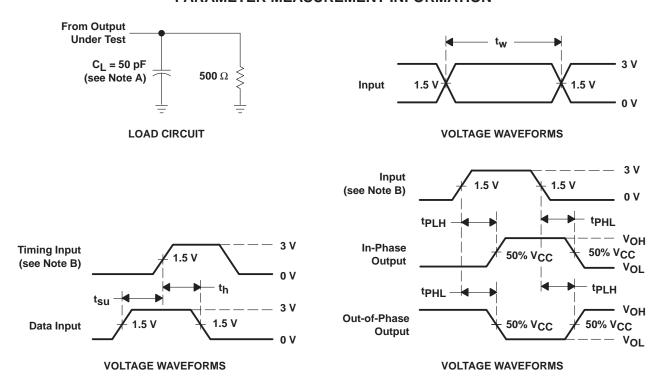
	PARAMETER	TEST CON	TYP	UNIT	
C _{pd}	Power dissipation capacitance per flip-flop	C _L = 50 pF,	f = 1 MHz	30	pF



[‡]This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

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PARAMETER MEASUREMENT INFORMATION



NOTES: A. CL includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \ \Omega$, $t_f = 3 \ ns$, $t_f = 3 \ ns$.
- C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
74ACT11074D	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT11074
74ACT11074D.A	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT11074
74ACT11074DBR	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AT074
74ACT11074DBR.A	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AT074
74ACT11074N	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	74ACT11074N
74ACT11074N.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	74ACT11074N
74ACT11074NSR	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT11074
74ACT11074NSR.A	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT11074

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





	•
A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device		Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74ACT11074DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
74ACT11074NSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74ACT11074DBR	SSOP	DB	14	2000	353.0	353.0	32.0
74ACT11074NSR	SOP	NS	14	2000	353.0	353.0	32.0

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
74ACT11074D	D	SOIC	14	50	506.6	8	3940	4.32
74ACT11074D.A	D	SOIC	14	50	506.6	8	3940	4.32
74ACT11074N	N	PDIP	14	25	506	13.97	11230	4.32
74ACT11074N	N	PDIP	14	25	506	13.97	11230	4.32
74ACT11074N.A	N	PDIP	14	25	506	13.97	11230	4.32
74ACT11074N.A	N	PDIP	14	25	506	13.97	11230	4.32



SMALL OUTLINE INTEGRATED CIRCUIT



- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.





SMALL OUTLINE PACKAGE



- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-150.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



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